

BOSTON



THE REFLECTOR

ISSUE #10
OCTOBER 2017

CALL FOR SPEAKERS
AND COURSES

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SYMPOSIUM
CALL FOR PAPERS,
(DEADLINE, OCT. 16)

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INVITED TO
SUBMIT AN
ARTICLE

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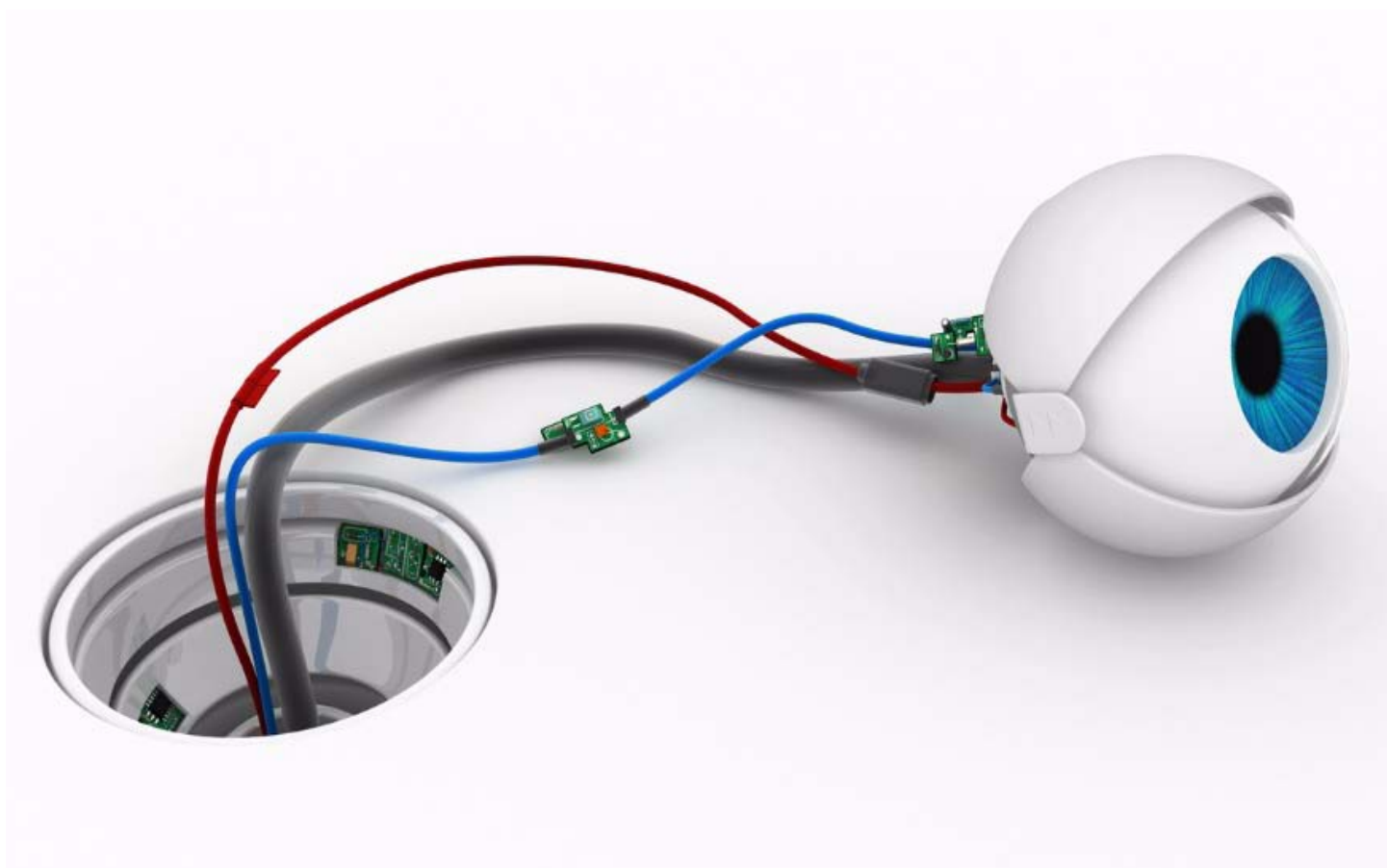


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So Long Cassini, It's Been Good to Know Ya'

Fausto Molinet, Publications Chair and Charles Recchia, Chair,
Boston Section Chapter of the Reliability Society

By the time of this editorial the Cassini Spacecraft has taken its final observations at Saturn and has been destroyed. It was a grand finale to a long and very successful 13-year mission that has yielded an immense amount of science contributing to our understanding of our solar system and the universe. It achieved virtually 100% of the mission goals.

If you follow this stuff, you can't help but be in awe of the scientists and engineers who planned, designed, built and executed this feat, much of it from a distance of over 800 million miles. It also lost nearly 8000 pounds (I wish I could lose weight on a trip). You can learn a lot more about Cassini from the JPL/NASA website.

Cassini would make a great topic for any of our chapter meetings. There is something in it for everyone, but I'd like to focus on just one here. That's reliability. We have a chapter for that.

Twenty-seven nations contributed to this program which travelled 4.9 billion miles, took 455,248 images and executed 2.5 million commands along with 360 engine burns. It had to work all the time, every time. That's all not counting the things here on earth and in space that had to support it all and the processes and procedures that had to be developed and tested here before being sent to the spacecraft.

Charles Recchia, chair of the Boston Section Chapter of the Reliability Society commented, "It's been my experience that a sizeable portion of research and development time is allocated to ensuring that the product or technology in question can meet reliability requirements. The degree of rigor applied and breadth of disciplines involved – from materials science to risk assessment statistics to computer science, etc. -- when ensuring spacecraft mission reliability is second to none".

The Boston Chapter of the IEEE Reliability Society has been in existence since 1960, making it one of the oldest chapters across all of the IEEE Societies worldwide, and the single largest Chapter in the Reliability Society globally. Serving out his last year as the Chapter's 33rd chairperson, Recchia looks forward to monthly Chapter meetings which are typically held at MIT Lincoln Laboratory in Lexington, and to working closely with past chairs including Daniel Weidman, Ramon de la Cruz, Don Markuson, Giora Kuller, Jeff Clark, and Gene Bridgers in keeping the rich tradition of technical fellowship thriving.

Reliability improves just about everything in our lives. It's important so why not investigate it further. It might just improve whatever it is you do.

Deadline: October 16, 2017!!!

Call for Papers and Posters

2018 IEEE International Symposium on Technologies for Homeland Security

2 – 3 May 2018 DoubleTree Hotel, Crystal City, VA

<http://ieee-hst.org/>



Sponsor:



Call for Papers & Posters

The 18th annual IEEE Symposium on Technologies for Homeland Security (HST '18), will be held 2 – 3 May 2018, in the greater Washington D.C. area. This symposium brings together innovators from leading academic, industry, businesses, Homeland Security Centers of Excellence, and government agencies to provide a forum to discuss ideas, concepts, and experimental results.

Produced by IEEE with technical support from DHS S&T, IEEE, IEEE Boston Section, and IEEE-USA and organizational support from MIT Lincoln Laboratory, Raytheon, and MITRE, this year's event will once again showcase selected technical papers and posters highlighting emerging technologies to:

Secure Cyberspace

Enhance Biometrics & Forensics

Secure Land and Maritime Borders

Prevent Terrorism & Manage Incidents

We are currently seeking technical paper and poster session submissions in each of the areas noted above. Papers examining the feasibility of transition to practice will also be considered. *This year, papers focused on DHS high-priority technology gaps will be of particular interest.* All areas will cover the following common topics:

- Strategy and threat characterization, operational concepts, risk analysis;
- Modeling, simulation, experimentation, and exercises & training; and
- Testbeds, standards, performance and evaluations.

Contact Information

For more detailed information on the Call for Papers and Posters, as well as Sponsorship and Exhibit Opportunities, visit the website <http://ieee-hst.org/> or email: information@ieee-hst.org. Submissions should be made at the following website: <https://cmt3.research.microsoft.com/HST2018>

Important Dates

Paper Extended Abstract and Poster Abstract Deadline:	October 16, 2017
Paper, Poster Acceptance Notification	December 15, 2017
Final Paper Submission Deadline:	March 30, 2018

All deadlines are by midnight Eastern Time.

Organizing Committee

General Chairs:	James Flavin, MIT Lincoln Laboratory Jordan Feidler, MITRE
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Karen Panetta, Tufts University
Rich Moro, Raytheon
John Aldridge, MIT Lincoln Laboratory
Secure Cyberspace
Claire Applegarth, MITRE
Mark Peters, MITRE

Call for Articles

Now that the Reflector is all electronic, we are expanding the content the publication. One of the new features we will be adding are technical and professional development articles of interest to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development articles should have broad applicability to the engineering community and should not explicitly promote services for which

a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional articles will be reviewed by the publications committee for suitability. The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to;
ieeebostonsection@gmail.com

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Entrepreneurs' Network, and Technology and Engineering Management Society – 6:30PM, Tuesday, 3 October

SBIR Grants and Non-Dilutive Funding to Bootstrap your Start-up Company

Meeting location – Constant Contact, 1601 Trapelo Road, 3rd Floor, Great Room, Waltham, MA.

PRE-MEETING DINNER at 5:15 PM (sharp) at Bertucci's, Waltham.

Starting a company to transform a great idea to a product or service can be fun and exciting. It usually requires lots of hard work and often and lots of money too. Entrepreneurs not blessed with a trust fund, wealthy relatives or a winning Powerball scratch ticket, have to get that money from somewhere. Venture Capital or Angel investors can be helpful, if the new company fits in with their investment strategy and interests, but this is expensive money that is very picky, usually impatient and can be as elusive as a winning lottery ticket.

Non-dilutive funding, generally in the form of grants from government agencies or private foundations, or even corporate partnerships, can give an entrepreneur the opportunity to launch a company and to build value without having to give up control or equity. And if equity investment ultimately becomes necessary, having built and demonstrated value can be quite beneficial in negotiations with investors.

During our October 3 meeting our panel will share their insights and experiences regarding non-dilutive funding – join us for inspiration and networking.

Agenda:

- 6:30-7:30 PM - Registration & networking
- 7:30-7:40 PM - ENET Chairman's announcements
- 7:40-7:55 PM - E Minute - Up to 3 Startup companies' presentations
- 7:55-8:45 PM - 3 expert speakers on the night's topic
- 8:45-9:00 PM - Audience / Speakers Q & A
- 9:00-9:30 PM - Final networking including meeting speakers

Speakers: Laura M. Hales, Ph.D. is a cofounder and Chief Business Officer of Extend Biosciences Inc., an emerging biotechnology company that is developing a novel drug delivery platform technology that improves



the pharmacokinetic properties of peptides and proteins.

At Extend Biosciences, Dr. Hales manages all of the outsourcing, operational and business development activities for the company. She has also been instrumental in obtaining the \$6M+ in SBIR grants

and other non-dilutive funding the company has received from multiple state and federal agencies.

Dr. Hales is also the Founder and Principal at The Isis Group, where her primary focus is to assist life science entrepreneurs in new business formation and non-dilutive funding efforts. Dr. Hales received her Ph.D. at the University of Illinois at Urbana-Champaign and was a postdoctoral fellow at Columbia University. She worked in the startup biotech industry for 9 years before co-founding Extend Biosciences.



Stephen Y. Chow, Esq., Partner, Burns & Levinson, LLP

Over three decades of practice, Attorney Stephen Y. Chow has developed numerous patent portfolios and strategies for a variety of industries including IT, chemical and life sciences enterprises, litigated patent, copyright, trademark, trade secret, antitrust, unfair competition, international trade, telecommunications and e-commerce cases before state and federal courts and agencies. Mr. Chow has coordinated or served as an expert in litigation before foreign tribunals. He has also advised manufacturers, telecommunications carriers, commercial exchanges and educational, financial and research institutions on commercial, legislative and regulatory matters, particularly in internal policies and development of new services and products, as well as in early-stage financing.

Mr. Chow sees himself as a strategist and trouble-

shooter for technology companies in financial, governance and intellectual property disputes and development. In particular, he offers integrated patent, technology and business prosecution, assessment and enforcement with the commensurate benefits.

From 1995-2013, Mr. Chow taught corporate, intellectual property and litigation practice at Suffolk University Law School, including the perennial "Counseling Technology-Leading Emerging Enterprises," and since then has been teaching a similar course at Boston University School of Law. In 1997, he was elected to the American Law Institute, for which he has been active on consultative committees on contract, corporate, employment, intellectual property, international and privacy law



Dr. Jeffrey Everson is the founder of J.H. Everson Consulting, where he assists clients in the pursuit of revenue generating opportunities by performing detailed technology and market studies based on the intersection of technologies, markets, environmental issues, and policies. This support includes

white papers and proposals to commercial and government organizations, including the Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) programs.

He specializes in Sensor Systems, Sensor Technology Development, and Collision Warning Systems for Roadway Vehicle Safety. Previously, he was Director of Business Development at Qinetiq North America, in Waltham, MA (previously Foster-Miller, Inc.). He started at Foster-Miller as a Senior Engineer at where he served as the principal investigator (PI) for multiple Small Business Innovation Research (SBIR) programs, including an inner city transit bus crash warning system, for which he won a national SBIR Tibbetts award.

Dr. Everson has a BS and MS in physics from Northeastern University with a minor in German and a PhD in physics from Boston College. For more information, please see www.JHEversonConsulting.com



Moderator:

Roger Frechette is Founder and Principal of New England PharmAssociates, LLC, a consultancy offering on-demand executive and business advisory services to life sciences en-

terprises. Dr. Frechette has been a volunteer with Boston ENET since 2014, and supports area start-ups as a mentor for MassBio's MassCONNECT Program and the MTTC's Platform Program.

Previously, Dr. Frechette was Co-Founder of MaxThera, an antibacterial drug discovery company funded exclusively through SBIR and US BioShield grants. MaxThera was sold in 2010 to Biota Holdings Limited, a Melbourne Australia anti-infectives company. Prior to starting MaxThera, Dr. Frechette was Project Director at Paratek Pharmaceuticals (Boston). At Paratek he led the team that discovered PTK0796 (currently in Phase III clinical trials) with strategic partner Glaxo-Wellcome. Previously, he was Associate Director of Chemistry at RiboGene (Hayward, CA). He began his career as a medicinal chemist at the R.W. Johnson Pharmaceutical Research Institute (J&J, Raritan, NJ).

Dr. Frechette was a Post-Doctoral Fellow at Yale University, earned his PhD in Organic Chemistry from Wesleyan University and his BA in Chemistry from College of the Holy Cross.

E-Minute Presentations: These 1 ½ minute presentations enable startup entrepreneurs to gain experience in presenting their summary to expert panels and audiences.

Refreshments: Cheese, crackers, chips, cookies, soft drinks & juice

Reservations: Free to ENET members and \$20 for non-members. No reservations are needed for the pre-meeting dinner. Members & non-members, pre-register for the meeting online, until midnight the day before the meeting. If you cannot pre-register, you are welcome to register at the door.

Pre-Meeting Dinner: Join us for a pre-meeting networking dinner (self-pay) at Bertrucci's in Waltham prior to the start of this meeting. Dinner at 5:15 sharp.

Constant Contact is adjacent to RT 128 / 95 at Exit 28B. See: <http://www.constantcontact.com/about-constant-contact/office-location-waltham.jsp>

IEEE Boston Section Online Courses:

(Students have 90 day access to all online, self-paced courses)

Verilog101:Verilog Foundations

Full course description and registration at ,
<http://ieeeeboston.org/verilog-101-verilog-foundations-online-course/>

System Verilog 101: Design Constructs

Full course description and registration at ,
<http://ieeeeboston.org/systemverilog-101-sv101-design-constructs-online-course/>

System Verilog 102: Verification Constructs

Full course description and registration at ,
<http://ieeeeboston.org/systemverilog-102-sv102-verification-constructs-online-course/>

High Performance Project Management

Full course description and registration at ,
<http://ieeeeboston.org/high-performance-project-management-online-course/>

Introduction to Embedded Linux Part I

Full course description and registration at ,
<http://ieeeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/>

Embedded Linux Optimization - Tools and Techniques

Full course description and registration at ,
<http://ieeeeboston.org/embedded-linux-optimization-tools-techniques-line-course/>

Software Development for Medical Device Manufacturers

Full course description and registration at ,
<http://ieeeeboston.org/software-development-medical-device-manufacturers-line-course/>

Fundamental Mathematics Concepts Relating to Electromagnetics

Full course description and registration at ,
<http://ieeeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/>

Reliability Engineering for the Business World

Full course description and registration at ,
<http://ieeeeboston.org/reliability-engineering-business-world-line-course/>

Communications, and Photonics Societies – 7:00PM, Thursday, 5 October

Laser Communications from the Moon

Don Boroson, MIT Lincoln Laboratory



Verizon Technology Center, 60 Sylvan Rd., Waltham, MA 02451.

This meeting is preceded by dinner with our guest speaker at Bertucci's, 475 Winter St, Waltham, MA at 5:30 PM.

Engineers have been trying to solve the free-space, high-rate laser communications problem for several decades. However, it is only since about 2001 that the technology has really taken off, with LEO and GEO systems successfully demonstrated by teams around the world. Then, in 2013, MIT Lincoln Laboratory built and operated NASA's Moon-to-Earth high rate duplex lasercom system called LLCD, the Lunar Laser Communication Demonstration. This system successfully demonstrated data rates up to 622 Mbps from a lunar-orbiting unmanned spacecraft to each of several optical ground terminals, and up to 20 Mbps on the uplink. The error-free links were used to transmit large data files much faster than ever demonstrated at lunar ranges, real-time spacecraft commands and telemetry, and high-definition video, both recorded and live, to the great amusement of the observers in the ground operations center. The wide bandwidths of both the uplink and downlink optical signals were also configured to achieve real-time continuous ranging with an accuracy better than one centimeter whenever the comm links were running.

The talk will give an overview of the system and its novel designs as well as the mission operations and lasercom performance. It will also discuss the after effects of the mission, including a quick snapshot of the ongoing effort to fly a similar terminal on the upcoming manned Orion missions.

Don Boroson received his BSE and PhD degrees in Electrical Engineering from Princeton University. He has spent his entire career at the MIT Lincoln Laboratory in Lexington, Massachusetts, where he is now a Labora-

tory Fellow in the Communications Division. Active in the lasercom community for 30 years, Dr. Boroson has led a number of projects designing, modeling, building, and testing high data rate laser communications systems for space applications. Recently, he acted as the Principal Investigator and Lincoln Program Manager for the NASA Lunar Laser Communication Demonstration project, which set many records including being the first laser communications system to operate at lunar distances. Don is the author of many journal and conference papers, and is a Fellow of the SPIE.

Please circulate to interested parties.

Venue Note. This is our venue at the new Verizon Technology Center Campus in Waltham.

The meeting begins at 7 PM at the new meeting auditorium at the Verizon Technology Center. The address is 60 Sylvan Road, Waltham, MA 02451. The entrance is by the far corner – with the picnic tables out front – and not the tower or the new building. It is most easily reached by the West Street entrance.

Important Note: Verizon Technology Center requests the names of the meeting attendees in advance of the meeting. If you plan to attend, please send a note via e-mail with your name to John Nitzke at RF@ieee.org by Wednesday, October 4th .

The meeting is preceded by dinner at Bertucci's, 475 Winter St, Waltham at 5:30 PM. The speaker will be joining us at dinner.

Directions to Bertucci's restaurant in Waltham: Take Exit 27B on I95/128, heading west on Winter Street. After exiting, stay all the way to the right and take the first right turn into the shopping plaza.

Please let Bob Malupin know if you plan to attend the dinner at Bertucci's. Bob can be contacted at Robert.Malupin@VerizonWireless.com .

Directions to Verizon Technology Center (old Verizon Labs location), 60 Sylvan Rd. campus, Waltham, MA 02451:

Take Exit 27B on I95/128, heading west on Winter Street. Stay all the way to the right. Verizon Technology Center is 1/2 mile ahead. At the second traffic light,

turn left onto WEST ST. and then take the first right (at the Verizon sign) which leads into the Verizon campus. Take the first left. The building and entrance for the meeting are on your right. Note that the entrance to the auditorium area is by the far corner – with the picnic tables out front – and not the tower or the new building.

Life Members – 4:00PM, Wednesday, 11 October

History of the USS Constitution - The story of its drydocking and repair

LCDR Timothy R. Anderson



Timbers and masts representing 200 years of “America’s Ship of State” have been repaired or replaced. New planks of appropriate wood have been obtained to duplicate and replace the existing ones. Copper sheets have been replaced to protect the hull from both invasive species and barnacles.

This massive repair has been done at regular intervals to preserve and protect the oldest fighting ship afloat in the world.

Lt. Cmdr. Timothy RO Anderson, United States Navy, Executive Officer, USS CONSTITUTION

Lieutenant Commander Timothy R. Anderson was raised in Champaign, Illinois. He attended the University of Illinois where he received a Bachelor of Arts degree in Political Science and was commissioned as an Ensign through the Naval Reserve Officer Training Corps (NROTC) in 2003.

LCDR Anderson’s initial sea duty was USS GLADIATOR (MCM 11), USS DEXTROUS (MCM 13) and USS FARRAGUT (DDG 99). He volunteered to deploy to Iraq as part of the stand-up of Joint CREW Composite

Squadron-One (JCCS-I) in the counter IED effort.

LCDR Anderson reported to the University of Missouri NROTC Unit in May of 2007 as a Naval Science Instructor where he earned his Master of Science degree in Parks, Recreation and Tourism in 2010.

Following this, he reported to Department Head School in Newport, R.I. and served operationally as the Chief Engineer of USS ROSS (DDG 71) and USS MONTE-REY (CG 61), deploying in support of theatre ballistic missile defense in the Arabian Gulf and Mediterranean Sea.

LCDR Anderson reported to USS CONSTITUTION in May 2015 as the Executive Officer for America’s Ship of State.

LCDR Anderson’s personal awards include the Navy and Marine Corps Commendation Medal (3 awards), the Navy and Marine Corps Achievement Medal (3 awards) and numerous campaign and unit awards.

Meeting Location: Lincoln Lab Auditorium, 244 Wood Street, Lexington, MA.

Reliability Society – 5:30PM, Wednesday, 11 October

The Genesis of Reliability Engineering aka “Certainty of Operations”

Gilmore G. Cooke, PE



The first two individuals to introduce reliability engineering in their work were: Dr. William Channing (1820 -1901), inventor of Boston’s fire alarm system over 160 years ago, and Fred Stark Pearson (1861-1915), chief engineer of the world’s first and largest public transit system of Boston. Channing had carefully examined and specified re-

quirements for communicating fire emergencies, coining the phrase ‘unerring certainty of operations’. Channing then incorporated certain design features to guard against circuit interruptions and false alarms. These included redundant conductors, separation of circuits, monitoring of circuits, and automatic testing of wires. In his paper to the Smithsonian Institution in 1855, he reported that the overall design had proved sufficient to make Boston’s fire alarm system the ‘most certain means of communications which has yet been devised, under all conditions of weather and seasons’.

Decades later when Pearson was an engineering student at Tufts College, he visited Boston’s central fire alarm station with Professor Dolbear. He became a disciple of Channing by expanding his motto to ‘taking the public view with regards to certainty of operations’.

Pearson applied reliability engineering concepts to develop power and traction systems in Boston, Manhattan, Niagara Falls, Mexico City, Sao Paulo, Rio de Janeiro and Barcelona.

Gilmore G. Cooke, PE of IEEE Boston Section History and Milestones Committee

Gilmore Cooke is Chair of the History and Milestones Committee of the IEEE Boston Section as well as its Secretary. He is a Professional Engineer in Massachusetts and California. He has worked throughout his career on large engineering and construction projects, both locally and throughout in the United States. He received the Bachelor of Electrical Engineering degree in 1962. He is a volunteer in the IEEE and belongs to various historical societies. He’s published numerous articles on electrical engineering history and wrote The Story of L-Street Power Station, 1898-2006. He teaches a class to adults at the community college entitled History of Wired and Wireless Communications on Cape Cod.

Email: gilcooke@ieee.org

Meeting Location: 3 Forbes Rd, Lexington, Massachusetts, 02421

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LinkedIn: <https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about>

Power Electronics Society – 4:00PM, Thursday, 12 October

SMART Power Flow Controllers for Smart Grid Applications

Kalyan K. Sen, PhD, PE, MBA - Fulbright Scholar



Schedule:

4:00 - 4:15 Arrival and sign in

4:15 - 6:15 Technical Presentation

6:15 - 7:00 Dinner (Pizza and Salad) and Networking

Meeting Location: MathWorks Campus, 1 Apple Hill Drive, Natick, MA 01760

Increasing transmission capacity is essential to meet an increased demand of electricity, integration of renewable generation and so on. The power industry's pressing need for the most economical ways to transfer bulk power along a desired path may be met by building new transmission lines, which is a long and costly process. Alternately, it may be quicker and cheaper to increase the available transfer capacity of the existing transmission lines with a power flow controller. Power flow control techniques have been practiced, from using inductors, capacitors, transformers and load tap changers in the earlier days of electrical engineering to power electronics-based solutions in recent years. Even though the costs and complexities of the available solutions vary widely, the basic underlying theory of power flow control is still the same as it always has been. To recommend proper solutions, SMART Power Flow Controllers (SPFC) are designed based on functional requirements and cost-effective solutions.

A SPFC is a Power Flow Controller that is derived from utilizing the best features of all the technical concepts that are developed in the power flow control area until now. A SPFC fulfills the true needs of a utility for its everyday use and they are high reliability, high efficiency, low installation and operating costs, component non-obsolescence, fast enough response for utility applications, high power density, interoperability, and easy relocation to adapt to changing power system's needs

while providing the optimal power flow control capability. The audience will hear from an expert who actually designed and commissioned a few power electronics-based power flow controllers since its inception in the 1990s.

The presentation will be of particular interest to all utility power engineering professionals. The required background is an equivalent of an electrical engineering degree with familiarity in power engineering terminology. Topics include principles of active and reactive power compensation; traditional power flow controllers – voltage regulating transformer, phase angle regulator, shunt inductor/capacitor, series inductor/capacitor; voltage-sourced converter (VSC), VSC-based technology and its implementation, comparison of simulation and field results; Sen Transformer.

Speaker: Kalyan Sen, a newly-selected Fulbright Scholar, is the Chief Technology Officer of Sen Engineering Solutions, Inc. (www.sentransformer.com) that specializes in developing SMART power flow controllers—a functional requirements-based and cost-effective solution. He spent 30 years in academia and industry and became a Westinghouse Fellow Engineer. He was a key member of the Flexible Alternating Current Transmission Systems (FACTS) development team at the Westinghouse Science & Technology Center in Pittsburgh. He contributed in all aspects (conception, simulation, design, and commissioning) of FACTS projects at Westinghouse. He conceived some of the basic concepts in FACTS technology. He has authored or co-authored more than 25 peer-reviewed publications, 8 issued patents, a book and 4 book chapters in the areas of FACTS and power electronics. He is the coauthor of the book titled, *Introduction to FACTS Controllers: Theory, Modeling, and Applications*, IEEE Press and John Wiley & Sons, Inc. 2009, which is also published in Chinese and Indian paperback editions. He is the co-inventor of Sen Transformer. He received BEE, MSEE,

and PhD degrees, all in Electrical Engineering, from Jadavpur University, India, Tuskegee University, USA, and Worcester Polytechnic Institute, USA, respectively. He also received an MBA from Robert Morris University, USA. He is a licensed Professional Engineer in the Commonwealth of Pennsylvania. He is a Distinguished Toastmaster who led District 13 of Toastmasters International as its Governor to be the 10th-ranking District in the world in 2007-8.

Kalyan, a Senior Member of IEEE, has served the organization in many positions. Under his leadership, IEEE Pittsburgh Section and its three chapters (PES, IAS and PELS) received the Best Section and Chapter Awards. His other past positions included Editor of the IEEE Transactions on Power Delivery (2002 – 2007), Technical Program Chair of the 2008 PES General Meeting in Pittsburgh, Chapters and Sections Activities Track Chair of the 2008 IEEE Sections Congress in Quebec City, Canada, PES R2 Representative (2010 and 2011) and Member of the IEEE Center for Leadership Excellence (CLE) Committee (2013, 2014). He has been serving as an IEEE PES Distinguished Lecturer since 2002. In that capacity, he has given presentations on power flow control technology more than 100 times in 15 countries. He is an inaugural class (2013) graduate of the IEEE CLE Volunteer Leadership Training (VOLT) program. Kalyan is the recipient of the IEEE Pittsburgh Section PES Outstanding Engineer Award (2004) and Outstanding Volunteer Service Award for reviving the

local Chapters of PES and IAS from inactivity to world-class performance (2004). He has been serving as the Special Events Chair of the IEEE Pittsburgh Section for the last decade. He is the Region 1-3 Coordinator of Power Electronics Society. For more details, click on http://ieee-pes.org/images/files/pdf/chapters/archive/April2009_Chapters_Sen_PES_Volunteer.pdf

Selected publications:

K. K. Sen, M. L. Sen, "Phase Angle Regulation Versus Impedance Regulation: Which Offers Greater Control Of Power Flow On the Grid?," How2Power.com Today, February, 2017.

http://www.how2power.com/newsletters/1702/articles/H2PToday1702_design_Sen.pdf?NOREDİR=1

K. K. Sen, "Overview Of Voltage Regulation Schemes For Utility And Industrial Applications," How2Power.com Today, September, 2015.

http://www.how2power.com/newsletters/1509/articles/H2PToday1509_design_Sen.pdf?NOREDİR=1

K. K. Sen, "Practical Power Flow Controller Brings Benefits of Power Electronics to the Grid," How2Power.com Today, March, 2015.

http://www.how2power.com/newsletters/1503/articles/H2PToday1503_design_Sen.pdf?NOREDİR=1

M. L. Sen and K. K. Sen, "Introducing the SMART Power Flow Controller - an Integral Part of Smart Grid," IEEE Electrical Power and Energy Conference, Paper no. 4, October 2012, London, Canada.

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Consultants Network – 6:30PM, Tuesday, 24 October

Coriandolo Radio: An open-source protocol for “drive-by” sensor-logger data collection

by Craig Goldman

Collecting sensor data from geographically-dispersed, low-powered data loggers is a problem. The loggers can record many kilobytes of data, which must be periodically gathered. Sending “collectors” into the field to connect to each logger one-at-a-time to upload the data is time-consuming, cellular radio requires lots of power and building a mesh radio infrastructure to “route” the data is expensive and often impractical.

We asked the question “would it be possible to gather sensor-logger data while driving by the remote sites without stopping?” Current radio protocol choices were not designed for this scenario. Low-energy radio protocols such as BLE transfer data slowly. Wi-Fi uses a lot of power and may take seconds just to establish the connection.

This talk describes a simple radio protocol, which operates at low power while waiting for a radio connection, yet is able to change modes and transfer bulk data at high rates. The protocol is open-source and available for down-load from GitHub.

Coriandolo Radio Website – info, links, purchase radio module www.coriandoloradio.com

Coriandolo Radio GitHub Site – source code, some documentation www.github.com/cr-craig/Coriandolo-Radio

Craig Goldman is founder and President of CoAutomation Inc., a consulting company specializing in the design of reliable firmware for commercial, industrial and medical products that MUST work correctly. A graduate of MIT, Mr. Goldman has been designing embedded microprocessor products for over 35 years. A recognized innovator, he has made a significant contribution

to dozens of successful designs and has been awarded ten US patents.

PLEASE NOTE: The meeting is open to the public. No charge for Consultants Network members or employees of Constant Contact; \$5 entrance fee for all others. Casual dress. Registration (no registration required).

The Consultants’ Network meeting starts at 6:30 PM. The meeting will take place at Constant Contact, Reservoir Place - 1601 Trapelo Road, Waltham, MA 02451. A no host, PRE-MEETING DINNER will take place at 5:15 PM (sharp) at Bertucci’s, 475 Winter Street, Waltham, MA 02451 (exit 27B, Rte 128).

Driving Directions

To Bertucci’s:

Follow I-95/route 128 to Winter St in Waltham. Take exit 27B from I-95/Route 128. Turn left on Wyman S, then left on Winter St. Bertucci’s is the 1st right after crossing the bridge over I 95/Route128.

To Constant Contact:

Follow I-95/route 128 to Trapelo Rd in North Waltham, Waltham. Take exit 28 from I 95/route 128. Constant Contact is the 1st right after crossing the bridge over I 95/Route128.

Consultants’ Network meetings generally take place on the fourth Tuesday of each month, but are not held during the summer months. Check the Consultants’ Network website for meeting details and last-minute information.

For more information, e-mail or chairman@boston-consult.com

Power and Energy Society – 6:00PM, Tuesday, 24 October

Applications of Synchrophasors Data for Power System Operation and Control

Speaker: Sarma (NDR) Nuthalapati, PhD Principal EMS Network Applications Engineer, PEAK Reliability, Vancouver, WA, USA



Sarma (NDR) Nuthalapati, PhD Principal EMS Network Applications Engineer, PEAK Reliability, Vancouver, WA, USA Date: Tuesday, October 24, 2017 Time: Refreshments - 6pm, Talk - 6:30pm Location: National Grid, 40 Sylvan Road, Waltham, MA 02451 (Rooms: Valley A&B) Abstract: To realize the

vision of the future smart electric grid, advanced technological solutions such as real-time measurements of synchrophasors need to be integrated into the existing power system operation and control practices. Phasor measurement units (PMUs) provide synchronized measurements at high rates for enhanced wide area situational awareness and decision support using new applications.

There have been several large scale implementations of synchrophasor technology in managing the grid across the world. Efforts are in place to take this technology into control room operations and develop good operational procedures to better manage the grid with wide area visualization tools using PMU data. This talk presents some basics of synchrophasors and discusses some use cases of synchrophasors in managing the grid.

Dr. Sarma (NDR) Nuthalapati obtained his B.Tech and M.Tech (Power Systems) degrees from National Institute of Technology, Warangal, in 1983 and 1986 respectively and Ph.D. degree from Indian Institute of

Technology, Delhi in 1995. Since, Feb 2017, he is working at PEAK Reliability as Principal EMS Network Applications Engineer. Prior to joining PEAK Reliability, he had worked for about eight years at ERCOT and was involved in a Synchrophasor Project funded by DOE under the Smart Grid Initiatives Grants.

He is currently the Chair of the IEEE Task Force on Real Time Contingency Analysis. He is also active at the NASPI Working Group meetings and was given NASPI Control Room Solutions Task Team Most Valuable Player (MVP) Award for 'being a leading organizer and contributor to the Control Room Solutions Task Team (CRSTT) and the NERC Synchronized Measurement Subcommittee and a public champion for Synchrophasor Technology'. He is currently working on a book on 'Power System Grid Operations Using Synchrophasor Technology' to be published by Springer. He is a senior member of IEEE and a member of IEEE Power and Energy Society (PES). He is also a distinguished lecture in the IEEE PES Distinguished Lecturer Program (DLP).

Meeting Location: National Grid, 40 Sylvan Road, Waltham, MA 02451 (Rooms: Valley A&B). Time: Refreshments - 6pm, Talk - 6:30pm

Free and Open to the Public - No Registration Required Visit the IEEE PES Boston Chapter website for further details <http://www.ieeepestboston.org/>

If you have any questions, please contact Amsa (781-907-3565) or Subhadarshi (781-907-2483)

Computer Society and GBC/ACM – 7:00PM, Thursday, 26 October

Data Provenance: From Theory to Practice

Margo Seltzer



There seems to be wide spread agreement that data provenance, the history of how a digital artifact came to be in its present state, is important. There also seems to be a great deal of activity in the research community about data provenance: how to collect it, how to represent it, how to store it, and how to query it. Given

this apparent meeting of the minds, why then do we not have seamlessly integrated provenance systems? I'll present a brief, and undoubtedly biased, history of what the research community has been up to in this domain and then talk about the obstacles to wide spread adoption. Finally, I'll wrap up with some suggestions about how we might bring theory and practice closer together in this important domain.

Margo I. Seltzer is Herchel Smith Professor of Computer Science and the Faculty Director for the Center for Research on Computation and Society in Harvard's John A. Paulson School of Engineering and Applied Sciences. Her research interests are in systems, construed quite broadly: systems for capturing and accessing provenance, file systems, databases, transaction processing systems, storage and analysis of graph-structured data, new architectures for parallelizing execution, and systems that apply technology to problems in healthcare.

She is the author of several widely-used software packages including database and transaction libraries and the 4.BSD log-structured file system. Dr. Seltzer was

a founder and CTO of Sleepycat Software, the makers of Berkeley DB, and is now an Architect at Oracle Corporation. She was the USENIX representative to the Computing Research Association Board of Directors and a past President of the USENIX Association. She is a Sloan Foundation Fellow in Computer Science, an ACM Fellow, a Bunting Fellow, and was the recipient of the 1996 Radcliffe Junior Faculty Fellowship. She is recognized as an outstanding teacher and mentor, having received the Phi Beta Kappa teaching award in 1996, the Abrahamson Teaching Award in 1999, and the Capers and Marion McDonald Award for Excellence in Mentoring and Advising in 2010.

Dr. Seltzer received an A.B. degree in Applied Mathematics from Harvard/Radcliffe College in 1983 and a Ph. D. in Computer Science from the University of California, Berkeley, in 1992.

This joint meeting of the Boston Chapter of the IEEE Computer Society and GBC/ACM will be held in MIT Room 32-G449 (the Kiva conference room on the 4th floor of the Stata Center, building 32 on MIT maps). You can see it on this map of the MIT campus.

Up-to-date information about this and other talks is available online at

<http://ewh.ieee.org/r1/boston/computer/>.

You can sign up to receive updated status information about this talk and informational emails about future talks at <http://mailman.mit.edu/mailman/listinfo/ieee-cs>, our self-administered mailing list.

Determining and Communicating Project Value Return on Investment (ROI)

ROI Value Modeling™ for Decision Making

Communicate Right, Reliable, and Responsible REAL ROI Business Cases

Date & Time: Wednesday, December 12; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

Companies are demanding reliable financial measures of proposed projects' value. Yet, project managers often don't know how to identify, calculate, or communicate a project's REAL ROI™ (Return on Investment). Traditional ROI calculations increasingly are being criticized for telling only part of the necessary story. The difficulty afflicts all types of projects but often is greatest in areas like IT, where benefits may seem intangible and frequent overruns impact estimates' credibility. This interactive workshop reveals 22 pitfalls that render common ROI determinations meaningless and shows instead how to identify full-story key effects on revenue and expense variables, reliably quantify tangible and intangible costs and benefits, and convincingly communicate the business value of project investments. Exercises enhance learning by allowing participants to practice applying practical techniques to a real case.

PARTICIPANTS WILL LEARN:

- * The financial information that business decision makers need and demand.
- * ROI and related calculations, strengths, weaknesses, and common pitfalls.

* Using ROI Value Modeling™ and Problem Pyramid™ to fully identify relevant costs and benefits.

* Quantifying intangibles, risk, flexibility, and opportunity.

* Professionally presenting credible business value measurements so people pay attention.

WHO SHOULD ATTEND: This course has been designed for business, systems, and project managers as well as analysts, implementers, users, and others who must know the return on project investments.

OUTLINE

WHAT MONEY HAS TO DO WITH IT

Project Manager role with regard to ROI
 Situations demanding ROI, their issues
 Difficulty of making convincing arguments
 Linking ROI to the business case
 Value Modeling™ Relationship Diagram
 Investment vs. expense
 Justification vs. objective analysis
 Meanings of "It costs too much"
 Total Cost of Ownership (TCO)
 Factors other than cost to be considered

Costs and benefits, revenues vs. expenses
 Return on Investment (ROI) calculations
 Net present value, discounted cash flow
 Payback period, annualized return
 Internal rate of return (IRR), hurdle rate
 'Telling the story' not just ROI calculations
 Failing to quantify 'intangibles' and risk
 Scenario approach to showing benefits
 Mistakenly thinking ROI does not apply

DETERMINING MEANINGFUL BENEFITS

Why it's important to find the benefits first
 Treacy's model of 5 revenue categories
 Problem Pyramid™ to find requirements
 Decision variable clarification chain
 Putting a dollar value on intangibles
 Opportunity, innovation, and flexibility
 Mandates, project with no apparent benefits

ESTIMATING CREDIBLE COSTS

Problem Pyramid™ ties costs to value
 Basing costs on implementation of design
 Business case framework
 Basic formula for estimating costs
 Main causes of poor estimates
 Top-down vs. bottom-up techniques
 Risks that afflict ROI calculations
 Three measurable ways to address risks
 Best-, worst-, most-likely-case scenarios
 Sources of parameter sizing assumptions
 Defining a reasonable scenario for success
 Getting reliable cost and revenue amounts

REPORTING AND MONITORING

Single vs. multiple scenario presentation
 Applying apples vs. apples, when you can't
 Scenario assumptions and parameters
 No change vs. proposed scenarios' ROIs

Measuring intangibles' monetary effects
 Continual, step-wise, and one-time changes
 Percentage-likelihood impact adjustments
 Presenting with spreadsheets
 ROI Value Dashboard™ modeling tool
 Caution about commercial ROI calculators
 Using value modeling to improve decisions
 Dashboard and scorecard-type notification
 Capturing, calibrating with project actuals
 Adjusting appropriately during project

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, *Discovering REAL Business Requirements for Software Project Success*, he regularly works with and trains business and systems professionals.

**Decision (Run/Cancel) Date for this Courses is
 Wednesday, December 6 , 2017**

Payment received by Nov. 29

IEEE Members	\$220
Non-members	\$245

Payment received after Nov. 29

IEEE Members	\$245
Non-members	\$265

<http://ieeeboston.org/determining-communicating-project-value-investment-roi>

Making You a Leader - Fast Track

Become the Leader You Want and Need

Date & Time: Monday, December 11; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

We do projects to make change. Yet, change will not occur without leadership, and leaders are rare. Leaders make others want to do what the leader wants done. Leaders cause ordinary people to achieve extraordinary things. Managing is not the same as leading, and titles do not make leaders. Seminars can teach you to manage, but they cannot teach you to be a leader. Rather, making a leader takes special techniques—such as our personal development clinics—that can change deep-seated behaviors learned over a lifetime.

However, since clinics usually last about ten weeks, this mini-clinic was devised as a more convenient alternative. This format places responsibility upon the participant to carry out an extended informal follow-on program after completion of the formal seminar workshop session.

During the follow-on period, the participant uses time-condensed methods that simulate the lifetime learning which makes a leader. Therefore, commitment to carrying out these exercises is essential for successful transformation.

PARTICIPANTS WILL LEARN:

- Leadership characteristics and practices that are essential for project and personal success.
- Differences between management and leadership, how they conflict, and why leaders are so rare.

- Behaviors leaders use to influence others, up and down, to want to do what the leader wants them to do
- Special techniques personal development clinics use to change lifetime learning and make leaders.
- How to employ those special techniques in a follow-on mini-clinic to develop the leadership skills they need to make their projects successful.

WHO SHOULD ATTEND: This course has been designed for business and systems professionals who want to improve their ability to lead and influence other people.

LEADERSHIP CHARACTERISTICS & ROLE

How leadership looks and feels

Management vs. leadership

Leadership components of project success

Basic leadership practices; power sources

Real change leaders in organizations

TEAMS AND LEADERSHIP

Everyone feels leadership is lacking

Everyone thinks s/he is a leader

Results, not actions or intent

Workgroups, teams, and leaders

Situational leadership styles

Coaching and sports analogies to projects

Hierarchy of needs effects on projects
 Hygiene factors vs. motivators
 Helping project players get their rewards
 Influencing up and down without authority
 Inspiring the extra efforts projects need
 Energizing the project team

SHARED VISIONS

Relating values and vision to projects
 Getting others to embrace one's vision
 Developing a motivating project vision

WHERE AND HOW LEADERS ARE MADE

Born or made? How do we know?
 Habits of thought that affect project success
 Overcoming self-limiting lifetime learning
 Leader's critical success factors
 Traditional education doesn't make leaders
 Special way—personal development clinics

SETTING AND ACCOMPLISHING GOALS

S.M.A.R.T. goals for self and project
 Action plans to achieve your goals
 Visualizing and emotionalizing

DEFINING THE FOLLOW-ON PROGRAM

Clarifying project leadership objectives
 Breaking into prioritized subgoals
 Establishing rewarding daily achievements
 Special techniques to change habits

CARRYING OUT THE MINI-CLINIC

Working with a follow-up support structure
 Mapping results regularly to goals
 Objectively recording leadership changes
 Self-leadership through the process

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, *Discovering REAL Business Requirements for Software Project Success*, he regularly works with and trains business and systems professionals.

**Decision (Run/Cancel) Date for this Courses is
 Monday, December 4, 2017**

Payment received by Nov. 27

IEEE Members	\$220
Non-members	\$245

Payment received after Nov. 27

IEEE Members	\$245
Non-members	\$265

<http://ieeeboston.org/making-leader-fast-track-become-leader-want-need/>



Join the Elite | IEEE Global Engineers

Join/Renew



2017 IEEE WIE USA EAST FORUM Call for Participation

November 30 – December 2, 2017 Baltimore, MD



Presentation Topics

- Mentoring the next generation of female leaders
- Strategies for increasing equity in power and decision making
- Women as leaders in education, industry, and government
- Development: communication skills in written and spoken word, effective dialog
- Cross-cultural aspects of leadership
- What it takes to be a great leader - qualities that all successful leaders share
- Shaping the future by female leaders
- Training vs inherent skills: can leadership be learned?
- Work-Life balance: family systems traditions and changes
- Leadership development for women: overcoming stereotypes
- The design, implementation, and evaluation of leadership from a structural perspective
- Helping girls and young women become leaders - motivating to empower, empowering to motivate
- Exploring the attrition gap - why do women leave the engineering field and what can be done to prevent it

Not a WIE member?

Our active community of female and male engineers is involved in career building, networking, and community outreach.

Join Now

Submission Deadline

Presentation topic abstract suitable for program (up to 150 words), and extended abstract for evaluation (up to 2 pages) due 24 July 2017.

For more information, visit:

<http://sites.ieee.org/wie-forum-usa-east/calls-for-participation/>



Registration is Now Open!!!



New Submission Deadlines

Paper: July 31st, 2017

Poster and Lightning Talk: September 3rd, 2017

To submit: <https://ieee-r1-studentconference.myreviewroom.com>

Envisioning a technical conference targeted towards undergraduate students all over the globe, the MIT IEEE Student Branch in 2015 inaugurated the IEEE MIT Undergraduate Research Technology Conference. This year we are organizing it again with the goal to make the conference a venue where undergraduate students can meet to present, discuss, and develop solutions advancing technology for humanity. Participants can attend a rich program with renowned speakers, technical sessions, a student design competition, exhibits, networking, and social activities, presenting a great opportunity for students to interact with leading industry experts.

The conference theme is “Meet Innovative Technology”, and the six fields of focus are:

1. Machine Learning / Artificial Intelligence (AI)
2. Biological and Biomedical Engineering and Technology (BioEECS)
3. Robotics and Automation Technology
4. Systems and Networking
5. Embedded Technologies
6. Innovative Technologies and Others

Authors may submit content in the form of a technical paper, poster, or lightning talk.

All submissions must be written in English. Paper submissions must be no longer than 4 pages, single-spaced, with a minimum font of 10 point, and submissions may include figures, illustrations, and graphs. Abstract submissions for the poster and lightning talk are limited to 500 words.

- New notification of paper acceptance by August 27, 2017.
- New notification of poster and lightning talk acceptance by September 24, 2017.
- Those who have made their submissions by the original deadline of June 30, 2017 will still receive the notification of acceptance by August 4, 2017.

Please join the mailing list (MIT-Conference@ieee.org) for more information and updates on submission, the technical program, registration, and accommodation.

A conference proceeding of all the accepted papers that have been presented at the conference may be published and included in the IEEE Xplore journal. Electronic and online media containing all accepted submissions will be distributed to all registered attendees.

Meet Innovative Technology

Sponsored by MIT IEEE Student Branch and IEEE Boston Section

<http://ieee.scripts.mit.edu/conference>

Last Notice Before Course Begins, Please Register Now!!!

Digital Signal Processing (DSP) for Wireless Communications - Under the Hood

Time and Dates: 6 - 9PM, Wednesdays, October 18, 24, November 1, 8, 14
(Note: Oct. 24 and Nov. 14 are Tuesdays) This is a date change!

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Dan Boschen, Microsemi

Course Summary:

This course is a fresh view of the fundamental concepts of digital signal processing most applicable to practical real world problems and applications in radio communication systems. This course will build an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real world applications in GPS and mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges in both the analog and digital domains, and not a tutorial on working with specific DSP processor hardware.

Target Audience:

All engineers involved in or interested in signal processing applications. Engineers with significant experience with DSP will also appreciate this opportunity for an in depth review of the fundamental DSP concepts from a different perspective than that given in a traditional introductory DSP course.

Benefits of Attending/ Goals of Course:

Attendees will build a stronger intuitive understanding of the fundamental signal processing concepts involved with digital filtering and mixed signal communications system design. With this, attendees will be able to implement more creative and efficient signal processing architectures in both the analog and digital domains

Topics / Schedule:

Class 1:

Correlation
Fourier Transform
Laplace Transform

Class 2:

Sampling and A/D Conversion
Z –transform
D/A Conversion

Class 3:

IIR and FIR Digital filters
Direct Fourier Transform

Class 4:

Windowing, Digital Filter Design
Fixed Point vs Floating Point

Class 5:

Fast Fourier Transform
Multirate Signal Processing
Multi-rate Filters

Speaker's Bio:

Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 20 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave de

signing and developing transceiver hardware from baseband to antenna for wireless communications systems. Dan is currently at Microsemi (formerly Symmetricon) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page at: <http://www.linkedin.com/in/danboschen>

**Decision (Run/Cancel) Date for this Course is
Monday, October 9, 2017**

Payment received by October 6

IEEE Members \$325

Non-members \$360

Payment received after October 6

IEEE Members \$360

Non-members \$425

<http://ieeeboston.org/digital-signal-processing-dsp-course-fall-2017>

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically diverse sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is

<http://ieeeboston.org/course-proposals/>

Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course)
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Embedded Linux Optimization - Tools and Techniques (*Online Edition*)

**New
Online
Course**

Students have access to this self-paced course for 90 days!!

Registration fee: \$250

Summary - This video course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand debugging, profiling and testing high performance Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.

- To give students the confidence to apply these concepts to their next Embedded Linux project.

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

Getting Started with Embedded Linux

Embedded Linux Training Overview

Terminology

Linux Versioning

The GPL

Building the Kernel Source Code

Embedded Linux Kernels

BSPs and SDKs

Linux References (Books and Online)

A Development Cycle Focused on Performance

A Basic Optimization Process

Basic Debugging Review

Embedded Applications Debug

GDB, GDB Server and the GDB Server Debugger

Other Debuggers

An Eclipse Remote Debug Example

Debugging with printk, syslog, syslogd and LTTng

System-Level Debug

System-Level Debug Tools

The /proc and /sys Filesystems

Basic Logging	New Tracing Methods
KDB and KGDB	SystemTap
Crash Dumps and Post-Mortem Debugging	Ftrace, Tracepoints and Event Tracing
Debugging Embedded Linux Systems	Tracehooks and utrace
Backend Debuggers	Profiling
In-Circuit Emulators	Basic Profiling
Hardware Simulators	gprof and Oprofile
Analyzers	Performance Counters
Requirements Development	LTTng
Performance Requirements	Another DDD Example
Derived Requirements	Manual Profiling
Testability and Traceability	Instrumenting Code
Reviewing Requirements	Output Profiling
Designing for Performance	Timestamping
Design for Test (DFT)	Addressing Performance Problems
Agile Software Design	Types of Performance Problems
Software and Linux Decomposition	Using Performance Tools to Find Areas for
Memory Management	Improvement
CPU and OS Partitioning	Application and System Optimization
Design Reviews	CPU Usage Optimization
Coding for Performance	Memory Usage Optimization
Coding Standards and Consistency	Disk I/O and Filesystem Usage Optimization
Languages, Libraries and Open Source Components	Measuring Embedded Linux Performance
Learning Magic Numbers	Some Ideas on Performance Measurement
Letting Compilers Work For You	Common Considerations
Global, Static and Local Variables	Uncommon Considerations
Code Reviews	Using JTAG Methods
	BootLoader Measurements
Software Testing	Boot Time Measurements
Unit-Level Testing	The Perf Tool
System-Level Testing	Origins of Perf
Code Coverage Tools	The Perf Framework
gcov	Perf Commands and Using Perf
Automated Testing	Listing Events
Some Embedded Linux Test Recommendations	Counting Events
DebugFS	Profiling with Perf
Configuring DebugFS	Static Tracing with Perf
DebugFS Capabilities	Dynamic Tracing with Perf
Advanced Logging	Perf Reporting
LogFS	Performance Tool Assistance
Using Logwatch and Swatch	Recording Commands and Performance
Using syslogd and syslog-ng	System Error Messages and Event Logging
Tracing	Dynamic Probes
ptrace and strace	Jprobes and Return Probes
	Kernel Probes

Kexec and Kdump	Improving System Memory Performance
Improving Boot Performance	Memory Performance Statistics
Boot Time Optimization	Linux Performance Tools for Memory
The Linux Fastboot Capability	Process-Specific Memory Performance Tools
Building a Smaller Linux	More Stupid Cache Tricks
Building a Smaller Application	Improving I/O and Device Driver Performance
Filesystem Tips and Tricks	Disk, Flash and General File I/O
Some Notes on Library Usage	Improving Overall Performance Using the Compiler
Improving Kernel Performance	Basic Compiler Optimizations
Kernel Hacking	Architecture-Dependent and Independent Optimization
CONFIG_EMBEDDED	Code Modification Optimizations
Configuring printk	Feedback Based Optimization
Test Code	Application Resource Optimization
Configuring Kernel and IO Scheduling	The Hazard of Trust
	An Iterative Process for Optimization
Improving CPU Performance	Improving Development Efficiency
Run Queue Statistics	The Future of Linux Performance Tools
Context Switches and Interrupts	Some Final Recommendations
CPU Utilization	
Linux Performance Tools for CPU	
Process-Specific CPU Performance Tools	
Stupid Cache Tricks	

<http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/>

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Software Development for Medical Device Manufacturers (Online Edition)

**New
Online
Course**

Students have access to this self-paced course for 90 days!! Registration Fee : \$125

Course Description This course provides an introduction to the development of medical device software. The course is comprised of 4 modules that range from 30-45 minutes in duration. The focus is on complying with FDA Design Controls and IEC 62304 requirements.

This course is intended for software developers who are actively involved in developing medical device software.

Module 1

- Medical Device Definitions: FDA and European Union (EU)
- Regulatory Roadmap
- FDA/EU Device Classifications
- FDA QSR Regulation
- FDA Guidance Documents that pertain to medical device software

Module 2

- International Standards that pertain to medical device software
- Types of Software Regulated by FDA
- Quality System basics: Procedures, Work Instructions and Records
- ALL Software is Defective...

Module 3:

- Design Control Overview
- General Requirements
- Design and Development Planning
- Software Development Models
- Design Input
- About Requirements...
- Design Output

- Design Reviews

Module 4:

- Design Control (continued)
- Design Verification
- Software Verification Process
- Testing Overview
- Design Validation
- Software Validation Process
- Design Changes
- Design Transfer
- Design History File
- Course Summary

Speaker Bio:

Steven R. Rakitin has over 40 years experience as a software engineer including 25 years of experience in the medical device industry. He has worked with over 85 medical device manufacturers worldwide, from startups to Fortune 100 corporations. He has written several papers on medical device software risk management as well as a book titled: *Software Verification & Validation for Practitioners and Managers*.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE and a member of MassMEDIC. He is on the Editorial Review Board for the ASQ Journal Software Quality Professional.

As President of Software Quality Consulting Inc., he helps medical device companies comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

<http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/>

Fundamental Mathematics Concepts Relating to Electromagnetics (*Online Edition*)



**New
Online
Course**

Students have access to this self-paced course for 90 days!!

Registration Fee: 150

Course Summary This course is designed for people wishing to refresh or to learn the fundamental mathematical concepts that are used to describe electromagnetic wave behavior. The modules address all of the basic math concepts covered in a traditional undergraduate electromagnetics course in an ECE curriculum. These concepts include Vector Basics, Integral Vector Calculus, Differential Vector Calculus, Fundamental Coordinate Systems and Complex Numbers. After completing these modules, a person should have sufficient math skills to pursue graduate studies in electromagnetics and/or be able to decipher the math presented in an upper-level text on the subject.

Target audience: This course is designed for people wishing to refresh or to learn the fundamental mathematical concepts that are used to describe electromagnetic wave behavior.

Course chapters

1. Vector Basics
2. Dot Product

3. Cross Product
4. Contour Integration
5. Vector Algebra
6. Surface Integration
7. Metric Coefficients
8. Coordinate Systems
9. Vector Coordinate Conversion
10. Del Operator and the Gradient
11. The Curl
12. Divergence
13. Stokes Theorem
14. Divergence Theorem
15. Laplacian
16. Complex Numbers

Instructor's Bio:

Dr. Kent Chamberlin is the Chair and a Professor in the Department of Electrical and Computer Engineering. In his more than thirty-five years in academia, he has performed research for more than twenty sponsors, including the National Science Foundation. He has received two Fulbright awards, including the prestigious Fulbright Distinguished Chair, which he served in Aveiro, Portugal. He has also served as an Associate Editor for the Institute for Electrical and Electronics Engineers, and he continues to be active in performing and publishing in a range of research areas.

<http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/>

Reliability Engineering for the Business World *(Online Edition)*



Students have access to this self-paced course for 90 days!!

Registration Fee: 320

Course Description

This course is about becoming a leader in reliability engineering. While statistics are the tools of reliability engineering, it takes knowledge not only of these tools but also of the business. Developing knowledge of the business, from sales, engineering, customer service, to supply chain management can determine how effective you can be in improving reliability.

Never take anything for granted, even some rules of thumb in reliability can be misleading, this course will show you how to prove what truly happens in the real world and how to effect change in any part of the business where it is needed. We will explore the balance sheet, organizational structure, customers, service, and high volume manufacturing. It's not just about how often things fail, it is also about where the defect came from, what is the financial effect, the recovery, when should a business take field action, effect of human error, failure analysis/material science, reliability testing, and much more. I will also discuss how you develop executive buy in for change. The course assumes a basic knowledge in reliability statistics. There are 12 sessions that cover the following topics.

Course Outline

Basics – Measurements
Business Model
Design Model (HW and SW)

HALT/RDT/Predictions
Manufacturing Model
Early Life Failures
Wear Out and Mid Life Crisis
Advanced Reliability

Course Objective

To teach you how to become the go to person in your business for objective business sensed reliability answers and requirements.

Instructor's Bio

Kevin is an innovative leader in reliability methodologies with more than 30 years experience in the storage industry. In his latest role as Director of Engineering, he developed a top down reliability/availability management process for design organizations developing mission-critical storage systems. Kevin previously directed the most extensive HALT/HASS operation in the industry, with over 300 chambers worldwide. He has written several papers, consulted with many companies, 3 patents awarded and 2 pending related to systems reliability and test.

His most recent work has been performing system architectural analysis to optimize system availability, serviceability and costs. Providing guidance to development to maximize system reliability and reduce service costs. He has provided consultation to many large companies such as EMC, CISCO, AT+T, HP, Seagate and many others. His position and experience has enabled him to perform extensive field studies and design of experiments. Kevin has developed many

<http://ieeeboston.org/reliability-engineering-business-world-line-course/>

Introduction to Embedded Linux

(Online Edition)



**New
Online
Course**

Students have access to this self-paced course for 90 days!! Registration Fee: 350

Course Summary:

This first of a 2-part series introduces the Linux Operating System and the use of Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part covers the methods for booting Embedded Linux distributions including embedded cross-development and target board considerations.

Who Should Attend:

The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives:

To provide a basic understanding of the Linux OS and the Eclipse IDE framework.

To gain an understanding of the complexities of Embedded Linux Distributions and their use in embedded systems.

To give students confidence to apply these concepts to their next Embedded Linux project

Hardware and Software Requirements

The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ instal-

lation or prior knowledge of C-based Makefiles is useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials

Linux Kernel Development by Robert Love
Linux System Programming by Robert Love
Linux Debugging and Performance Tuning by Steve Best
Optimizing Linux Performance by Phillip G. Ezolt
Embedded Linux Primer by Christopher Hallinan
Pro Linux Embedded Systems by Gene Sally
Embedded Linux Development Using Eclipse by Doug Abbott
Linux Device Drivers by Jonathan Corbet et al
Essential Linux Device Drivers by Sreekrishnan Venkateswaran

Course Downloadable Content:

Video Lecture
Hands-On Lab Instructions
Hands-On Lab Solutions
Additional Related Materials

The Basics

Linux Terminology, History and Versioning
The Linux Community: Desktop & Embedded
The GPL
Linux References (Books and Online)

Getting Started

Kernel Source Code
Building the Kernel
Embedded Linux Kernels
Linux 2.6

Basic Kernel Capabilities

Process and Threads Management
Signals and System Calls

Synchronization, IPC and Error Handling
Timing and Timers
Memory Management and Paging
The I/O Subsystem: A Tale of Two Models
Modularization

Debugging

Process-Level and System-Level Debug
GDB and KGDB
GDB Server and Remote Debugging

An Eclipse Debug Example

Other Debug and Test Tools

Other System-Level Debug Approaches

Process & Threads Management

What are Processes and Threads?
Virtual Memory Mapping
Creating and Managing Processes and Threads
Thread-Specific Data (TSD) POSIX
The Native POSIX Threading Library (NPTL)
Kernel Threads

Signals

System Calls

Scheduling

Linux 2.4 and 2.6 Scheduling Models
The O(1) Scheduler
The Completely Fair Scheduler (CFS)

Synchronization

Via Global Data
Via Semaphores, Files and Signals

Inter-Process Communications (IPC)

Message Queues
Semaphores Revisited
Shared Memory
Pipes, FIFOs and Futexes
Remote Procedure Calls
Networking

Error Handling

errno and perror
strerror and strerror_r
oops, panics and Segmentation Faults

Timing

How Linux Tells Time
Kernel, POSIX and Interval Timers
High-Resolution Timers (HRTs)

Memory Management and Paging

Demand Paging and Virtual Memory
Allocating User and Kernel Memory
Mapping Device Memory
The Slab Allocator
The OOM Killer
Memory in Embedded Systems

Modularization

Creating a Module and Module Loading
Dependency Issues
In Embedded Systems

Shared Libraries

A Shared Library Example
Static and Dynamic Libraries

The I/O Subsystem: A Tale of Two Models

The Original Device Driver Model
The Standard I/O Interface
The New Device Driver Model and Kernel Object
Classes
Initialization
Platform Devices, Busses, Adapters and Drivers
Comparing the Two Models

Embedded Linux Trends

Development, Monitoring and Testing

Some Final Recommendations

Lecturer:

Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at Tlera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based development tools, training and consulting for the embedded systems market.

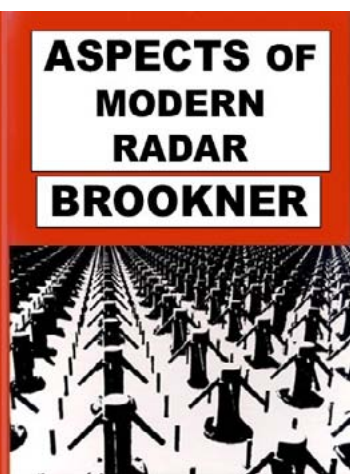
Last Notice Before Course Begins, Please Register Now!!!

Radar Basics and Amazing Recent Advances

Date & Time: 6 – 9PM, Mondays, Nov. 6, 13, 20, Dec. 4, Jan. 8, 22, 29, Feb. 5
(If needed snow/makeup days Feb. 12, 26)

Location: Location: MITRE Corporation, 202 Burlington Rd., Bedford, MA
(Rt 3, Exit 26 , 2.3 mi from Rt 128/95)

Speaker: Dr. Eli Brookner, Raytheon Company (Retired)



The following book plus over 15 paper reprints are provided FREE with your registration:

1. "Aspects of Modern Radar", Dr. Eli Brookner (Editor), Artech House, Hardcover, 432 pages, 1988, List price: \$159. The 1st chapter gives the best easy to read introduction to radar. It covers all aspects of radar: transmitters, receiver, antennas, signal processing, tracking, clutter derivation of radar equation in easy terms and definition of dB. The 2nd chapter gives detailed descriptions of different radar systems like: Cobra Dane, Pave Paws, BMEWS, Series 320 3D radar, OTH radars and dome antenna. The book has a catalog giving the detailed parameters for over 200 radars from around the world. The remaining chapters cover AEGIS SPY-1, Hybrid and MMIC circuits, ultra low sidelobe antennas (ULSA), mmw, radar cross section and Doppler weather radars. The material in the book is easy to access and as a result the text serves as a handy reference book.

All Attendees of the class will receive a trial license of MATLAB, Phased Array System Toolbox, and Antenna Toolbox from MathWorks in addition to a set of examples which help demonstrate the key radar concepts covered in the course material. MathWorks will also give a radar demonstration.

This course is an updated version of the Radar Technology course given previously. Those who have taken the Radar Technology previously should find it worthwhile taking this revised version. New material includes latest on solid state devices and transmitters including GaN, SiC, SiGe; Breakthroughs in Radar — \$10 T/R module, Digital Beam Forming (DBF), Packaging, Disruptive Technology, Metamaterials, radar on a chip, 256 element phased array on a chip, Memristors, Graphene. Also covered are radar height-range coverage diagram using the powerful SPAWAR's AREPS program. AREPS

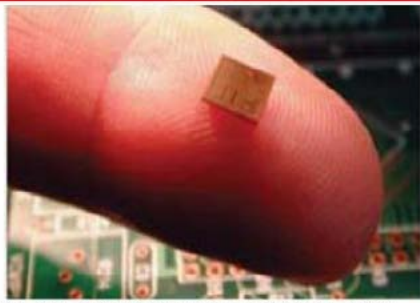
provides coverage for arbitrary propagation conditions (ducts [evaporation, surface, or elevated], subrefraction and superrefraction) and terrain conditions based on DTED map data. AREPS now accounts for surface roughness scattering and evaluates sea and land clutter backscatter versus range. Attendees will be told how to obtain AREPS FREE. Valued at over \$7,000. Also new is coverage of Anomalous Propagation and what to do about it. Finally also covered is the new Multiple-Input Multiple-Output (MIMO) explained in simple physical terms.

Updated course is framed around FREE book described above. Also given out free are supplementary notes consisting of copies of >800 slides plus over 15 paper reprints by Dr. Brookner.

For the beginner, basics such as the radar equation,

MTI (Moving Target Indicator), pulse doppler processing, antenna-scanning techniques, pulse compression, CFAR, RAC and SAW devices, dome antenna, CCDs, BBDs, SAW, SAW monolithic convolvers, microstrip antennas, ultra-low antenna sidelobes (<-40 dB), stacked beam and phased array systems, (1-D, 2-D, Limited Field of View [LFOV]), Moving Target Detection (MTD) are all explained in simple terms. For both the novice and experienced covered are tracking, prediction and smoothing in simple terms (mystery taken out of GH, GHK and Kalman filters); the latest developments and future trend in solid state, tube and digital processing technologies; synthetic aperture radar (SAR); Displaced Phase Center Antenna (DPCA); Space-Time Adaptive Processing (STAP); digital beam forming (DBF); Adaptive-Adaptive Array Processing for jammer suppression with orders of magnitude reduction in computation; RECENT AMAZING RADAR BREAKTHROUGHS

SINGLE CHIP 77GHz RADAR



(G. KLARI, ET AL., "SINGLE CHIP MM RADAR", MICROWAVE J., 1-14-15;
R. J. Evans et al., "Consumer Radar," *Int. Radar Conf.*, Adelaide, 9/2013, pp. 21-26)

and Far Field Defined, Phased Steering, Subarraying, Array Weighting, Monopulse, COBRA DANE slide tour (10 story building).

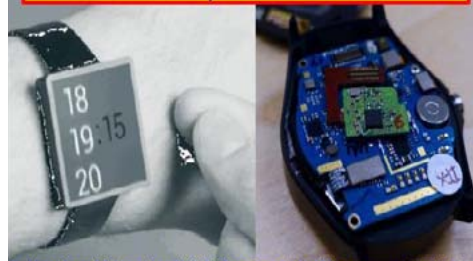
FUNDAMENTALS OF Radar: Radar equation derived. FREQUENCY TRADEOFFS: Search vs Track, Range and Doppler Ambiguities, Detection in Clutter. Blind Velocity region, range eclipsing, Environmental Factors, Dependence of clutter model on grazing angle and size radar resolution cell discussed, Weibull clutter, Polarization Choice.

Lecture 2, Nov. 13

FUNDAMENTALS of Radar: Part 2: Antenna Pattern Lobing in Elevation due to multipath, Detection of Low Flying Low Cross-Section targets, Ground Multipath Elevation Angle Error Problem and ways to cope with it, e.g., use of an even difference pattern Off-Axis Monopulse,

GOOGLE RADAR IN SMART WRIST WATCH

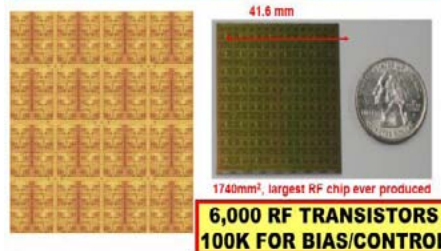
**FITS ON PINKY TOE NAIL
4 ANTENNAS; 0.05W DC POWER**



<http://spendergast.blogspot.com/2016/05/googles-project-soli-demos-mmwave-micro.html>
<http://www.theverge.com/2016/5/20/11720876/google-soli-smart-watch-radar-atap-io-2016>

surface-based ducts, evaporation ducts. Determination of radar coverage using new AREPS program. ANTENNA SCANNING SYSTEMS: Fixed Beam System: Wake Measurement Radar; 2-D Radars, 3-D Radars: Stacked Beam: Marconi Martello, Smart-L, SMART-ELLO, ARSR-4; 1-D Frequency Scanning: ITT Series 320; 1-D Phased Scanning: TPS-59, GE-592, RAT-31DL; Phased-Frequency Scanners: Raytheon Fire Finder and Plessey AR320.

256 (16X16) - ELEMENT SINGLE CHIP 60 GHZ TX/RX PHASED ARRAY



**6,000 RF TRANSISTORS
100K FOR BIAS/CONTROL**

S. ZINIR & G. M. REBEIZ, IEEE IMS, MAY, 2016

IEEE WSC: Millimeter-wave Systems

Lecture 3, Nov. 20

FUNDAMENTALS of Radar: Part 4: ULTRA LOW ANTENNA SIDELOBES (40 dB down or more). MOVING TARGET INDICATOR (MTI): Two-Pulse Cancellor, Pulse Doppler Process-

ing; MOVING TARGET DETECTOR (MTD); Optimum Clutter Cancellor, Space-Time Adaptive Processing (STAP), Airborne MTI (AMTI), Displaced Phase Center Antenna (DPCA).

Lecture 4, Dec. 4

SIGNAL PROCESSING: Part 1: What is PULSE COMPRESSION? Matched Filters; Chirp Waveform Defined; ANALOG PROCESSING: Surface Acoustic Wave (SAW) Devices: Reflective Array Compressor (RAC), Delay Lines, Bandpass Filters, Oscillators, Resonators;

Complex Monopulse, Two Frequency Radar Systems: Marconi L- and S-band S631, Signaal/Thales

(Holland), Flycatcher X and Ka System; Tube and Solid State OTH. PROPAGATION: standard, superrefraction, subrefraction,

**USING TUBES \$35 STICK WOULD:**

- COST \$130B (\$1/TUBE)
- REQUIRE 130 GW (1W/TUBE) OR 130 NUCLEAR POWER PLANTS
- WOULD STACK TO 9X DISTANCE TO THE MOON

ECHODYNE RADARS USING METAMATERIAL ARRAYS

MESA-D-DEV K-BAND RADAR: FACILITY/BORDER PROTECTION

RANGE >500M FOR MAN TARGET
± 60° AZ, ± 40° EL

MESA-DAA K-BAND RADAR: UAV DETECTION &

RANGE 3KM
± 60° AZ, ± 40° EL

(ECHODYNE WEB PAGE)

STEALTH DEFEATING QUANTUM RADAR

- MAKES USE OF QUANTUM ENTANGLEMENT
- DETECTION OF SINGLE PHOTON
- CAN BE USED TO DETECT CANCER CELLS
- ELECTRONICS TECHNOLOGY GROUP CORPORATION (CETC) OF CHINA
- TECHNOLOGY USED IN CHINA QUANTUM SATELLITE



HTTPS://WWW.RT.COM/NEWS/358664-CHINA-QUANTUM-RADAR-TEST/

IMCON Devices; Analog Programmable Monolithic SAW Convolver; BBD/CCD. What are they?

Lecture 5, Jan. 8

SIGNAL PROCESSING: Part 2: DIGITAL PROCESSING: Fast Fourier Transform (FFT); Butterfly, Pipeline and In-Place Computation

explained in simple terms; Maximum Entropy Method (MEM) Spectral Estimate; State-of-the-art of A/Ds, FPGAs and Memory; Signal Processor Architectures: Pipeline FFT, Distributed, Systolic; Digital Beam Forming (DBF). Future Trends.

Lecture 6, Jan. 22

SYNTHETIC APERTURE RADAR (SAR): Strip and Spotlight SAR explained in simple terms.

TUBES: Basics given of Magnetron, Cross Field Amplifiers, Klystrons, Traveling Wave Tubes, Gyro Tubes.

TREND TOWARD SOLID STATE PHASED-ARRAY TRANSMITTERS: Discrete All Solid State PAVE PAWS and BMEWS radars; advantages

over tube radars; MMIC (Monolithic Microwave Integrated Circuitry; integrated circuitry applied to microwave components): THAAD, SPY-3, IRIDIUM, XBR, JLENS. Solid State 'Bottle' Transmitters: ASR -11/ DARS, ASR-23SS, ASDE-X. Extreme MMIC.

Breakthroughs and Trends in Radar and Phased-Arrays: Radar on a chip, 258 element phased array on a chip, new revolutionary metamaterial for electronically scanned arrays and target stealthing, Moore's Law marches forward, quantum anti-stealth radar, you have heard of orthogonal H and V polarization which can double channel data rate, there are an infinite other polarizations called orbital angular momentum (OAM).

SS* AIR TRAFFIC CONTROL RADARS

*SS=SOLID STATE
**J. WANG,
E. BROOKNER,
RAYTHEON US PATENT
2009/0096662 A1

**Lecture 7, Jan. 29**

TRACKING, PRE-DICTION AND SMOOTHING: $\alpha\beta\gamma$ (GHK) Filter; Kalman Filter. All explained in simple physical terms.

Lecture 8, Feb. 5

HOW TO LOOK LIKE A GENIUS IN DE-

TECTION WITHOUT REALLY TRYING: Simple procedure for determining detection. Covered are beam shape, CFAR, mismatch losses.

The Following is Included in Your Registration:

	Value
Textbook	\$159
15 Reprints	\$300
Over 800 Vugraphs	\$120

Decision (Run/Cancel) Date for this Course is Friday, October 27, 2017

Payment received by October 24

IEEE Members	\$300
Non-members	\$340

Payment received after October 24

IEEE Members	\$340
Non-members	\$370

Last Notice Before Course Begins, Please Register Now!!!)

Modern Wireless System Design: From Circuit to Web-based Apps.

Date & Time: 9AM - 4:30PM, Thursday & Friday, October 26 & 27**Location:** Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA**Speaker:** Henry Lau Lexiwave Technologies**Overview:**

Nowadays, as the features of wireless communication products and systems are getting more in number and sophisticated to stay competitive, the products have to contain both hardware and software. It is thus beneficial for an engineer or manager to acquire a broad understanding on how a modern wireless communication product or system works with both hardware and software components. This course is aimed to provide an opportunity for participants to acquire technical insights on the vital aspects of Modern Wireless System Design from an industry and practical perspective. It is an introductory level for circuit, software, system engineers and managers who would like to acquire an overview on the vital aspect and design considerations on complete wireless system design. Various functional blocks of wireless systems and products will be discussed and analyzed with practical examples on commercial products. The software development will also be addressed to provide a comprehensive understanding of the development of complete wireless systems. The course will be conducted by a wireless design expert with rich industrial experience. Interactive and open discussions between speaker and participants are encouraged and facilitated to make the whole course more interesting and thought stimulating.

Audience:

System engineers, wireless product designers, software engineers, RF and microwave circuit design engineers, field application engineers, business development engineers and managers involved in wireless products and systems.

Benefits:

Upon completion of this course, participants should be able to:

1. understand the key functional blocks of Modern Wireless Products/Systems and their characteristics and specifications
2. understand how the key component blocks interact and the implications on overall system performance
3. compare and evaluate different types of receiver and transmitter architectures
4. comprehensive understanding on the embedded software development as well as web-based and app-based software development
5. acquire practical design techniques from case studies on commercial wireless products

Course Content:**Receiver**

System Characteristics

Signal and Noise

Noise temperature, noise bandwidth, noise figure, sensitivity

Linearity

Dynamic Range, one dB compression point, intermodulation

Critical Circuit blocks

LNA, local oscillator, mixer, IF amplifier, demodulator, baseband amplifier

System Architectures and design considerations

Heterodyne, Direct Conversion, Image-reject and Low-IF Receiver

Sample Receiver Designs

Transmitter

Circuit blocks: oscillator, modulator, buffer amplifier, frequency multiplier, power amplifier, output filter

Major issues: power gain, power efficiency, harmonic prevention and suppression

Wireless Modules

Types: GPS, Bluetooth, GSM/GPRS, Wifi
Applications
Electrical parameters

Miniature Antennas for Portable electronics

Antenna Fundamentals
Radiation mechanism
Source of radiation
Characteristic of radiation
Parameters and specifications
Radiation pattern, antenna efficiency, aperture concept, directivity and gain
Types of antenna and performance
Dipole
Monopole
Loop
miniature antennas – patch, inverted-L, inverted-F, meandered line
Practical design considerations and techniques for portable electronics

Software Development

Embedded device
Type of MCU
Characteristics, functions and features
Design considerations
Web database development
MySQL
Website development
Software - HTML, Javascript and PHP
Web server

Smartphone Apps Development
Android development tool
Phonegap
IOS

Expertise:

Henry Lau received his M.Sc. and MBA degrees from UK and USA respectively. He has more than 25 years of experience in designing wireless systems, products and RFICs in both Hong Kong and US. He worked for Motorola and Conexant in US as Principal Engineer on developing RFICs for cellular phone and silicon tuner applications. Mr Lau holds five patents and has one patent pending, all in RF designs. He is currently running Lexiwave Technology, a wireless company in Hong Kong and US designing and selling RFICs, RF modules and wireless solutions. He has also been teaching numerous RF-related courses internationally.

Decision (Run/Cancel) Date for this Course is Tuesday, October 17, 2017

Payment received by October 13

IEEE Members	\$405
Non-members	\$435

Payment received after October 13

IEEE Members	\$435
Non-members	\$455

***notes, lunch and coffee breaks
included with registration***

<http://ieeeboston.org/modern-wireless-system-design-circuit-web-based-apps-fall-2017>

IEEE Boston Section Social Media Links:

Twitter: <https://twitter.com/ieeeboston>

Facebook: <https://www.facebook.com/IEEEBoston>

YouTube: <https://www.youtube.com/user/IEEEBostonSection>

Google+: <https://plus.google.com/107894868975229024384/>

LinkedIn: <https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about>

Practical RF PCB Design: Wireless Networks, Products and Telecommunications

Date & Time: Thursday & Friday, December 14 & 15; 9AM - 4:30PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Henry Lau, Lexiwave Technology

Overview: One of the most demanding consumer products in the market is the wireless telecommunication product. A well-designed Radio Frequency Printed Circuit Board (RF PCB) contributes significantly to the success of any wireless product as the layout of the PCB greatly affects the performance, stability and reliability of the product. In today's highly competitive wireless products market with increasingly compressed development time-frame, there is a strong demand for RF professionals who possess the knowledge and experience to design top-performing RF PCBs in less number of iterations. What matters is whether your level of competence is up to the required standard to meet such demand.

Audience: RF Designers, Wireless Product Designers, Field Application Engineers, Design Managers and related professionals.

Benefits: This course aims to provide participants with an insightful training on RF PCB design from a practical, industrial perspective. Participants will be led through a systematic, theoretical presentation with case studies on commercial products in the training. The course will be conducted by an RF expert with rich industrial experience. It is suitable for RF professionals who want to keep up-to-date their skills and knowledge in RF PCB design and stay competitive.

OUTLINE

1. Printed circuit board design for RF circuits

From product design, circuit design to PCB design
Layer stack-up assignment
Grounding methods and techniques
Interconnects and I/O
Bypassing and decoupling
Partitioning methods

2. Printed circuits board design for other circuits

Clock circuits
Base-band circuits
Audio circuits
Power supplies
Impedance-controlled circuits

3. PCB design for EMC/EMI compliance

EMC/EMI compliance
Grounding methods
Decoupling methods
Shielding methods

4. Additional Design Techniques

Production concerns
Systematic product design approach
RF Modules
Evaluation boards
Other RF concerns
Casing design

5. Case studies

Expertise:

Henry Lau received his M.Sc. and MBA degrees from UK and USA respectively. He has more than 25 years of experience in designing RF systems, products and RFICs in both Hong Kong and US. He worked for Motorola and Conexant in US as Principal Engineer on developing RFICs for cellular phone and silicon tuner applications. Mr Lau holds five patents all in RF designs. He is currently running Lexiwave Technology, a fables semiconductor company in Hong Kong and US designing and selling RFICs, RF modules and RF solutions. He has also been teaching numerous RF-related courses internationally.

*notes, lunch and coffee breaks
included with registration*

**Decision (Run/Cancel) Date for this Courses is
Monday, December 4, 2017**

Payment received by November 29

IEEE Members \$405

Non-members \$435

Payment received after November 29

IEEE Members \$435

Non-members \$455

<http://ieeeboston.org/practical-rf-pcb-design-wireless-networks-products-telecommunications-fall-2017>

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is

<http://ieeeboston.org/course-proposals/>

Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course)
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Last Notice Before Course Begins, Please Register Now!!!

Patenting Outside of the U.S.

Date & Time: 6 – 9PM, Monday, October 23**Location:** Tufts University, Halligan Hall, Room 127., 161 College Ave, Medford, MA**Speaker:** Christine Kuta, Kuta Intellectual Property Law, LLC

Course Overview: Most countries in the world have a patent office where one can apply for protection of inventive ideas. There is, however, no global patent that provides rights everywhere. Operating in the global economy, though, requires some patent protection beyond the U.S. borders. Therefore, understanding the systems and strategies for determining how and where to apply for protection outside the U.S. is critical for operating in the global economy. This class will provide information about systems and strategies for obtaining patent protection outside the U.S.

Description: The class will provide an overview of the laws and requirements, and explain the procedures in obtaining foreign patent rights. International treaties such as the Patent Cooperation Treaty (PCT) will be discussed. The PCT enables the applicant to begin the patent process in most of the world's countries simultaneously. The European Union (EU) unitary patent, the first multinational patent, and unified patent court will also be discussed. The EU unitary patent and the unified court have been in development for a number of years and is about to launch despite delays caused by Brexit. Foreign filing rights are easy to lose and costs can be difficult to contain, however, the class will also provide some strategies for effective foreign filing in spite of the difficulties.

Target Audience: Engineers in large and small companies with new ideas, inventors, entrepreneurs seeking to develop a patent strategy, anyone interested in learning about patents and how to obtain a patent outside the U.S.

Benefits of attending: Understanding the process and requirements for obtaining a foreign patent;

information about how to leverage U.S. patents rights in the foreign application process; understanding the procedures in order to make effective business decisions and contain costs. Course will include handouts including a list of resources.

Course outline:

- I. Patents
 - A. Quick overview of what patents protect and why patent protection should be pursued.
 - B. High level view of process
 - C. Foreign filing license
- II. Foreign patents
 - A. Basis for foreign patent protection
 - B. Representation
 - C. Differences in the process as compared to U.S.
 - i. Patent eligibility
 - ii. Inventorship
 - iii. Patent Types
 - iv. Process
 - v. Fees
- III. International applications – i.e., starting the foreign application process in many countries at once
 - A. Patent Cooperation Treaty
 - B. Regional applications
- IV. The Unitary Patent and Unified Patent Court -- new developments in the Old World
 - A. What it is and how it works
 - B. Proposed dates of implementation
 - C. Filing options
- V. Protection strategies
- VI. A few words about enforcement

Christine Kuta is an Intellectual Property lawyer. Her practice includes Intellectual Property strategy, portfolio development and management, and patent and trademark prosecution, search and opinions. Ms. Kuta counsels clients in a wide variety of technical areas including computer systems and software applications, medical devices, lighting systems, optics, materials and manufacturing processes, complex data management systems, electronics, energy management systems and energy storage including fuel cells, mechanical devices and consumer products including clothing and accessories.

**Decision (Run/Cancel) Date for this Course is
Monday, October 16, 2017**

Payment received by October 12

IEEE Members \$50

Non-members \$60

Payment received after October 12

IEEE Members \$60

Non-members \$70

<http://ieeeboston.org/patenting-outside-u-s-fall-2017>

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

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<http://ieeeboston.org/course-proposals/> .

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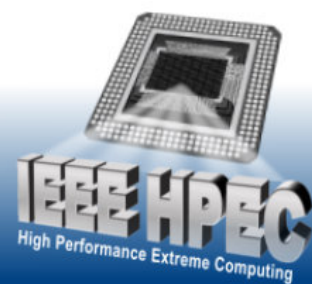
CALL FOR PAPERS



2018 IEEE High Performance Extreme Computing Conference (HPEC '18)

Twenty-second Annual HPEC Conference

25 - 28 September 2018
Westin Hotel, Waltham, MA USA



www.ieee-hpec.org

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The IEEE High Performance Extreme Computing Conference (HPEC '18) will be held in the Greater Boston Area, Massachusetts, USA on 25 – 28 September 2018. The HPEC charter is to be the premier conference in the world on the confluence of HPC and Embedded Computing.

The technical committee seeks new presentations that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- Machine Learning
- Graph Analytics and Network Science
- Advanced Multicore Software Technologies
- Advanced Processor Architectures
- Automated Design Tools
- Big Data and Distributed Computing
- Big Data Meets Big Compute
- Case Studies and Benchmarking of Applications
- Cloud HPEC
- Computing Technologies for Challenging Form Factors
- ASIC and FPGA Advances
- Data Intensive Computing
- Digital Front Ends
- Fault-Tolerant Computing • Embedded Cloud Computing
- General Purpose GPU Computing
- High Performance Data Analysis
- Interactive and Real-Time Supercomputing
- Mapping and Scheduling of Parallel and Real-Time Applications
- New Application Frontiers
- Open System Architectures
- Secure Computing & Anti-Tamper Technologies

HPEC accepts two types of submissions:

1. Full papers (up to 6 pages, references not included), and
2. Extended abstracts (up to 2 pages, references included).

IMPORTANT DATES:

Submission Deadline: **May 18, 2018**
Notification of Acceptance: **July 1, 2018**
Camera Ready Deadline: **August 1, 2018**

Preference will be given to papers with strong, quantitative results, demonstrating novel approaches or describing high quality prototypes. Authors of full papers can mark their preference for a poster display or an oral presentation. Presenters who wish to have hardware demonstrations are encouraged to mark their preference for a poster display. Accepted extended abstracts will be displayed as posters. All paper and extended abstract submissions need to use the approved IEEE templates. Full paper submissions with the highest peer review ratings will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions and extended abstracts are published on ieee-hpec.org. Vendors are encouraged to sign up for vendor booths. This will allow vendors to present their HPEC technologies in an interactive atmosphere suitable for product demonstration and promotion. Papers can be declared "student paper" if the first author was a student when doing the presented work, and will be eligible for the "IEEE HPEC best student paper award." Papers should not be anonymized. We welcome input (hpec@ieee-hpec.org) on tutorials, invited talks, special sessions, peer reviewed presentations, and vendor demos. Instructions for submitting will be posted on the conference web site shortly. Full paper submissions should use the approved IEEE templates. The highest scoring submissions will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions are published on ieee-hpec.org.

Advanced Embedded Linux Optimization

Time & Date: 6 - 9PM, Mondays, Jan. 8, 15, 22 & 29, 2018 (12 hours of instruction!)

Location: Woburn, MA area near to Rt. 95/128

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand debugging, profiling and testing high performance Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.
- To give students the confidence to apply these concepts to their next Embedded Linux project.

Course Schedule Day 1

Getting Started with Embedded Linux
 Embedded Linux Training Overview
 Terminology
 Linux Versioning
 The GPL
 Building the Kernel Source Code
 Embedded Linux Kernels
 BSPs and SDKs
 Linux References (Books and Online)
 A Development Cycle Focused on Performance
 A Basic Optimization Process
Basic Debugging Review
 Embedded Applications Debug
 GDB, GDB Server and the GDB Server Debugger
 Other Debuggers
 An Eclipse Remote Debug Example
 Debugging with printk, syslog, syslogd and LTTng
System-Level Debug
 System-Level Debug Tools
 The /proc and /sys Filesystems
 Basic Logging
 KDB and KGDB
 Crash Dumps and Post-Mortem Debugging
Debugging Embedded Linux Systems
 Backend Debuggers
 In-Circuit Emulators
 Hardware Simulators
 Analyzers

Course Schedule Day 2

Requirements Development

Performance Requirements
 Derived Requirements
 Testability and Traceability
 Reviewing Requirements
 Designing for Performance
 Design for Test (DFT)
 Agile Software Design
 Software and Linux Decomposition
 Memory Management
 CPU and OS Partitioning
 Design Reviews
 Coding for Performance
 Coding Standards and Consistency
 Languages, Libraries and Open Source
 Components
 Learning Magic Numbers
 Letting Compilers Work For You
 Global, Static and Local Variables
 Code Reviews

 Software Testing
 Unit-Level Testing
 System-Level Testing
 Code Coverage Tools
 gcov
 Automated Testing
 Some Embedded Linux Test Recommendations
 DebugFS
 Configuring DebugFS
 DebugFS Capabilities
 Advanced Logging
 LogFS
 Using Logwatch and Swatch
 Using syslogd and syslog-ng
 Tracing
 ptrace and strace
 New Tracing Methods
 SystemTap
 Ftrace, Tracepoints and Event Tracing
 Tracehooks and utrace
 Profiling
 Basic Profiling
 gprof and Oprofile
 Performance Counters
 LTTng

Another DDD Example
 Manual Profiling
 Instrumenting Code
 Output Profiling
 Timestamping

Course Schedule Day 3

Addressing Performance Problems
 Types of Performance Problems
 Using Performance Tools to Find Areas for
 Improvement
 Application and System Optimization
 CPU Usage Optimization
 Memory Usage Optimization
 Disk I/O and Filesystem Usage Optimization
 Measuring Embedded Linux Performance
 Some Ideas on Performance Measurement
 Common Considerations
 Uncommon Considerations
 Using JTAG Methods
 BootLoader Measurements
 Boot Time Measurements
 The Perf Tool
 Origins of Perf
 The Perf Framework
 Perf Commands and Using Perf
 Listing Events
 Counting Events
 Profiling with Perf
 Static Tracing with Perf
 Dynamic Tracing with Perf
 Perf Reporting
 Performance Tool Assistance
 Recording Commands and Performance
 System Error Messages and Event Logging
 Dynamic Probes
 Jprobes and Return Probes
 Kernel Probes
 Kexec and Kdump
 Improving Boot Performance
 Boot Time Optimization
 The Linux Fastboot Capability
 Building a Smaller Linux
 Building a Smaller Application
 Filesystem Tips and Tricks

Some Notes on Library Usage

Course Schedule Day 4Improving Kernel Performance

Kernel Hacking

CONFIG_EMBEDDED

Configuring printk

Test Code

Configuring Kernel and IO Scheduling

Improving CPU Performance

Run Queue Statistics

Context Switches and Interrupts

CPU Utilization

Linux Performance Tools for CPU

Process-Specific CPU Performance Tools

Stupid Cache Tricks

Improving System Memory Performance

Memory Performance Statistics

Linux Performance Tools for Memory

Process-Specific Memory Performance Tools

More Stupid Cache Tricks

Improving I/O and Device Driver

Performance

Disk, Flash and General File I/O

Improving Overall Performance Using theCompiler

Basic Compiler Optimizations

Architecture-Dependent and Independent Optimization

Code Modification Optimizations

Feedback Based Optimization

Application Resource Optimization

The Hazard of Trust

An Iterative Process for Optimization

Improving Development Efficiency

The Future of Linux Performance Tools

Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

Decision (Run/Cancel) Date for this Course is Thursday, December 28, 2017

Payment received by December 26**IEEE Members \$395****Non-members \$415****Payment received after December 26****IEEE Members \$415****Non-members \$435**

<http://ieeeboston.org/advanced-embedded-linux-optimization-2>

IEEE Boston Section Social Media Links:**Twitter:** <https://twitter.com/ieeeboston>**Facebook:** <https://www.facebook.com/IEEEBoston>**YouTube:** <https://www.youtube.com/user/IEEEBostonSection>**Google+:** <https://plus.google.com/107894868975229024384/>**LinkedIn:** <https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about>

Last Notice Before Course Begins, Please Register Now!!!

Introduction to Embedded Linux

Time & Date: 6 - 9PM, Mondays, Oct. 16, 30, Nov. 6, **23** (12 hours of instruction!)
(Note date change: October 23rd date changes to November 23)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4 day course introduces the Linux Operating System and Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part of the course covers testing, booting and configuring of Embedded Linux systems including embedded cross-development and target board considerations.

Who Should Attend - The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives

- To provide a basic understanding of the Linux OS and the Eclipse IDE framework.
- To understand the complexities of Embedded Linux Distributions in embedded systems.
- To learn how to configure, boot and test Embedded Linux distributions and applications running on Embedded Linux target systems.
- To give students the confidence to apply these concepts to their next Embedded Linux project

Hardware and Software Requirements - The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ installation or prior knowledge of C-based Makefiles is useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials

- Linux Kernel Development by Robert Love
- Linux System Programming by Robert Love
- Embedded Linux Primer by Christopher Hallinan
- Pro Linux Embedded Systems by Gene Sally
- Embedded Linux Development Using Eclipse by Doug Abbott
- Linux Device Drivers by Jonathan Corbet et al
- Essential Linux Device Drivers by Sreekrishnan Venkateswaran

Course Schedule Day 1

Embedded Development Basics

Embedded Systems Characteristics

Embedded Real-Time Systems

Embedded Linux Systems and the Internet of Things (IOT)

Embedded Linux Basics

Embedded Linux Training Overview

Linux Terminology, History and Versioning

The Linux Community: Desktop & Embedded Linux and the GPL

Linux References (Books and Online)

Getting Started in Embedded Linux

Kernel Source Code

Building the Kernel

Embedded Linux Kernels

Linux 2.6, 3.x and 4.x

Embedded Linux Kernel Overview

Process and Threads Management

Signals and System Calls

Synchronization, IPC and Error Handling

Timing and Timers

Memory Management and Paging

The I/O Subsystem: A Tale of Two Models

Modularization

Debugging

Process-Level and System-Level Debug

GDB, GDB Server and the GDB Server Debugger

Other Debug and Test Tools

An Eclipse Remote Debug Example

Advanced Debug with printk, syslogd and LTTng

System-Level Debug

System-Level Debug Tools

The /proc Filesystem

Advanced Logging Methods

KGDB and KDB

Crash and Core Dumps

Course Schedule Day 2

Process & Threads Management

What are Processes and Threads?

Virtual Memory Mapping

Creating and Managing Processes and Threads

Thread-Specific Data (TSD)

POSIX

The Native POSIX Threading Library (NPTL)

Kernel Threads

Signals in Embedded Linux

System Calls in Embedded Linux

Scheduling

Linux 2.4 and 2.6 Scheduling Models

The O(1) Scheduler

The Completely Fair Scheduler (CFS)

Synchronization

Via Global Data

Via Semaphores, Files and Signals

Condition and Completion Variables

Mutexes and Futexes

Inter-Process Communications (IPC)

Message Queues

Semaphores Revisited

Shared Memory

Pipes and FIFOs

Remote Procedure Calls

Networking

Course Schedule Day 3

Memory Management and Paging

Linux, Demand Paging and Virtual Memory

Allocating User and Kernel Memory

Mapping Device Memory

The Slab Allocator

The OOM Killer

Managing Aligned Memory

Anonymous Memory Mappings

Debugging Memory Allocations

Locking and Reserving Memory

Huge Pages

Memory in Embedded Systems

Error Handling

errno and perror

strerror and strerror_r

oops, panics and Segmentation Faults

Timing

How Linux Tells Time

Kernel, POSIX and Interval Timers

High-Resolution Timers (HRTs)

Sleeping

Sleep Waiting and Spinlocks

Using Timers

Embedded Recommendations for Timing

Modularization

Creating and Building a Module

A Simple Kernel Module

Module Loading

Module Dependencies

Module Licensing

Shared Libraries

A Shared Library Example

Static and Dynamic Libraries

Interrupt and Exception Handling

Bottom Halves and Deferring Work

Course Schedule Day 4

The I/O Subsystem: A Tale of Two Models

The UNIX Device Driver Model

The Standard I/O Interface

Major and Minor Numbers

Configuring the Device Driver

The Evolution of the New Device Driver Model

The Initial Object-Oriented Approach

Platform Devices, Busses, Adapters and Drivers

A Generic Subsystem Model

The Generic Subsystem Model in Detail

Subsystem Registration

The Probe and Init Functions

The Show and Store Functions

User Access via the /sys Filesystem

Configuring the New Device Driver

The udev Linux Application

Comparing the Two Driver Models

Advanced I/O Operations

Standard UNIX I/O Operations

Scatter-Gather and Asynchronous I/O

Poll/Select and Epoll

Memory-Mapped I/O

File Advice

I/O Schedulers and inotify

The Linux Boot Process

The Root Filesystem

Desktop Linux Boot

Bootloaders and U-Boot

Embedded Linux Boot Methods

Building and Booting from SD Cards

Managing Embedded Linux Builds

Configuring and menuconfig

Oldconfig, menuconfig, xconfig and gconfig

Building Custom Linux Images

Target Image Builders

The Open Embedded Project and the Yocto Project

System Architecture Design Approaches

Deploying Embedded Linux

Choosing and Building the Root Filesystem

Module Decisions

Final IT Work

Embedded Linux Trends

Development Trends

Monitoring Trends

Testing Trends

Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

**Decision (Run/Cancel) Date for this Course is
Friday, October 6, 2017**

Payment received by October 2

IEEE Members \$400

Non-members \$430

Payment received after October 2

IEEE Members \$430

Non-members \$455

<http://ieeeboston.org/introduction-embedded-linux-fall-2017>

Embedded Linux Board Support Packages and Device Drivers

Date & Time: 6 - 9PM; Mondays, Nov. 13, 27, Dec. 4, 11 & 18 (15 hours of instruction!)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 5-day technical training course provides advanced training in the development of Embedded Linux Board Support Packages (BSPs) and Device Drivers. The first part of the course focuses on BSP and Software Development Kit (SDK) development in an Embedded Linux context with a focus on application performance measurement and improvement. The latter part of the course covers Embedded Linux Device Driver development including key device driver decisions and deployment considerations for Embedded Linux BSPs.

Who Should Attend - The course is designed for real-time engineers who are developing Embedded Linux BSPs and Device Drivers for Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Linux BSP and Device Driver development.

Course Objectives

- To gain an understanding of the complexities of BSP and SDK development and their uses in Embedded Linux systems.
- To provide a basic understanding of the Linux I/O Subsystem and the Device Driver Models provided with Embedded Linux distributions.
- To gain an in-depth understanding of character-based device drivers in Embedded Linux
- To understand key device driver subsystems including relatively slow I/O interconnects such as I2C, SPI and USB as well as high-speed interfaces such as Ethernet, USB 3.0 and PCIe

- To give students the confidence to apply these concepts to their next Embedded Linux project.

Course Schedule Day 1

Getting Started with Embedded Linux

Embedded Linux Training Overview
Linux Terminology, History and the GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs
Linux References (Books and Online)
BSP Requirements
U-Boot and Bootloader Development

Embedded Linux BSP Development Basics

Basic BSP Development
Files and Filesystem Support
The I/O Subsystem: Talking to Hardware
Memory Management and Paging
Error Handling in Embedded Linux BSPs
Timing and Timers
Interrupt and Exception Handling in BSPs
BSP Deployment Issues and Practices

Embedded Linux SDK Basics

The 3 Pieces of an SDK
Embedded Linux Distributions and the GNU Compiler Collection (GCC)
Other Embedded Linux Development Tools

Library Support, Glibc and Alternatives
SDK Deployment and Support

Course Schedule Day 2

Debugging

GDB, GDB Server and the GDB Server Debugger
Other Debug and Test Tools
An Eclipse Remote Debug Example
Advanced Debug with printk and syslogd

System-Level Debug

System-Level Debug Tools
The /proc and sys Filesystems
Advanced Logging Methods
KGDB and KDB
Crash Dumps

Debugging Embedded Linux Systems

Configuring Embedded Linux

Config Methods
Config Syntax
Adding Code to the Linux Kernel

Bootting Embedded Linux

Processor Startup
Initial Functions
The initcalls
Using __init Functions
NFS Booting

Root File Systems

RAMdisk Booting with initrd
RAMdisk Booting with initramfs
initrd vs initramfs
Root File System Development
Busybox Development
Building a RAMdisk for an initrd
Building a RAMdisk for an initramfs
Flash File System Development

Course Schedule Day 3

Testing and Debug of Embedded Linux BSPs

Kernel Debug and Kernel Probes
Kexec and Kdump
The Linux Test Project (LTP)
Performance Tuning Embedded Linux BSPs
Virtualization

Measuring Embedded Linux BSP Performance

Common Considerations
Uncommon Considerations
BootLoader Optimizations
Boot Time Measurements
Effective Memory and Flash Usage
Filesystem Performance Measurement
Some Ideas on Performance Measurement

The Original UNIX Device Driver Model

The fops and file structs
The inode and dentry structs
Major and Minor Numbers
Embedding Channel Information
Deferring Work
The /proc Filesystem
Configuring the Device Driver
A Simulated Device Driver
Modularization Revisited

Course Schedule Day 4

The Evolution of a New Driver Model

The Initial Object-Oriented Approach
Platform Devices and Drivers
A Generic Subsystem Model

The Generic Subsystem Model in Detail

Subsystem Registration
The Probe and Init Functions
The Show and Store Functions
User Access via the /sys Filesystem
Configuring the New Device Driver

The udev Linux Application

Comparing the Two Driver Models

The Flattened Device Tree (FDT)
openBoot and its Effect on Embedded Linux
The Device Tree Script (dts) File
The Device Tree Compiler (dtc)
The Device Tree Blob (dtb) File
Building a dtb File

Hybrid Device Drivers

Other fops Functions
The Need for ioctl

Linux Device Driver Subsystems

Direct Connect Device Drivers
Serial/Console Drivers, I2C & SPI
Real-Time Clocks and Watchdogs
GPIO and the Pinmux
Flash MTDs and Direct Memory Access
USB, Power and CPU Management
Video and Audio
PCI and VME
Block Devices
RAMdisk and Flash Filesystems
MMCs and SD Cards

Network Device Drivers

MAC and PHY Device Drivers
net_device and net_device_stats
Network Device Initialization
Device Discovery and Dynamic Initialization
Network Interface Registration
Network Interface Service Functions
Receiving and Transmitting Packets
Notifier Chains and Device Status Notification

Course Schedule Day 5

Unwired Device Drivers

Wireless Device Drivers (WiFi, WLAN)
Bluetooth and BlueZ
Infrared and IrDA
Cellular from 2G to 5G
Drivers in User Space
Accessing I/O and Memory Regions
User Mode SCSI, USB and I2C
UIO
High-Speed Interconnects
PCIe
iSCSI
Infiniband
FibreChannel
Debugging Device Drivers
kdb, kgdb and JTAG
Kernel Probes
Kexec and Kdump
Kernel Profiling
User Mode Linux
Performance Tuning Device Drivers

Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at LynuxWorks, Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based software development tools, training and consulting services for the embedded systems market.

**Decision (Run/Cancel) Date for this Course is
Friday, November 3, 2017**

Payment received by November 1

IEEE Members	\$450
Non-members	\$490

Payment received after November 1

IEEE Members	\$490
Non-members	\$525

Writing Agile User Story and Acceptance Test Requirements -

Cut Creep Overruns, Disappointment, and Embarrassment

Date & Time: Tuesday, December 12; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

Everyone complains that poor requirements are the major cause of project problems. Yet, like the weather, nobody does much about it, at least not effectively. Traditional approaches advocate writing voluminous requirements documents that too often don't seem to help much and may even contribute to difficulties. Agile goes to the opposite extreme, relying on brief requirements in the form of three-line user stories that fit on the front an index card and a few user story acceptance criteria that fit on the card's back. Surprise, as Mark Twain noted, in some ways it's even harder to write Agile's brief requirements effectively. This interactive workshop reveals reasons user stories and their acceptance tests can fall short of their hype, explains critical concepts needed for effectiveness, and uses a real case to provide participants guided practice writing and evaluating user stories and their acceptance criteria/tests.

PARTICIPANTS WILL LEARN:

- * Major sources of poor requirements that cause defects, rework, and cost/time overruns.
- * How Agile user stories and their acceptance criteria/tests address these issues.

- * Difficulties that still afflict requirements in Agile projects and why they persist.
- * Writing more effective user stories and acceptance criteria/tests.
- * What else is necessary to produce working software that provides real value.

WHO SHOULD ATTEND:

This course has been designed for product owners, analysts, developers, and other Agile (and other) project team members who are or should be involved in defining requirements.

AGILE, USER STORY FUNDAMENTALS

Agile Manifesto's relevant points
 Characterization of traditional approaches
 Waterfall and big up-front requirements
 Agile's sprints and backlogs alternative
 Agile project team roles
 User story "As a <role>..." (Card)
 User story acceptance criteria (Confirmation)
 Estimating user story size
 Splitting and refining
 Prioritizing and allocating to backlogs/sprint
 Constructing/implementing (Conversations)
 Reviewing, retrospectives
 Grooming backlog and reprioritizing

**REQUIREMENTS ARE REQUIREMENTS—
OR MAYBE NOT**

User stories are backlog items, features
 Chicken and egg relation to use cases
 Issues and inconsistencies
 Business vs. product/system requirements
 “Levels Model” of requirements
 Other mistaken presumptions
 Requirements overview
 Where user stories should fit, do fit instead
 Conversation conundrum

WRITING MORE SUITABLE USER STORIES

Problem Pyramid™ tool to get on track
 Exercise: Using the Problem Pyramid™
 Exercise: Business Requirement
 User Stories
 Issues identifying requirements
 Product owner and business analyst roles
 Project team participation
 Dictating vs. discovering
 Data gathering and analysis
 Planning an effective interview
 Controlling with suitable questions
 Then a miracle occurs...

AND USER STORY ACCEPTANCE TESTS

Missed and unclear criteria
 Turning criteria into tests, issues
 How many tests are really needed
 Test design techniques
 Checklists and guidelines
 Decision trees, decision tables
 Boundary testing
 Testing is main means to control risk

Defects and new user stories
 Testing that user story focus misses
 Reactive vs. proactive risk analysis
 Given, when, then format

Exercise: Write User Story Acceptance Criteria
 Exercise: Design their Tests
 Exercise: Review Your User Stories/Tests

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, *Discovering REAL Business Requirements for Software Project Success*, he regularly works with and trains business and systems professionals.

**Decision (Run/Cancel) Date for this Courses is
 Tuesday, December 5, 2017**

Payment received by Nov. 28

IEEE Members \$220

Non-members \$245

Payment received after Nov. 28

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Non-members \$265

<http://ieeeboston.org/writing-agile-user-story-acceptance-test-requirements-2>



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Risk Management Methods for Test Projects

Make Sure the Most Important Testing Is Done in Limited Available Time

Date & Time: Thursday, December 14; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

Testing is our primary means of reducing risks related to systems and software. All testing is risk-based in that there are more potential tests than we have time and resources to run, so we choose those that address higher risks. The difficulty is adequately identifying the potential risks, for which a number of structured techniques are described. Risk management involves obtaining, directing, and controlling resources for continuously planning, strategizing, identifying, analyzing, prioritizing, preventing, responding to, mitigating, monitoring, controlling, and reporting risk. Key types of risks and identification approaches are distinguished. Powerful Proactive Testing™ techniques are demonstrated that enhance conventional reactive testing risk analysis to enable testing higher risks not only more but earlier. Exercises aid learning by allowing participants to practice applying practical methods to realistic examples.

Participants will learn:

- The elements of risk and risk response, and their relation to software development and testing.
- Importance of distinguishing business, management, functional, and technical risk causes and effects.
- Alternative methods for identifying, analyzing, classifying, and prioritizing the several types of risks.
- Proactive Testing™ methods that enhance conventional reactive testing risk identification, response.
- Monitoring, evaluating, adjusting, and reporting on risk activities, findings, and results.

WHO SHOULD ATTEND: This course has been designed for analysts, designers, programmers, testers, auditors, users, and managers who rely on, plan, oversee, and/or carry out testing of software products.

1 NATURE AND IMPORTANCE OF RISK

Murphy's Law; O'Brien's Law
 Relation of risk to software and testing
 Classical risk management
 Impact and probability risk elements
 Classical risk mitigation, contingency plans
 Costs, ease of detecting, controlling vs. harm
 Quantifying qualitative risk, tricks and traps
 Types, classifications of risks
 Threats, vulnerabilities, triggers
 Risk identification analysis methods
 Business, functional, and operational risks
 Direct and indirect forms of injury
 Management and technical risks
 Effects vs. causes risk identification
 Monitoring, controlling, reporting risks

2 PROJECT MANAGEMENT RISKS

Most frequently encountered risks
 Changing requirements and scope creep
 Lack of management support, priorities
 Typically unrecognized interrelationships
 Features/quality, resources, schedule risks
 Software risks—or just poor management
 Sizing implications for software QA/testing
 Traditional checklists for project managers
 Evaluating risk factor checklists usefulness
 Software risk taxonomy
 Monitoring and managing risk as a project

3 CONVENTIONAL RISK ANALYSIS

Testing riskier features, components more
 Costs, additional testing resources vs. fixed
 System, development practices checklists
 Design analysis vs. prioritizing test cases
 Common subjective risk judgment methods
 Rating vs. ranking, setting objective criteria
 Reporting, gaining agreement on risks

Differentiating user and technical views
 Risk analysis in test designs and test cases
 Risks of not testing some things
 Metrics to monitor effectiveness, efficiency
 Anticipating and measuring operational risks
 Risk management roles and responsibilities
 Reporting risk status, expected and actual
 Categorizing actuals, improving over time

4 PROACTIVE RISK-BASED TESTING

Why typical risk-based testing is reactive
 Proactive Testing™ Life Cycle
 Structured model of test planning
 Multiple levels, points of risk analysis
 Prioritization demands knowing the choices
 Project-level proactive risk analysis
 Identifying overlooked project-specific risks
 Refocusing on tests that reduce the key risks
 Letting testing drive development
 Gaining user, manager, developer support
 Identifying and analyzing lower-level risks

**Decision (Run/Cancel) Date for this Courses is
 Thursday, December 7, 2017**

Payment received by Nov. 30

IEEE Members \$220

Non-members \$245

Payment received after Nov. 30

IEEE Members \$245

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<http://ieeeboston.org/risk-management-methods-test-projects/>

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LinkedIn: <https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about>

Developing Reusable Test Designs

Be an Instant Expert--Run More, and More Thorough, Tests in Less Time

Date & Time: Friday, December 15; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Would you like to be an instant testing expert, able to start testing effectively in new situations without delay? And would you like to spend more of your time running tests and less of your time creating the tests? Reusable test designs are a little-known but powerful test planning/design tool that make it possible for you to run more effective test cases in less time. This interactive seminar/workshop shows you how to apply a systematic structured Proactive Testing™ approach that first enables you to design much more thorough tests than traditional methods. Then, you'll discover how to convert your test designs into reusable test designs that you can apply instantly in new situations. You'll develop several reusable test designs in class and be ready to add more to your toolkit back on the job. Exercises enhance learning by allowing participants to practice applying practical techniques to an actual case.

Participants will learn:

- How test designs fit into the overall test planning structure and provide special advantages
- Systematic reliably repeatable methods for identifying test designs to test a given system.
- Checklists and guidelines that enable you to spot the conditions traditional methods overlook.
- Converting your project-specific test designs into reusable test designs you can use for other systems.
- Applying reusable test designs to jumpstart your testing with instant expertise and effectiveness.
- Quickly and reliably selecting the subset of test cases suitable for scale and risk.

WHO SHOULD ATTEND: This course has been designed for testers, managers, analysts, designers, programmers, auditors, and users who plan, oversee, and/or carry out testing of software products.

PROACTIVE TEST DESIGN BENEFITS

Proactive vs traditional reactive testing
 Proactive Testing™ Life Cycle advantages
 IEEE Standard for Test Documentation
 Often-overlooked key to proper prioritizing
 Systematic drill-down strategy
 Master and detailed test plans
 Test design specifications
 Test case specifications
 How taking time to structure saves time
 Structuring to make test sets manageable
 Facilitating reconstruction of test data
 Taking off the blinders to allow selectivity
 Re-using instead of rebuilding test designs
 Instant expertise for testing new situations

IDENTIFYING NEEDED TEST DESIGNS

Functional (black box) testing
 Three-level approach to functional testing
 Keys for thoroughness
 Breaking down to manageable pieces
 Functionality Matrix technique
 Use case perspective
 Technical software actions
 Test design specifications that are needed

DESIGNING TESTS MORE THOROUGHLY

How designing adds thoroughness
 Traditional test design still misses a lot
 Focused brainstorming for a better start
 Checklists and guidelines to fill the gaps

Tests based on data formats
 Coverage of data and process models
 Decision trees and tables
 Concerns common to all types of testing
 Equivalence classes and partitioning
 Ranges and boundary testing
 GUI and navigation issues
 Often-overlooked other dimensions to test
 Formal/informal test design specifications
 Extracting the reusable elements
 Enhancing with system-specific tests
 Link to driving effective automated tests

Other essential test case component
 Finding and creating test data
 Test script and matrix formats
 Simple and sophisticated automation

**Decision (Run/Cancel) Date for this Courses is
 Friday, December 8, 2017**

Payment received by Dec. 1

IEEE Members \$220

Non-members \$245

Payment received after Dec. 1

IEEE Members \$245

Non-members \$265

SPECIFYING (REUSABLE) TEST CASES

Translating test designs into test cases
 Selecting scaled subset based on risk
 Reusable test case specifications

<http://ieeeboston.org/developing-reusable-test-designs/>

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically diverse sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is

<http://ieeeboston.org/course-proposals/>

Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course)
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.