

BOSTON



THE REFLECTOR

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COMPUTER &
YP CHAPTER
MEETING

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HOMELAND
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Please Register by March 24 to get the Early Registration Discount and Save \$\$\$\$!!!

SAVE THE DATE! PLAN TO ATTEND!

2017 IEEE International Symposium on Technologies for Homeland Security

25 – 26 April Westin Hotel, Waltham, MA

<http://ieee-hst.org/>



PLENARY SPEAKERS:

Kay C. Goss, CEM, President, World Disaster Management, LLC Internationally recognized expert, lecturer, author on *Emergency Management and General Resiliency*

Dr. Melissa Flagg, CEO, Flagg Consulting, LLC. Previously she served as the Deputy Assistant Secretary of Defense for Research in the Office of the Assistant Secretary of Defense, Research and Engineering (OASDR&E) within the Department of Defense (DoD)

The 16th annual IEEE Symposium on Technologies for Homeland Security (HST '17), will be held 25-26 April 2017 **must attend event**, in the Greater Boston, Massachusetts area. This symposium brings together innovators from leading academic, industry, business, Homeland Security Centers of Excellence, and government programs to provide a forum to discuss ideas, concepts, and experimental results.

Produced by IEEE with technical support from **DHS S&T, IEEE, IEEE Boston Section, and IEEE-USA** and organizational support from **MIT Lincoln Laboratory, Raytheon, Battelle, and MITRE**, this year's event will once again showcase selected technical paper and posters highlighting emerging technologies in the areas of

There are over 110 paper and posters to be presented at the symposium with focus on technologies with applications available for implementation within about five years. All areas will cover the following common topics:

- Strategy and threat characterization, CONOPs, risk analysis,
- Modeling, simulation, experimentation, and exercises & training, and
- Testbeds, standards, performance and evaluations.

In addition there will be plenary sessions as well as ample networking activities to interact and exchange ideas with speakers and other symposium attendees.

Contact Information

For more detailed information on sponsorship and Exhibit Opportunities, visit the website <http://ieee-hst.org/> or email: information@ieee-hst.org.

The symposium technical program as well as the conference registration and hotel reservation pages are now online (www.ieee-hst.org)

Technical Sessions

Cyber Security Track:

- #1: Cyber-Physical Systems
- #2: Authentication
- #3: Intrusion Detection
- #4: Approaches in Cybersecurity Modeling
- #5: Secure Systems
- #6: Analytics
- #7: Testbeds and Training Environments
- #8: Privacy
- #9: Classification and Scoring Algorithms in Cybersecurity

Attack/Disaster Track:

- #1: Critical Infrastructure
- #2: Cyber Risk Management and Intelligence Analysis
- #3: Resilience
- #4: Disaster Preparedness and Response
- #5: Network Vulnerability
- #6: Situational Awareness
- #7: Machine Learning and UAV
- #8: Terrorism and Disaster Preparedness

Border Security Track:

- #1: Airborne Sensing
- #2: Enhancing Data Exploitation 1
- #3: Enhancing Data Exploitation 2
- #4: Ground-based Hardware for Border and Customs Enforcement
- #5: Counter-UAS and Small Aircraft Detection
- #6: Underwater Imaging
- #7: Human- and Cargo-Borne Concealed Threat
- #8: Radiological and Nuclear Detection

Biometrics & Forensics Track

- #1: Facial Recognition
- #2: Finger and Palm Prints
- #3: Video Analytics
- #4: Ocular Biometrics and Other Modes

Plus 20 Poster Presentations during our Welcome/networking Reception



Snow What?

by Fausto Molinet, Chair, Publications Committee

I just finished digging out from our latest snowfall. Thank goodness it wasn't what some of the experts predicted, 5" rather than 16". But, it got me thinking about weather, science and engineering and how it all fits together.

That led to reflection on something Francesca Scire Scapuzzo, Chair of the Boston Section Chapter of the Geoscience and Remote Sensing Society (GRSS) said at our Chapter Chair training session on February 8. By the way, if you are a chapter chair who couldn't make it, we missed you. There was a great exchange of information and everyone came away with something useful.

Anyhow, she mentioned that many scientists felt they didn't fit in with engineers and I suspect there is a similar feeling from the engineering side. And it's not just GRSS, quite a few years ago, one of my bosses told me that I was an engineer, so don't think like a scientist. That led to a, so far, lifelong conversation with myself on that subject.

Engineering and science, I opine, are inextricably intertwined. Engineers depend on scientists discovering new phenomena that they can use to develop new instrumentation and scientists need the tools engineers produce to develop data to support (or refute) hypotheses. Engineering principles are practical extensions of and depend on good science. A robust conversation and interaction be-

tween the groups is an absolute must for progress.

Sometimes the dichotomy between the academic approach of science and the more practical approach of engineering can get in the way although it was not always so. Specialization has helped to exacerbate the differences, as each side focuses on more detail in that interesting-topic-of-the-day. Sometimes a robust, informal venue for interchange of ideas and viewpoints helps a lot.

IEEE societies and chapters can help foster such interaction. GRSS recognizes the need to make all parties to the development of that intertwined science and technology work together. I suspect most other societies and chapters do likewise. So, consider how you can expand the discussion, maybe by finding a science oriented society where you can cosponsor some meetings or approach some academic institutions that are science, not engineering oriented and see how you can cooperate and reach out. It can't hurt and might just be successful.

And, oh yes, they're calling for more snow this weekend. Why not? It's New England and it's Winter.

As always, the views expressed in our editorials are those of the author and not necessarily those of the IEEE Boston Section

Letters to the editor can be sent to, ieeebostonsection@gmail.com



The Institute of Electrical and Electronic Engineers, Inc.

Spring 2017 Professional Development and Education Program

www.ieeeboston.org

Phased-Array and Adaptive-Array Fundamentals and Their Recent Advances

Dates and Time: Ten Monday Evenings,
Feb. 27, March 6, 13, 20, 27, April 3, 10, 24, May 1, 15
(Snow/make-up dates May 22, June 5, 12
6:00PM - 9:00PM

MITRE Corporation, Bedford, MA

Introduction to Embedded Linux

Dates and Time: Mondays, March 20, 27, April 3, 10
6:00PM - 9:00PM

More Digital Signal Processing (DSP) for Wireless Communications

Dates and Time: Wednesdays, March 22, 29, and
April 5, 12, 26; 6:00PM - 9:00PM

Software Development for Medical Device

Manufacturers: An intensive Two-day Workshop

Dates and Time: Wednesday, April 5 and Thursday,
April 6; 8:30AM - 4:30PM

Embedded Linux BSPs and Device Drivers

Dates and Time: Wednesdays, April 12, 19, 26
and May 3; 6:00PM - 9:00PM

QA and Testing in DevOps Automation

Date and Time: Thursday, April 20
8:00AM - 5:00PM

Advanced Embedded Linux Optimization

Dates and Time: Wednesdays, May 10, 17, 24 and 31
6:00PM - 9:00PM

Practical Antenna Design for Wireless Products

Dates and Time: Thursday, June 1 and Friday, June 2
9:00AM - 4:30PM

Making You A Leader Fast Track

Date and Time: Monday, May 22; 8:30AM - 5:00PM

Writing Agile User Story and Acceptance Test Requirements

Date and Time: Tuesday, May 23; 8:30AM - 5:00PM

Determining and Communicating Project Value Return on Investment (ROI)

Date and Time: Wednesday, May 24; 8:30AM - 5:00PM

Proactive User Acceptance Testing - Confident Competence

Date and Time: Thursday, May 25; 8:30AM - 5:00PM

Online Courses

(Each Online Course - 90 day access for registrants!!!)

- Verilog 101: Verilog Foundations
 - Systems Verilog 101 (SV101) Design Construct
 - Systems Verilog 102 (SV102) Verification Constructs
 - High Performance Project Management
- (Discounts available if register for all three Verilog Courses)

- Software Development for Medical Device Manufacturers
 - Reliability Engineering for the Business World
- Fundamental Mathematical Concepts Relating to Electromagnetics
 - Introduction to Embedded Linux

See our new online platform for these four new online courses!!!

All Courses are being held at the Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn unless otherwise noted. For more information on these courses and other local IEEE activity see our website at www.ieeeboston.org, email: ieeebostonsection@gmail.com, or call 781-245-5405

IEEE Boston Section Online Courses:

(Students have 90 day access to all online, self-paced courses)

Verilog101:Verilog Foundations

Full course description and registration at ,
<http://ieeeeboston.org/verilog-101-verilog-foundations-online-course/>

System Verilog 101: Design Constructs

Full course description and registration at ,
<http://ieeeeboston.org/systemverilog-101-sv101-design-constructs-online-course/>

System Verilog 102: Verification Constructs

Full course description and registration at ,
<http://ieeeeboston.org/systemverilog-102-sv102-verification-constructs-online-course/>

High Performance Project Management

Full course description and registration at ,
<http://ieeeeboston.org/high-performance-project-management-online-course/>

Introduction to Embedded Linux Part I NEW Online course

Full course description and registration at ,
<http://ieeeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/>

Software Development for Medical Device Manufacturers NEW Online course

Full course description and registration at ,
<http://ieeeeboston.org/software-development-medical-device-manufacturers-line-course/>

Fundamental Mathematics Concepts Relating to Electromagnetics NEW Online course

Full course description and registration at ,
<http://ieeeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/>

Reliability Engineering for the Business World NEW Online course

Full course description and registration at ,
<http://ieeeeboston.org/reliability-engineering-business-world-line-course/>

Entrepreneurs' Network – 6:30PM, Tuesday, 7 March

Term Sheets and Valuation

Meeting Location – Constant Contact, 3rd Floor Great Room, 1601 Trapelo Road, Waltham, MA. (Exit 28, I-95/Route 128)

PRE-MEETING DINNER at 5:15 PM (sharp) at Bertucci's, Waltham.

Company founders getting ready to raise outside financing do not want to give up more equity than necessary. Investors want more equity for their investment as a reward for the risk they are taking on the young company. Valuation is used to determine a fair trade-off of cash for equity. But, what is a reasonable valuation for a startup? Must this determination be made when first obtaining funds? What terms might an entrepreneur see when presented with a Term Sheet and what are the trade-offs when negotiating these? How do terms impact founders' managerial control of investments and operating decisions?

Our panel, including a Valuation expert, the General Manager of a large Angel investment group, and the President of startup, will discuss these issues concerning valuation and term sheets. A networking session will precede the meeting and a question and answer session will follow the panelists' presentations.

Speaker Panel:



JOHN FRANSON, CFA, Director of Globalview Advisors LLC, <http://globalviewadvisors.com>
John's over 15 years of valuation experience includes valuation of business enterprises, intangible assets, and equity instruments for various purposes including common stock valuations, business combinations, goodwill im-

pairment, corporate acquisitions and divestitures, litigation support, and financial and tax reporting.

Prior to joining Globalview Advisors in 2007, John worked as an independent consultant assisting CFOs with acquisition and divestiture projects, managing capitalization models, assessing business activity, communicating between all stakeholders, and customizing financial presentations. He was also employed with KPMG Valuation Services where he performed valuations in connection with both publicly traded and privately held companies.

John received his MS in Finance from Boston College and his BA in Economics from the University of New Hampshire. He has successfully completed the business valuation curriculum of the American Society of Appraisers (ASA), as well as the national exam on the Uniform Standards of Professional Appraisal Practice (USPAP). John is a Chartered Financial Analyst (CFA).



Christopher Mirabile, Co-Managing Director, LaunchPad Venture Group

Christopher Mirabile is the co-Managing Director of LaunchPad Venture Group. Christopher is a full-time angel and an active member of the Boston-area angel investing community with investments in more than 40 start-up companies. He was named one of XConomy's "Top Angel Investors in New England" for 2012.

Christopher is an adjunct lecturer in the MBA program at Babson College, a regular advisor and mentor to start-ups, and a frequent panelist and speaker. He is a member of the Board of Directors

or Board of Advisors of numerous start-up companies as well as several non-profits.

Christopher has served as a public company CFO with IONA Technologies PLC, a corporate and securities lawyer with Testa Hurwitz & Thibault and as a management consultant with Price Waterhouse's Strategic Consulting Group.

Christopher earned his J.D. from Boston College Law School and his B.A., with honors, from Colgate University.



Sven Karlsson, CFA, MBA, President & Co-Founder, Platelet BioGenesis

Sven Karlsson, an Eagle Scout, has over six years of experience in business development and financial analysis. Prior to co-founding Platelet BioGenesis, Sven Karlsson worked in Business Development at J.P. Morgan and as a Research Analyst at Seamans Capital Management. Sven received a B.S. in Engineering from Cornell University and an MBA with Distinction from New York University's Stern School of Business.

Moderator:

Michael S. Chester, President, International Manufacturing Consultants,
<http://www.imcglobaladvisors.com>,
intlmfg@aol.com, Past Chairman
 Boston Entrepreneurs' Network (ENET)



Mike has founded and built companies, set up manufacturing operations, formed strategic partnerships, set up global joint ventures, raised over \$40M for startups which he co-founded, both in the US and China, and commercialized technologies. Mike advises startups in high tech, clean tech, biotech, software, and manufacturing. The Chinese government has invested in Mike's companies. One of his startups provided mobile banking services in China and was acquired by a European company. BioHermes, a biotech which

he cofounded in China, was sold in 2010. Mike was VP Business Development for Tonbu, which developed web-based collaborative environments for the electronics industry grew to 142 employees. Mike spent 16 years with IBM designing robots and automation, marketing and selling IBM products to manufacturing companies, setting up global operations and supply chains, and founding an IBM consulting organization for manufacturing clients that he grew into a \$20M business. Mike also lived in China from 1986-1987 while consulting to companies owned by the Machine Building Ministry and teaching graduate courses at Hunan University.

Mike earned his BS in Electrical Engineering and MS in Computer Engineering from Syracuse University and his MBA from Union College. He is past Chair of the IEEE Boston Entrepreneurs' Network, has served on the board of APICS Boston, and was a member of the planning committee of the MIT Enterprise Forum for over 10 years. Mike is a frequent speaker at conferences on Global Entrepreneurship, Supply Chains, Manufacturing, and China business. He is judge and mentor to companies competing the Mass Challenge and the Clean Tech Open. Mike and his sons have competed on the TV show Robot Wars with their robotic rabbit, "Bunny Attack".

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Computer Society and GBC/ACM and co-sponsoring Young Professionals –
7:00PM, Wednesday, 8 March

Next Generation Sequencing: Underlying Technology and Applications to Cancer

John Methot, Director of Health Informatics Architecture at the Dana-Farber Cancer Institute



The development of DNA sequencing technology was spurred by the Human Genome Project in the 1990s resulting in massively parallel techniques that are referred to as Next Generation Sequencing. Introduced in 2006, these and subsequent technologies have revolutionized biology. Hundreds of organisms

have complete reference genomes. Hundreds of thousands of humans have been sequenced. Myriad creative adaptations of sequencing have been and continue to be devised. Sequencing is now a routine technique that is at the core of biological research in academia, industry and medicine and increasingly in medical care itself.

Precision Medicine is the concept that differences in disease risk, prognosis, and response to treatment can be elucidated at the molecular level, often using nucleic acid sequencing. While it is expected to impact many diseases precision medicine has had its earliest applications and successes in cancer. The identification of specific DNA alterations that segment what were previously considered similar tumors has lead to the development of alteration-specific drugs called targeted therapies.

This presentation will include a brief history of sequencing technology and a description of how sequencing is performed, how the large volume of resulting data is analyzed, and a brief survey of the ever-growing collection of applications. Then we'll

focus on the main application in cancer, somatic variant identification, and its use in clinical care.

John Methot is a software and systems architect with more than 30 years' experience developing applications in scientific and technical domains. Since 2006 his work has focused on genomics in the life sciences in pharmaceutical and biotech research and most recently in clinical cancer research. He holds a BS in Computer Science from the University of Washington and a Masters in Bioinformatics from the University of Illinois, Chicago. He is currently the Director of Health Informatics Architecture at the Dana-Farber Cancer Institute, and is also a co-organizer of the Boston Computational Biology and Bioinformatics group with over 1300 members.

This joint meeting of the Boston Chapter of the IEEE Computer Society and GBC/ACM will be held in the Broad Institute Auditorium (MIT building NE-30). The Broad Institute is at 415 Main St between Vassar and Ames streets. You can see it on a map at this location. The auditorium is on the ground floor near the entrance.

Up-to-date information about this and other talks is available online at <http://ewh.ieee.org/r1/boston/computer/>. You can sign up to receive updated status information about this talk and informational emails about future talks at <http://mailman.mit.edu/mailman/listinfo/ieee-cs>, our self-administered mailing list.

For more information contact Peter Mager
p.mager@computer.org

Life Members and co-sponsoring Nuclear and Plasma Science Society – 4:00PM, Wednesday, 8 March

Whistler Wave Interactions Experiments at Arecibo, Puerto Rico

By Professor Min-Chang Lee - Department of Electrical & Computer Engineering, Boston University

We report on whistler wave injection experiments at Arecibo Observatory (AO), starting with our joint US-USSR Active Space Plasma program conducted on December 24, 1989. In this AO experiment whistler waves at 10 kHz and 10 kW were transmitted from the USSR Active Satellite. The 430 MHz radar was used to diagnose whistler wave interactions with ionospheric plasmas over AO. A series of controlled whistler wave experiments with AO HF heater were subsequently carried out during 1990 - 1998. In these ionospheric HF heating experiments, 28.5 kHz whistler waves were launched from the nearby Naval transmitter (code-named NAU) located at Aguadilla, Puerto Rico. HF heater waves were used to create ionospheric ducts (in the form of large plasma sheets as parallel plate waveguides) to facilitate the entering of NAU whistler waves from the neutral atmosphere into the ionosphere.

Conjugate whistler wave propagation experiments were performed between Arecibo, Puerto Rico and Trelew, Argentina in 1997. In the next 18 years or so (1999 - ongoing) we conducted whistler wave experiments in the absence of an HF heater. Naturally-occurring large-scale ionospheric irregularities (due to spread F or TIDs) were relied on to guide whistler wave propagation from the ionosphere further into the radiation belts. Hence, we have been able to investigate whistler wave interactions with the ionosphere as well as with the radiation belts for satellite remediation research at AO. We plan to use the newly built Arecibo HF heater and NAU VLF trans-

mitter together with Arecibo UHF and microwave radars for further study of whistler wave interactions with space plasma.

Min-Chang Lee received his Ph.D. in Electrophysics/Applied Plasma Physics from University of California San Diego. Dr. Lee is currently a Professor of Electrical and Computer Engineering at Boston University (BU). In the past 25+ years he has developed an integrated educational and research program at BU in electromagnetic wave interactions with plasmas for space and energy applications, including theoretical study, field experiments, and laboratory simulation experiments. Dr. Lee is IEEE Boston Chapter Chair of Nuclear and Plasma Science Society (NPSS).

The meeting will be held at the Lincoln Lab Auditorium, 244 Wood Street., Lexington, MA at 4:00 PM. Refreshments will be served at 3:30 PM. Registration is in the main lobby. Foreign national visitors to Lincoln Lab require visit requests. **Please pre-register by e-mail to reception@ll.mit.edu and indicate your citizenship.** Please use the Wood Street Gate. For directions go to <http://www.ll.mit.edu/>

For other information, contact Steve Teahan, Chairman, at (978)763-5136, or Steve.F.Teahan@raytheon.com

Meeting Location: Lincoln Lab Auditorium, 244 Wood Street, Lexington, MA 02421, USA



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Reliability Society – 5:30PM, Wednesday, 8 March

Reliability Engineering, The Headhunter's View

Leslie Gabriele, Gabriele & Company



This meeting is an interactive discussion where you have the opportunity to investigate market trends, consider job prospects, and explore behind the scenes hiring behaviors, with an emphasis on reliability engineering in particular. The

speaker has worked in both retainer and contingency search environments and has specialized in recruiting manufacturing engineering talent for the past 30 years.

Together, we will create a lively discussion and get some answers to the questions and concerns you have about your career. The roll today of the recruiter in the job search--does the fact of the recruiter's commission help or hurt the candidate's chances? What value is derived for the employer? How many recruiters should a job searcher connect with? What's the difference between contingency and retained recruiters and how do I pick one? The latest set of accepted standards for what a resume should look like--what works and what doesn't work? A resume for visual impact or one to get by screening software? What steps do you take if the job you thought you had forever ends tomorrow? How has social media changed the job hunting process? What are the most common interviewing mistakes to avoid?

Agenda

5:30-6:00 Sign In, Networking, Light Dinner & Refreshments

6:00-6:10 Chapter Chair Greetings and Announcements

6:10-7:30 Leslie Gabriele, Gabriele & Company

7:30-7:45 Q&A Session, Meeting Adjourns

Leslie Gabriele of Gabriele & Company, Recruiters for Manufacturing and Materials

Leslie Gabriele's recruiting career ranges from start-ups to Fortune 50's, from individual contributors to presidents for a wide variety of industries and disciplines. She founded Gabriele & Company in 1993. At McInturff & Associates, she established the manufacturing practice. At Fenwick Partners / Korn Ferry, she completed search engagements for top level executives.

Leslie is the founder of the VP of Operations Group, past Chair of the Boston Chapter of the Society of Manufacturing Engineers (SME), past board member of the American Society of Quality Control (ASQC), American Production and Inventory Control Society (APICS), and steering committee member for the Manufacturing Roundtable. Leslie earned her MBA at the Wallace E. Carroll Graduate School of Management at Boston College.

Email: leslie@gabrieleandcompany.com

Meeting Location: This meeting will be held on Wednesday, March 8, 2017 at MIT Lincoln Laboratory, 3 Forbes Road, Lexington, MA.

To assist us in planning this meeting, please pre-register at

<https://events.vtools.ieee.org/m/43854>.

Photonics Society – 6:30PM, Thursday, 9 March

Reconfigurable Plasmonics and Metamaterials

Prof. Yongmin Liu, Northeastern University, Boston, MA



Plasmonics has become a very important branch in nano optics. It allows us to concentrate, guide, and manipulate light at the deep subwavelength scale, promising enhanced light-matter interaction, next-generation optical circuits, sub-diffraction-limited imaging, and ultrasensitive biomedical detection [1-4].

Furthermore, the assembly of judiciously designed metallic structures can be used to construct metamaterials and metasurfaces with exotic properties and functionalities, including anomalous refraction/reflection, strong chirality and invisibility cloak [5,6]. There is a pressing need of tunability and reconfigurability for plasmonics and metamaterials, in order to perform distinct functionalities and miniaturize the device footprint.

In this talk, I will present our recent work in reconfigurable plasmonics and metamaterials. First, I will discuss the first demonstration of reconfigurable plasmonic lenses operating in microfluidic environment, which can dynamically diverge, collimate and focus surface plasmons [7]. Second, I will present a novel graphene metasurface to fully control the phase and amplitude of infrared light with very high efficiency. It manifests broad applications in beam steering, biochemical sensing and adaptive optics in the crucial infrared wavelength range [8]. Finally, I will discuss origami-based, dual-band chiral metasurfaces at microwave frequencies.

The flexibility in folding the metasurface provides another degree of freedom for geometry control in the third dimension, which induces strong chirality from the initial, 2D achiral structure [9]. These re-

sults open up a new avenue towards lightweight reconfigurable meta-devices.

References: [1] S. A. Maier, "Plasmonics: fundamentals and applications", Springer Science+ Business Media (2007); [2] T. Zentgraf et al., "Plasmonic Luneburg and Eaton lenses", *Nature Nanotechnology* 6, 151 (2011); [3] Y. M. Liu et al., "Compact magnetic antennas for directional excitation of surface plasmons", *Nano Letters* 12, 4853 (2012); [4] Z. Wang et al., "Manipulating Smith-Purcell Emission with Babinet Metasurfaces", *Physical Review Letters* 117, 157401 (2016); [5] Y. M. Liu and X. Zhang, "Metamaterials: a new frontier of science and technology", *Chemical Society Reviews* 40, 2494 (2011); [6] K. Yao and Y. M. Liu, "Plasmonic metamaterials", *Nanotechnology Review* 3, 177 (2014); [7] C. L. Zhao et al., "A reconfigurable plasmo-fluidic lens", *Nature Communications* 4:2350 (2013); [8] Z. B. Li et al., "Graphene plasmonic metasurfaces to steer infrared light", *Scientific Reports* 5, 12423 (2015); [9] Z. Wang et al., "Origami-based Reconfigurable Chiral Metamaterials", manuscript under review.

Dr. Yongmin Liu obtained his Ph.D. from the University of California, Berkeley in 2009. He joined the faculty of Northeastern University at Boston in fall 2012 with a joint appointment in the Department of Mechanical & Industrial Engineering and the Department of Electrical & Computer Engineering. Dr. Liu's research interests include nano optics, nanoscale materials and engineering, plasmonics, metamaterials, biophotonics, and nano optomechanics.

He has authored and co-authored over 50 journal papers, including *Science*, *Nature*, *Nature Nanotechnology*, *Nature Communications*, *Physical Re-*

view Letters and Nano Letters. Dr. Liu was a recipient of NSF CAREER Award (2017), Office of Naval Research Young Investigator Award (2016), SPIE DCS Rising Researcher Award (2016), 3M Non-Tenured Faculty Award (2016), Air Force Summer Faculty Fellowship (2015), and Chinese Government Award for Outstanding Students Abroad (2009). Currently he serves as an editorial board member for Scientific Reports, EPJ Applied Metamaterials and Nano Convergence.

This meeting begins at 6:30 PM Thursday, February 9th, 2017 and will be located 3 Forbes Road (an MIT Lincoln Laboratory facility), Lexington, MA, 02420. The meeting is free and open to the public. All are welcome. Prior to the seminar there will

be social time and networking from 6:30 – 7:00PM. Dinner will also be provided. The seminar will begin at 7:00PM. For more information contact Ajay Garg, Boston IEEE Photonics Society Chapter chair at ajay.garg@ll.mit.edu, or visit the Boston IEEE Photonics Society website at www.bostonphotonics.org.

Directions to Forbes Rd Lincoln Laboratory: (from interstate I-95/Route 128)

- Take Exit 30B onto Marrett Rd in Lexington – Merge into left lane
- Make the first Left onto Forbes Rd.
- Proceed straight through the small rotary and enter the parking lot.
- The entrance is on your right, by the flags.



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*Reliability Society – co-sponsoring the SELSE Workshop –
8:00AM, Tuesday, 21 March and Wednesday, 22 March*

The 13th Workshop on Silicon Errors in Logic – Systems Effects

The growing complexity and shrinking geometries of modern manufacturing technologies are making high-density, low-voltage devices increasingly susceptible to the influences of electrical noise, process variation, transistor aging, and the effects of natural radiation. The system-level impact of these errors can be far-reaching. Growing concern about intermittent errors, unstable storage cells, and the effects of aging are influencing system design and failures in memories account for a significant fraction of costly product returns. Emerging logic and memory device technologies introduce several reliability challenges that need to be addressed to make these technologies viable. Finally, reliability is a key issue for large-scale systems, such as those in data centers.

The SELSE workshop provides a forum for discussion of current research and practice in system-level error management. Participants from industry and academia explore both current technologies and future research directions (including nanotechnology). SELSE is soliciting papers that address the system-level effects of errors from a variety of perspectives: architectural, logical, circuit-level, and semiconductor processes. Case studies are also solicited.

Key areas of interest are (but not limited to):

- Technology trends and the impact on error rates.
- New error mitigation techniques.
- Characterizing the overhead and design complexity of error mitigation techniques.
- Case studies describing the tradeoffs analysis for reliable systems.
- Experimental silicon failure data.
- System-level models: derating factors and validation of error models.
- Error handling protocols (higher-level protocols for robust system design).
- Characterization of reliability of systems deployed in the field and mitigation of issues.

Agenda: <http://www.selse.org/>

Meeting Location: Northeastern University, 360 Huntington Avenue, Boston, Massachusetts
Building: Curry Student Center, Building #50 –
Room Number: 2nd Floor Ballroom

Registration link: <http://www.selse.org>



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Join/Renew



Entrepreneurs' Network – 6:00PM, Tuesday, 21 March

Sales Models - Online, Inside, and Field Sales - How and When to Choose a Sales Model for Your Startup

Meeting location – Pivotal Labs, 145 Broadway, 3rd Floor, Cambridge, MA

The ENET meeting on March 21, 2017 is on sales for startup and early stage companies. Our first focus will be to help the founders with the question of how and when to choose a sales model for your startup company. In that early stage the goal should be to start to generate sales as soon as possible, with a minimum viable product. This is the first phase of customer discovery and validation, to establish an impactful value proposition. As Jack Derby (one of our speakers) has written “At the outset, just focus on selling some stuff for the simple purpose of having customers who are paying you money and from whom you can learn the following:

- Why they bought your product
- How they are using those same products
- What do they want to see in the future, so that ...
- You have the ability to work closely with these early customers and determine the financial value that they receive at their companies.

The company will next want to determine a scalable selling platform and a cost-effective sales model. We will then discuss these three major sales models and the experience of our speakers in applying these sales models in early stage companies?

- Online - Products that the customer is able to find, determine if it meets their needs, and purchase on their own are self-procured, usually online.
- Inside - Inside sales is when the sale is completed with the sales person and customer interacting remotely. Driven by technology, inside sales models are being used more frequently in B2B and some higher end B2C transactions.

- Outside - Field sales, or outside sales, are ‘face to face’ customer sales. For higher priced, more complex products, cases where there are numerous stakeholders involved in the purchasing decision, consultative sales, or products that need in person demonstrations – visits with the customer are necessary to seal the deal.

Our three speakers are all sales experts used to developing sales for, and mentoring, early stage companies. They will discuss getting those first sales, and then, successively when, how and what sales model or combination of sales models is right for your startup or early stage company. The panel will be moderated by ENET’s long term chairman who received an IEEE-USA award for contribution to the entrepreneurial community and has been recognized as one of the “Top 20 Boston Startup Attorneys”.



Speaker: Jack Derby is Head Coach and President @ Derby Management, a 25 year old boutique management consulting firm, focuses its expertise in three primary services for its 400+ customers: Business & Strategic Planning; Sales & Marketing Productivity Improvement; Senior Management Development Coaching. www.derbymanagement.com/ He is an active angel investor and past Chairman of Common Angels, rebranded to Converge Venture Partners, where he remains a partner. Jack is also currently a member of eight profit and non-profit Board of Directors including Reiser Inc., where he is Chairman.

In his spare time Jack teaches. He is a Professor of

Marketing at Tufts, where in 2015, he was named “Teacher of the Year” and Lecturer at MIT in Business Planning and Marketing. Jack’s background includes past positions as CEO of Mayer Electronics Corporation, President of CB Sports, President of Litton Industries Medical Systems, CEO of Datamedix Corporation and President of Becton Dickinson Medical Systems, before he formed in 1990, Derby Management. Jack is extremely active in the New England emerging and middle market business communities. Jack has been named to Mass High Tech’s All Star Team. Jack has been the Founder or Co-founder of 12 companies. Jack has also served as Chairman of the Association for Corporate Growth, Chairman of the MIT Enterprise Forum, Vice Chair of the Smaller Business Association of New England, President of the University Club of Boston. Jack is a graduate of Boston College, the University of Chicago and the United States Peace Corps. He divides his time between working in Boston, living and snowboarding in southern Vermont during the winter and living and surfing on the beach in NH whenever he can.



Speaker: Emmanuelle Skala, VP Sales & Customer Success @ DigitalOcean, a cloud infrastructure provider focused on simplifying web infrastructure for software developers.

<https://www.digitalocean.com/> She brings to our panel extensive software startup experience and a proven sales vision that

has been honed over the last 20 years. Prior to Digital Ocean, Emmanuelle was VP Sales at Influitive, where she led sales growing the business 10x in 2yrs. Grew team from 4 to 40. She was responsible for Managed Sales Development, Commercial Sales, Enterprise Sales, Account Management and Sales Ops/Enablement.

Before Influitive, she was VP, Global Channel Sales at Sophos, where she built the company’s global channel organization. In this role, she earned a

number of industry titles, including CRN Channel Chief in 2012 and 2013, and CRN Top 100 Women in the Channel in 2013. Previously, Emmanuelle was also the first salesperson at two B2B technology companies: Endeca, which was acquired by Oracle for more \$1 billion, and Vertica, acquired by Hewlett-Packard Company. In both of these roles, she rapidly built the sales teams and processes that drove revenue growth and company expansion. She is a graduate of Carnegie Mellon, with a BS in Industrial Management, with an MBA from NYU’s Stern School of Business, where she was Co-President of the Entrepreneur Exchange.



Speaker: Mark Ruthfield, Vice President of Sales, Executive Team @t Zaius, which empowers B2C marketers to maximize customer lifetime revenue..

<https://www.zaius.com/> Mark is a Sales Business Leader, Executive Management Team Leader, Corporate Officer with over 20+ years of business experience in leading technology companies in start-up, turn-around, and accelerated growth situations. He is a leader that inspires others in driving record-breaking year-over-year Sales growth results and profitability.

Prior to Zaisu, Mark was Vice President of Sales @ Yesware, where he was Awarded the “2016 Top 25 Most Influential Inside Sales Professionals Prestigious Award” by the American Association of Inside Sales Professionals across the organization’s 10,000+ members with 63 Chapters internationally for the “6th” consecutive year! Previously, he was Vice President of Sales @ ZoomInfo, where he spearheaded the ZoomInfo Sales Dream Team, and more than quadrupled sales over the last 4 years. ZoomInfo’s 2014 revenue results were the highest in company history from a Sales results, year-over-year growth, and profitability standpoint.

Prior to that he had the position New Business Development Sales @Forrester Research. , Mark has

considerable experience working effectively within a start-up environment and building-out scalable sales organizations via repeatable sales processes and best practices. He is the author of a number of publications in the sales field and a frequent speaker at events and webinars to large audiences (hundreds) discussing industry trends and Sales best practices. Mark is an honors graduate of University of Massachusetts at Amherst - Isenberg School of Management



Moderator: Robert Adelson, business and tax attorney, partner at Boston law firm of Engel & Schultz LLP (www.Executive-EmploymentAttorney.com), and Chairman of The Boston Entrepreneurs' Network. Rob has been an attorney for over 30 years specialized in business, tax, stock and options, employment, contracts, financings, trademarks and intellectual property. Rob began as an associate at major New York City law firms before returning home to Boston in 1985 where he has since been a partner in small and medium sized firms before joining his present firm in 2004.

Rob represents entrepreneurs, start-ups and small companies, independent contractors and employees and executives, and family businesses. Rob is a frequent speaker on business law topics and author of numerous articles published in Boston Business Journal, Mass High Tech and other publications. He has been named among the "Top 20 Boston Startup Lawyers" by ChubbyBrain.com, a website that provides tools for entrepreneurs. Rob has been on the ENET Board since 2002 and Chairman since 2009 and is also a Co-Founder and Board member of the 128 Innovation Capital Group. In January 2016, he received the professional achievement award from IEEE-USA for "ex-

treme dedication and contributions to the IEEE entrepreneurship community." He holds degrees from Boston University, B.A., summa cum laude, Northwestern University (Chicago), J.D., Law Review, and New York University, LL.M. in Taxation.

Meeting Location: Pivotal Labs, 145 Broadway, 3rd Floor, Cambridge, MA .

Check for Updates: Boston Entrepreneurs' Network Website at (<http://www.boston-enet.org>)

Refreshments: PIZZA, CHIPS AND SOFT DRINKS WILL BE SERVED AT THE MEETING.

Reservations: ENET meetings are free to ENET members and \$10 for non-members. To expedite sign-in for the meeting, we ask that everyone -- members as well as non-members -- pre-register for the meeting online. Pre-registration is available until midnight the day before the meeting. If you cannot pre-register, you are welcome to register at the door.

Rob represents entrepreneurs, start-ups and small companies, independent contractors and employees and executives, and family businesses. Rob is a frequent speaker on business law topics and author of numerous articles published in Boston Business Journal, Mass High Tech and other publications. He has been named among the "Top 20 Boston Startup Lawyers" by ChubbyBrain.com, a website that provides tools for entrepreneurs. Rob has been on the ENET Board since 2002 and Chairman since 2009 and is also a Co-Founder and Board member of the 128 Innovation Capital Group. In January 2016, he received the professional achievement award from IEEE-USA for "ex-



**Be an
Even Better
Engineer**

Join/Renew



Consultants Networks – 6:30PM, Tuesday, 28 March

How Changing Your Belief System.....Allows New Solutions to Enter Your Consciousness

Stan Sidman, The Business Development Group

Stan Sidman is the founder of The Business Development Group and has been running it for 30 years. His monthly meetings are held at McLane Middleton Law in the Cummings Trade Center - Woburn.

Fascinated by the mind since age 12, Stan went on to become a Certified Hypnotherapist and a Certified Practitioner of NLP (Neuro Linguistic Programming). This was done to enhance the experience participants realize both at his regular meetings as well as those with consulting clients.

Stan's motivation for doing what he does is to help undo the conditioning to which we are all subjected from our early environmental influences. The sad thing he found is the disturbing numbers of participants he has worked with who, even though very bright, are not sensitive to the powerful influences that are still exerting pressures on their daily lives.

Please join us for an "eye opening adventure"..... for those who are open enough to allow conflicting thoughts to enter their consciousness. And yes, a sense of humor and a level of humility is required to benefit from Stan's different approach to training and development, both in business and personally. Feel free to visit his site for more info:
www.Businessdevgrp.com.

PLEASE NOTE: The meeting is open to the public. No charge for Consultants Network members or employees of Constant Contact; \$5 entrance fee for all others. Casual dress. Registration (no regis-

tration required).

Meeting Location: Constant Contact, 1601 Trapelo Road, Waltham, MA 02451

The Consultants Network meeting starts at 6:30 PM. The meeting will take place at Constant Contact, Reservoir Place - 1601 Trapelo Road, Waltham, MA 02451. A no host, PRE-MEETING DINNER will take place at 5:15 PM (sharp) at Bertucci's, 475 Winter Street, Waltham, MA 02451 (exit 27B, Rte 128).

Driving Directions

To Bertucci's:

Follow I-95/route 128 to Winter St in Waltham. Take exit 27B from I-95/Route 128. Turn left on Wyman S, then left on Winter St. Bertucci's is the 1st right after crossing the bridge over I 95/Route128.

To Constant Contact:

Follow I-95/route 128 to Trapelo Rd in North Waltham, Waltham. Take exit 28 from I 95/route 128. Constant Contact is the 1st right after crossing the bridge over I 95/Route128.

Consultants Network meetings generally take place on the fourth Tuesday of each month, but are not held during the summer months. Check the Consultants Network website for meeting details and last-minute information.

**For more information, e-mail or
chairman@boston-consult.com**

2017 IEEE WIE USA EAST FORUM Call for Participation

November 30 – December 2, 2017 Baltimore, MD



Presentation Topics

- Mentoring the next generation of female leaders
- Strategies for increasing equity in power and decision making
- Women as leaders in education, industry, and government
- Development: communication skills in written and spoken word, effective dialog
- Cross-cultural aspects of leadership
- What it takes to be a great leader - qualities that all successful leaders share
- Shaping the future by female leaders
- Training vs inherent skills: can leadership be learned?
- Work-Life balance: family systems traditions and changes
- Leadership development for women: overcoming stereotypes
- The design, implementation, and evaluation of leadership from a structural perspective
- Helping girls and young women become leaders - motivating to empower, empowering to motivate
- Exploring the attrition gap - why do women leave the engineering field and what can be done to prevent it

Not a WIE member?

Our active community of female and male engineers is involved in career building, networking, and community outreach.

Join Now

Submission Deadline

Presentation topic abstract suitable for program (up to 150 words), and extended abstract for evaluation (up to 2 pages) due 24 July 2017.

For more information, visit:

<http://sites.ieee.org/wie-forum-usa-east/calls-for-participation/>



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2017 IEEE MIT Undergraduate Research Technology Conference



Nov 3 - 5, 2017 | Massachusetts Institute of Technology (MIT), Cambridge MA, USA



Call for Submissions

Submission Deadline: June 30th, 2017

Envisioning a technical conference targeted towards undergraduate students all over the globe, the MIT IEEE Student Branch in 2015 inaugurated the IEEE MIT Undergraduate Research Technology Conference. This year we are organizing it again with the goal to make the conference a venue where undergraduate students can meet to present, discuss, and develop solutions advancing technology for humanity. Participants can attend a rich program with renowned speakers, technical sessions, a student design competition, exhibits, networking, and social activities, presenting a great opportunity for students to interact with leading industry experts.

The conference theme is "Meet Innovative Technology", and the six fields of focus are:

1. Machine Learning / Artificial Intelligence (AI)
2. Biological and Biomedical Engineering and Technology (BioEECS)
3. Robotics and Automation Technology
4. Systems and Networking
5. Embedded Technologies
6. Innovative Technologies and Others

Authors may submit content in the form of a technical paper, poster, or lightning talk.

All submissions must be written in English. Paper submissions must be no longer than 4 pages, single-spaced, with a minimum font of 10 point, and submissions may include figures, illustrations, and graphs. Abstract submissions for the poster and lightning talk are limited to 500 words.

All submissions will be peer-reviewed. Submissions are online, with a deadline of June 30th, 2017. Notification of acceptance will be sent via email by August 4th, 2017.

Please join the mailing list (MIT-Conference@ieee.org) for more information and updates on submission, the technical program, registration, and accommodation.

A conference proceeding of all the accepted papers that have been presented at the conference may be published and included in the IEEE Xplore journal. Electronic and online media containing all accepted submissions will be distributed to all registered attendees.

Meet Innovative Technology

Sponsored by MIT IEEE Student Branch and IEEE Boston Section

<http://ieee.scripts.mit.edu/conference>



Software Development for Medical Device Manufacturers *(Online Edition)*



**New
Online
Course**

Students have access to this self-paced course for 90 days!!

Course Description This course provides an introduction to the development of medical device software. The course is comprised of 4 modules that range from 30-45 minutes in duration. The focus is on complying with FDA Design Controls and IEC 62304 requirements.

This course is intended for software developers who are actively involved in developing medical device software.

Module 1

- Medical Device Definitions: FDA and European Union (EU)
- Regulatory Roadmap
- FDA/EU Device Classifications
- FDA QSR Regulation
- FDA Guidance Documents that pertain to medical device software

Module 2

- International Standards that pertain to medical device software
- Types of Software Regulated by FDA
- Quality System basics: Procedures, Work Instructions and Records
- ALL Software is Defective...

Module 3:

- Design Control Overview
- General Requirements
- Design and Development Planning
- Software Development Models
- Design Input
- About Requirements...
- Design Output

- Design Reviews

Module 4:

- Design Control (continued)
- Design Verification
- Software Verification Process
- Testing Overview
- Design Validation
- Software Validation Process
- Design Changes
- Design Transfer
- Design History File
- Course Summary

Speaker Bio:

Steven R. Rakitin has over 40 years experience as a software engineer including 25 years of experience in the medical device industry. He has worked with over 85 medical device manufacturers worldwide, from startups to Fortune 100 corporations. He has written several papers on medical device software risk management as well as a book titled: *Software Verification & Validation for Practitioners and Managers*.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE and a member of MassMEDIC. He is on the Editorial Review Board for the ASQ Journal Software Quality Professional.

As President of Software Quality Consulting Inc., he helps medical device companies comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

<http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/>

Fundamental Mathematics Concepts Relating to Electromagnetics (*Online Edition*)



**New
Online
Course**

Students have access to this self-paced course for 90 days!!

Course Summary This course is designed for people wishing to refresh or to learn the fundamental mathematical concepts that are used to describe electromagnetic wave behavior. The modules address all of the basic math concepts covered in a traditional undergraduate electromagnetics course in an ECE curriculum. These concepts include Vector Basics, Integral Vector Calculus, Differential Vector Calculus, Fundamental Coordinate Systems and Complex Numbers. After completing these modules, a person should have sufficient math skills to pursue graduate studies in electromagnetics and/or be able to decipher the math presented in an upper-level text on the subject.

Target audience: This course is designed for people wishing to refresh or to learn the fundamental mathematical concepts that are used to describe electromagnetic wave behavior.

Course chapters

1. Vector Basics
2. Dot Product
3. Cross Product

4. Contour Integration
5. Vector Algebra
6. Surface Integration
7. Metric Coefficients
8. Coordinate Systems
9. Vector Coordinate Conversion
10. Del Operator and the Gradient
11. The Curl
12. Divergence
13. Stokes Theorem
14. Divergence Theorem
15. Laplacian
16. Complex Numbers

Instructor's Bio:

Dr. Kent Chamberlin is the Chair and a Professor in the Department of Electrical and Computer Engineering. In his more than thirty-five years in academia, he has performed research for more than twenty sponsors, including the National Science Foundation. He has received two Fulbright awards, including the prestigious Fulbright Distinguished Chair, which he served in Aveiro, Portugal. He has also served as an Associate Editor for the Institute for Electrical and Electronics Engineers, and he continues to be active in performing and publishing in a range of research areas.

<http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/>

Reliability Engineering for the Business World *(Online Edition)*



Students have access to this self-paced course for 90 days!!

Course Description

This course is about becoming a leader in reliability engineering. While statistics are the tools of reliability engineering, it takes knowledge not only of these tools but also of the business. Developing knowledge of the business, from sales, engineering, customer service, to supply chain management can determine how effective you can be in improving reliability.

Never take anything for granted, even some rules of thumb in reliability can be misleading, this course will show you how to prove what truly happens in the real world and how to effect change in any part of the business where it is needed. We will explore the balance sheet, organizational structure, customers, service, and high volume manufacturing. It's not just about how often things fail, it is also about where the defect came from, what is the financial effect, the recovery, when should a business take field action, effect of human error, failure analysis/material science, reliability testing, and much more. I will also discuss how you develop executive buy in for change. The course assumes a basic knowledge in reliability statistics. There are 12 sessions that cover the following topics.

Course Outline

Basics – Measurements
Business Model
Design Model (HW and SW)
HALT/RDT/Predictions

Manufacturing Model
Early Life Failures
Wear Out and Mid Life Crisis
Advanced Reliability

Course Objective

To teach you how to become the go to person in your business for objective business sensed reliability answers and requirements.

Instructor's Bio

Kevin is an innovative leader in reliability methodologies with more than 30 years experience in the storage industry. In his latest role as Director of Engineering, he developed a top down reliability/availability management process for design organizations developing mission-critical storage systems. Kevin previously directed the most extensive HALT/HASS operation in the industry, with over 300 chambers worldwide. He has written several papers, consulted with many companies, 3 patents awarded and 2 pending related to systems reliability and test.

His most recent work has been performing system architectural analysis to optimize system availability, serviceability and costs. Providing guidance to development to maximize system reliability and reduce service costs. He has provided consultation to many large companies such as EMC, CISCO, AT+T, HP, Seagate and many others. His position and experience has enabled him to perform extensive field studies and design of experiments. Kevin has developed many

<http://ieeeboston.org/reliability-engineering-business-world-line-course/>

Introduction to Embedded Linux – Part I

(Online Edition)



**New
Online
Course**

Course Summary:

This first of a 2-part series introduces the Linux Operating System and the use of Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part covers the methods for booting Embedded Linux distributions including embedded cross-development and target board considerations.

Who Should Attend:

The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives:

To provide a basic understanding of the Linux OS and the Eclipse IDE framework.

To gain an understanding of the complexities of Embedded Linux Distributions and their use in embedded systems.

To give students confidence to apply these concepts to their next Embedded Linux project

Hardware and Software Requirements

The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ installation or prior knowledge of C-based Makefiles is

useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials

Linux Kernel Development by Robert Love
Linux System Programming by Robert Love
Linux Debugging and Performance Tuning by Steve Best
Optimizing Linux Performance by Phillip G. Ezolt
Embedded Linux Primer by Christopher Hallinan
Pro Linux Embedded Systems by Gene Sally
Embedded Linux Development Using Eclipse by Doug Abbott

Linux Device Drivers by Jonathan Corbet et al
Essential Linux Device Drivers by Sreekrishnan Venkateswaran

Course Downloadable Content:

Video Lecture
Hands-On Lab Instructions
Hands-On Lab Solutions
Additional Related Materials

The Basics

Linux Terminology, History and Versioning
The Linux Community: Desktop & Embedded
The GPL
Linux References (Books and Online)

Getting Started

Kernel Source Code
Building the Kernel
Embedded Linux Kernels
Linux 2.6

Basic Kernel Capabilities

Process and Threads Management

Signals and System Calls
Synchronization, IPC and Error Handling
Timing and Timers
Memory Management and Paging
The I/O Subsystem: A Tale of Two Models
Modularization

Debugging

Process-Level and System-Level Debug
GDB and KGDB
GDB Server and Remote Debugging

An Eclipse Debug Example

Other Debug and Test Tools

Other System-Level Debug Approaches

Process & Threads Management

What are Processes and Threads?
Virtual Memory Mapping
Creating and Managing Processes and Threads
Thread-Specific Data (TSD) POSIX
The Native POSIX Threading Library (NPTL)
Kernel Threads

Signals

System Calls

Scheduling

Linux 2.4 and 2.6 Scheduling Models
The O(1) Scheduler
The Completely Fair Scheduler (CFS)

Synchronization

Via Global Data
Via Semaphores, Files and Signals

Inter-Process Communications (IPC)

Message Queues
Semaphores Revisited
Shared Memory
Pipes, FIFOs and Futexes
Remote Procedure Calls
Networking

Error Handling

errno and perror
strerror and strerror_r
oops, panics and Segmentation Faults

Timing

How Linux Tells Time
Kernel, POSIX and Interval Timers
High-Resolution Timers (HRTs)

Memory Management and Paging

Demand Paging and Virtual Memory
Allocating User and Kernel Memory
Mapping Device Memory
The Slab Allocator
The OOM Killer
Memory in Embedded Systems

Modularization

Creating a Module and Module Loading
Dependency Issues
In Embedded Systems

Shared Libraries

A Shared Library Example
Static and Dynamic Libraries

The I/O Subsystem: A Tale of Two Models

The Original Device Driver Model
The Standard I/O Interface
The New Device Driver Model and Kernel Object
Classes
Initialization
Platform Devices, Busses, Adapters and Drivers
Comparing the Two Models

Embedded Linux Trends

Development, Monitoring and Testing

Some Final Recommendations

Lecturer:

Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at Titera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based development tools, training and consulting for the embedded systems market.

<http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/>

MWSCAS BOSTON USA 2017

60th IEEE International Midwest Symposium on Circuits and Systems

Boston, MA, USA | August 6th-9th, 2017
www.mwscas2017.org

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CALL FOR PAPERS IEEE INTERNATIONAL MWSCAS 2017

The IEEE International Midwest Symposium on Circuits and Systems is the oldest Circuits and Systems Symposium sponsored by IEEE. The 60th edition will be held on the campus of Tufts University, Boston, MA, USA, August 6 - 9, 2017. MWSCAS 2017 will include oral and poster sessions, student paper contest, tutorials given by experts in circuits and systems topics, and special sessions. Topics include, but are not limited to:

Track 1. Analog Circuits and Systems I

- 1.1 Analog Circuits
- 1.2 Analog Systems
- 1.3 Biomedical Electronics
- 1.4 Bioengineering Systems and Bio Chips
- 1.5 Other Analog Circuits and Systems

Track 2. Analog Circuits and Systems II

- 2.1 Linear Analog Systems
- 2.2 Non-Linear Analog Systems
- 2.3 System Architectures
- 2.4 Neuromorphic Systems

Track 3. Digital Circuits and Systems I

- 3.1 Digital Integrated Circuits
- 3.2 System On a Chip (SOC) and Network on a Chip (NOC)

Track 4. Digital Circuits and Systems II

- 4.1 Digital Filters
- 4.2 Hardware-Software Co-Design
- 4.3 Other Digital Circuits and Systems

Track 5. Communications Circuits and Systems

- 5.1 Communications Circuits, Computers and Applications
- 5.2 Communications Systems and Control
- 5.3 Information Theory, Coding and Security
- 5.4 Communications Theory
- 5.5 Other Communications Circuits and Systems

Track 6. RF and Wireless Circuits and Systems

- 6.1 RF Front-End Circuits
- 6.2 Mixed-Signal RF and Analog and Baseline Circuits
- 6.3 Wireless Mobile Circuits and Systems and Connectivity
- 6.4 VCO's and Frequency Multipliers, PLL's and Synthesizers
- 6.5 Other RF and Wireless Circuits and Systems

Track 7. Sensor Circuits and Systems

- 7.1 Technologies for Smart Sensors
- 7.2 Sensor Fusion
- 7.3 Control Systems
- 7.4 Mechatronics and Robotics
- 7.5 Other Sensor Circuits and Systems

Track 8. Converter Circuits and Systems

- 8.1 Analog to Digital Converters
- 8.2 Digital to Analog Converters
- 8.3 DC-DC Converters
- 8.4 Other Converter Circuits and Systems

Track 9. Signal and Image Processing

- 9.1 Analog and Mixed Signal Processing
- 9.2 Digital Signal Processing
- 9.3 Signal Processing Theory and Methods
- 9.4 Image, Video and Multi-Dimensional Signal Processing
- 9.5 Other Signal and Image Processing

Track 10. Hardware Design

- 10.1 Processor and Memory Design
- 10.2 MEMS/NEMS
- 10.3 Nano-Electronics and Technology
- 10.4 Optics and Photonics
- 10.5 Power Management, Power Harvesting and Power Electronics
- 10.6 Photovoltaic Devices/Panels and Energy Harvesting

Track 11. Hardware Security

- 11.1 Hardware Authentication and Physically Unclonable Functions (PUFs)
- 11.2 Trusted Microelectronics
- 11.3 Hardware Anti-Tamper
- 11.4 Architectural System Security
- 11.5 Other Hardware Security

Prospective authors are invited to submit a full paper (4 pages) describing original work. Only electronic submissions will be accepted. Papers should include title, abstract, and topic category from the list above in standard IEEE two-column format for consideration as lecture or poster. Both formats have the same value, and presentation method will be chosen for suitability. All submissions should be made electronically through the MWSCAS 2017 web site (<http://www.mwscas2017.org>). Students are encouraged to participate in the best student paper award contest. Accepted papers will be published in the conference proceedings subject to advance registration of at least one of the authors.

IMPORTANT DATES

March 18: Tutorial and Special Session proposals deadline

March 18: Regular and Student paper submission deadline

April 1: Special session and invited paper submission deadline

April 29: Notice of acceptance

May 20: Final camera-ready paper deadline



www.mwscas2017.org

CALL FOR PAPERS




2017 IEEE High Performance Extreme Computing Conference (HPEC '17)
Twenty-first Annual HPEC Conference

12 - 14 September 2017
 Westin Hotel, Waltham, MA USA



www.ieee-hpec.org

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The IEEE High Performance Extreme Computing Conference (HPEC '17) will be held in the Greater Boston Area, Massachusetts, USA on 12 – 14 September 2017. The HPEC charter is to be the premier conference in the world on the confluence of HPC and Embedded Computing.

The technical committee seeks new presentations that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- Advanced Multicore Software Technologies
- Case Studies and Benchmarking of Applications
- Automated Design Tools
- Mapping and Scheduling of Parallel and Real-Time Applications
- Computing Technologies for Challenging Form Factors
- ASIC and FPGA Advances
- Open System Architectures
- Data Intensive Computing
- Big Data and Distributed Computing
- Interactive and Real-Time Supercomputing
- Graph Analytics and Network Science
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- General Purpose GPU Computing
- Advanced Processor Architectures
- Secure Computing & Anti-Tamper Technologies
- New Application Frontiers
- High Performance Data Analysis
- Cloud HPEC
- Big Data Meets Big Compute

HPEC accepts two types of submissions:

1. Full papers (up to 6 pages, references not included), and
2. Extended abstract (up to 2 pages, references included).

IMPORTANT DATES:

Submission Deadline: **May 19, 2017**

Notification of Acceptance: **June 16, 2017**

Preference will be given to papers with strong, quantitative results, demonstrating novel approaches or describing high quality prototypes. Authors of full papers can mark their preference for a poster display or an oral presentation. Presenters who wish to have hardware demonstrations are encouraged to mark their preference for a poster display. Accepted extended abstracts will be displayed as posters. All paper and extended abstract submissions must use the approved IEEE templates. Full paper submissions with the highest peer review ratings will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions and extended abstracts are published on ieee-hpec.org. Vendors are encouraged to sign up for vendor booths. This will allow vendors to present their HPEC technologies in an interactive atmosphere suitable for product demonstration and promotion.

We welcome input (hpec@ieee-hpec.org) on tutorials, invited talks, special sessions, peer reviewed presentations, and vendor demos. Instructions for submitting will be posted on the conference web site shortly.

Practical Antenna Design for Wireless Products

An intensive Two-day Workshop

Time & Date: 9AM - 4:30PM, Thursday & Friday, June 1 & 2

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speakers: Henry Lau, Lexiwave Technology

INTRODUCTION

To stay competitive in today's fast evolving business environment, faster time to market is necessary for wireless communication products. Playing a critical role in determining the communication range of products, RF design, particularly the antenna design, becomes crucial to the success of the introduction of new wireless products. Competence in advanced antenna designs can definitely strengthen the competitive edge of RF product design or manufacturing companies.

COURSE OBJECTIVES

This 2-day course aims to provide participants with technical insights on the vital aspects of antenna design from a practical and industrial perspective. It covers the fundamental antenna concepts and definitions, specifications and performance of different types of commonly-used and advanced antennas in RF products. Simulation tools will be introduced and discussed. Practical implementation strategies in RF products for optimum antenna performance will also be presented.

WHO SHOULD ATTEND

Antenna designers, RF designers, wireless product designers, field application engineers, business development engineers and managers, design managers, and related professionals.

OUTLINE

Day 1 (1 June)

Fundamental Concepts

1. Antenna Fundamental

- * Basic types of Antenna
- * Dipole, Monopole, helical, loop, printed PCB
- * Radiation Mechanism
- * Source of radiation
- * Characteristics of radiation

2. Specification and Performance

- * Radiation pattern
- * Antenna efficiency, aperture
- * Impedance and circuit matching
- * Directivity, gain
- * Friis Transmission Equation

3. Antenna Elements

- * Dipole antenna
- * Monopole antenna
- * Multi-band antenna
- * Miniature chip type antenna
- * Loop antenna

Day 2 (2 June)

Advanced Antenna Elements

4. Miniature antenna for portable electronics

- * Patch, inverted-L, inverted-F
- * Meandered line, multi-band

5. CAD Design and Simulation

- * CAD tools

- * Design strategies
- * Limitations
- * Case studies

Practical implementation strategies

6. How to design good antennas

- * Understand the requirements
- * Selection of antenna type, size and geometry
- * Location and placement

7. Team work with product designers, electronic engineers and mechanical engineers

- * Why it matters
- * Case studies on designing good antennas

EXPERTISE

Henry Lau received his M.Sc. and MBA degrees from UK and USA respectively. He has more than 26 years of experience in designing RF systems, products and RFICs in both Hong Kong and US.

He worked for Motorola and Conexant in US as Principal Engineer on developing RFICs for cellular phone and silicon tuner applications. Mr Lau holds five patents all in RF designs. He is currently running Lexiwave Technology, a fables semiconductor company in Hong Kong and US designing and selling RFICs, RF modules and RF solutions. He has also been teaching numerous RF-related courses internationally.

**Decision (Run/Cancel) Date for this Course is
Monday, May 22, 2017**

Payment received by May 17

IEEE Members	\$405
Non-members	\$435

Payment received after May 17

IEEE Members	\$435
Non-members	\$455

<http://ieeeboston.org/practical-antenna-design-wireless-products/>

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Contact Kevin Flavin or 978-733-0003 for more information on rates for Print and Online Advertising

Simulink Model based FPGA Digital Design and Digital Signal Processing

Time & Date: **Course postponed until fall 2017**

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speakers: Cherif Chibane, Rick Rosson; MIT Lincoln Laboratory

Description:

Over the last 30 years, applications for Field Programmable Gate Array (FPGA) designs have increased exponentially. FPGA's have moved from just digital designs to other areas such as embedded controllers, Digital Signal Processing, communication systems, and configurable computing. This has made exposure to and mastery of FPGA design crucially important for many people in industry and academia.

This course provides a detailed overview of FPGA technologies, a top-down design workflow, modeling and simulation, standard design tools, and applications. Using a mixture of theory and hands-on laboratories, the course provides students what they need to know in modeling, simulation, design, verification, and implementation of multi-disciplinary applications targeting FPGA's. This course provides plenty of hands-on lab exercises to reinforce the key concepts. While the material covered in this class targets Xilinx devices, it can be easily used for others devices such as ALTERA and other FPGA devices.

Presenters:

This course will be jointly presented by Cherif Chibane and Rick Rosson of MIL Lincoln laboratory. Their combined and complementary expertise will greatly benefit attendees from industry and academia.

Cherif Chibane is currently with MIT Lincoln laboratory as a research staff. He was one of the early adopters of FPGA's for configurable computing. Prior to MIT-LL, he was part of the BAE Systems team that pioneered the use FPGA's for Software Denied Radio (SDR). He has more than 25 years in the design of advanced configurable computing using FPGA's for DSP, digital logic, and embedded designs.

Rick Rosson is a senior modeling and simulation engineer at MIT Lincoln Laboratory. Prior to joining MIT-LL, Rick served as a senior applications engineer at MathWorks for 9 years, with a focus on digital signal processing, statistical signal processing, embedded systems design, modeling and simulation, and data analysis and visualization. Rick holds a Master of Science in Electrical Engineering from Boston University and a Master of Science in Management from the MIT Sloan School of Management.

Agenda

Session #1

- Course Overview
- Model based benefits in today's FPGA designs.
- Simulink/Matlab Overview
- Simulink Examples

Session #2

- FPGA Technologies Overview
- Xilinx ISE Overview
- Fixed point Vs floating point overview
- HDL/FPGA Examples

Session #3

- Preparing Simulink models for HDL code generation
- Generating HDL code from Simulink
- Verifying the generated code
- Code Generation Examples

Session #4

- Modeling Signal Processing and Communications Systems in Simulink®
- Signal Processing Examples
- Implementing Signal Processing Systems on FPGA's

Session #5

- Advanced Topics using FPGA's
- End-To-End Design and Verification
- End-To-End Design Example
- Course Summary

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

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If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is

<http://ieeeboston.org/course-proposals/> .

Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course)
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Software Development for Medical Device Manufacturers

An intensive Two-day Workshop

Time & Date: 8:30AM - 4:30PM, Wednesday & Thursday, April 5 & 6, 2017

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speakers: Steve Rakitin, President, Software Quality Consulting, Inc.

OVERVIEW:

Developing software in compliance with FDA, EU regulations and international standards is challenging. This two-day intensive course provides practical guidance and suggestions for developing software that complies with applicable FDA and EU regulations, guidance documents and international standards such as IEC 62304 and ISO 14971. The focus of this course is interpreting Design Controls for software. Each section of the Design Controls regulation (820.30) is discussed from the software perspective. Corresponding requirements from IEC 62304 are woven into the flow.

In-depth discussion of critical topics such as Requirements, Software Verification & Validation, Risk Management and Fault Tree Analysis are included. In addition, techniques for validating software development tools and software used in Manufacturing and Quality Systems are also discussed. Interactive group exercises are included to facilitate discussion and learning.

WHO SHOULD ATTEND

Software and firmware engineers, software managers, RA/QA staff, validation engineers, and project managers. Anyone interested in learning how to develop medical device software in compliance with regulations, standards and guidance documents.

COURSE OUTLINE

• Introduction

Medical Device Definitions – FDA and EU
Regulatory Roadmap and FDA/EU Device
Classification Schemes
FDA Regulations and Guidance Documents
for Software
Standards – ISO 13485, IEC 62304, ISO
14971, EN-14971, IEC 60601, and
IEC 62366-1
All Software is Defective

• Interpreting Design Controls for Software

Software Development Models
Design and Development Planning
Design Inputs
• **About Requirements...**
• **Requirements Exercise**
Design Outputs
Design Reviews
Design Verification
• Software Verification Techniques
Design Validation
• Software Validation Process
Design Transfer
Design Changes
Design History File

- **Validation of...**

- Software Tools used to develop Medical Device Software
 - Software used in Manufacturing
 - Software used in Quality Systems

- **Risk Management**

- Standards and Regulations
 - Terms and Concepts
 - Risk Management Process
 - Risk Management Tools and Techniques

- **Fault Tree Exercise**

- Data Collection and Analysis
 - Documentation Requirements

- **Summary**

- **Comprehensive reference materials included**

Speaker Bio:

Steven R. Rakitin has over 40 years experience as a software engineer including 25 years of experience in the medical device industry. He has worked with over 85 medical device manufacturers worldwide, from startups to Fortune 100 corporations. He has written several papers on medical device software risk management as well as a book titled:

Software Verification & Validation for Practitioners and Managers.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE and a member of MassMEDIC. He is on the Editorial Review Board for the ASQ Journal Software Quality Professional.

As President of Software Quality Consulting Inc., he helps medical device companies comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

Decision (Run/Cancel) Date for this Course is Friday, March 24, 2017

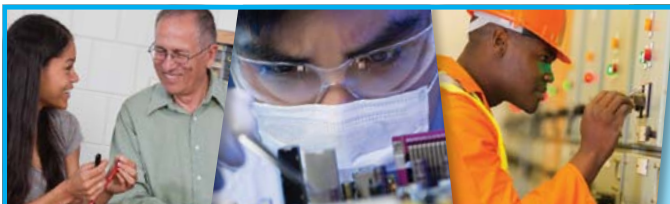
Payment received by March 20

IEEE Members	\$465
Non-members	\$495

Payment received after March 20

IEEE Members	\$495
Non-members	\$545

<http://ieeeboston.org/software-development-medical-device-manufacturers-intensive-two-day-workshop/>



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Last Notice Before Course Begins, Please Register now and Save \$\$\$!!!

More Digital Signal Processing (DSP) for Wireless Communications

Time and Dates: 6 - 9PM, Wednesdays, March 22, 29, April 5, 12, 26

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Dan Boschen, Microsemi

Course Summary

This course is a continuation of the IEEE course "DSP for Wireless Communications" also taught by Dan Boschen, detailing digital signal processing most applicable to practical real world problems and applications in radio communication systems. Students need not have taken the Part I course if they are familiar with basic DSP concepts.

This course brings together core DSP concepts to address signal processing challenges encountered in radios and modems for modern wireless communications. Specific areas covered include carrier and timing recovery, equalization, automatic gain control, and considerations to mitigate the effects of RF and channel distortions such as multipath, phase noise and amplitude/phase offsets.

Dan builds an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real world applications for mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges, rather than a tutorial on implementations with DSP processors.

Target Audience:

All engineers involved in or interested in signal processing for wireless communications. Students should have either taken the first part of this course "DSP for Wireless Communications" or have been sufficiently exposed to basic signal processing concepts such as Fourier, Laplace, and Z-transforms,

Digital filter (FIR/IIR) structures, and representation of complex digital and analog signals in the time and frequency domains. Please contact Dan at boschen@loglin.com if you are uncertain about your background or if you would like more information on the course.

Benefits of Attending/ Goals of Course:

Attendees will gain a strong intuitive understanding of the practical and common signal processing implementations found in modern radio and modem architectures and be able to apply these concepts directly to communications system design.

Topics / Schedule:

Class 1:

DSP Review, Radio Architectures, Transforms, Mapping to Digital, Pulse Shaping, Eye Diagrams

Class 2:

ADC Receiver, CORDIC Rotator, Digital Down Converters, Numerically Controlled Oscillators

Class 3:

Digital Control Loops; Output Power Control, Automatic Gain Control

Class 4:

Digital Control Loops; Carrier and Timing Recovery, Sigma Delta Converters

Class 5:

RF Signal Impairments, Equalization and Compensation, Linear Feedback Shift Registers

Speaker's Bio:

Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 20 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems. Dan is currently at Microsemi (formerly Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page at:

<http://www.linkedin.com/in/danboschen>

**Decision (Run/Cancel) Date for this Course is
Monday, March 13, 2017**

Payment received by March 9

IEEE Members \$325

Non-members \$360

Payment received after March 9

IEEE Members \$360

Non-members \$425

<http://ieeeboston.org/digital-signal-processing-dsp-wireless-communications-2/>

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**2017 IEEE International Symposium on
Technologies for Homeland Security**
April 25 - 26, 2017
www.ieee-hst.org
(The technical program, conference
registration is now online)

**2017 IEEE International Midwest
Symposium on Circuits and Systems**
August 6 - 9, 2017
www.MWSCAS2017.org
(Call for Papers Deadline,
March 10, 2017)

**2017 IEEE High Performance Extreme
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Submission deadline is
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- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Course Begins Monday, Please Register now and Save \$\$\$!!!

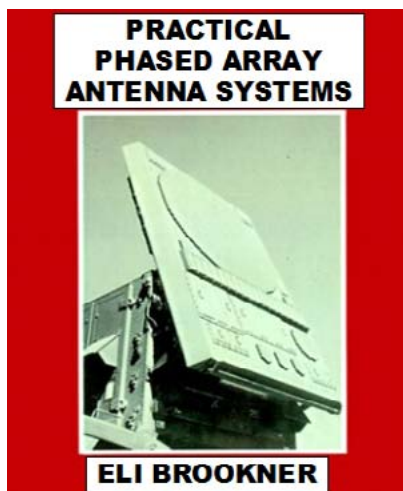
Phased-Array and Adaptive-Array Fundamentals and Their Recent Advances

Time & Date: 6 - 9PM, Mondays, Feb. 27, March 6,13, 20, 27, April 3, 10, 24, May 1, 15
(Snow/make-up days May 22, June 5, 12)

Location: MITRE Corp., 202 Burlington Rd., Bedford, MA (tentative)

Speaker: Dr. Eli Brookner, Raytheon, (Retired)

Text: "Practical Phased Array Antenna Systems", Dr. Eli Brookner
(included with registration)



"Practical Phased Array Antenna Systems", Dr. Eli Brookner, Editor, Artech House, 1991, Hardcover, 258 pages, List Price \$179, Hardcover, 258 pages. Covers array fundamentals: phase and time-delay steering; grating lobes for 1- and 2-dimensional arrays; effects of errors and failures on gain, sidelobes and angle accuracy; array weighting, thinning, blindness, mutual coupling, elements, phase-shifters and feeds; limited field of view (LFOV) arrays; SPY-1; example design.

This course is based on the book entitled Practical Phased Array Antenna Systems by Dr. Eli Brookner. The book covers array basics and fundamentals which do not change with time. The course, the book and the notes will provide an ideal introduction to the principles of phased array antenna design and adaptive arrays. The course material and notes cover in addition recent developments in phased arrays updated to 2017.

With the explicitly tutorial approach the course and book offers a concise, introductory-level survey of the fundamentals without dwelling on extensive mathematical derivations or abstruse theory. Instead a physical feel will be given. The book

provides extensive curves, tables and illustrative examples. Covered in easy terms will be sidelobe cancellation, full adaptive array processing without suffering its computation complexity (through the use of adaptive-adaptive array processing also called beam-space processing and eigenbeam processing). Finally, Space-Time Adaptive Array (STAP) for airborne platforms will be explained and related to the displaced phase center antenna (DPCA).

All Attendees of the class will receive trial trial license of MATLAB and Phased Array System Toolbox from MathWorks in addition to a set of examples which help demonstrate key array concepts covered in the course.

This course is intended for the engineer or scientist not familiar with phased-array antennas as well as the antenna specialist who wants to learn about other aspects of phased-array antenna systems as well as get the latest developments in array systems, such as: MIMO, metamaterial arrays, Extreme MMIC arrays, stealthing and cloaking. The major emphasis will be on the system aspects of phased-arrays.

Lecture #1. Monday February 27; Phased Array Fundamentals: Electronically Scanned Array (ESA) explained with tube COBRA DANE used as example. Covered will be: Near and Far Field Definitions, Phased Steering, Switched-Line Phase Steering, Time Delay Steering, Sub-

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US ARMY FIELDING TO 2048

- >200 BUILT, 13 NATIONS
- 5000 EL PER/FACE, C-BAND

(FEB. 19, 2015/PRNEWSWIR1520E;
MICROWAVE&RF, AUG 2015, P. 24;
RAYTHEON WEBSITE)



(SEE: BROOKNER, E., MJ,2/15)

arraying, Array Weighting, Monopulse, Duplexing, Array Thinning, Embedded Element, dual polarized circular waveguide element, advantage of triangular lattice over square lattice, Tour of COBRA DANE (6 stories high) via color slides.

Lecture #2. Monday March 6; Linear Array Fundamentals: Conditions for no grating lobes; beam-width vs scan angle; sine space; Array Factor; sidelobe level vs antenna beamwidth; directivity; antenna efficiency factors; array weightings; array frequency scanning; array bandwidth.

Lecture #3. Monday March 13; Planar Arrays: Array Factor; array separability; sine-space ($\sin\alpha$ space, T -space); grating lobes location for triangular and rectangular lattice; directivity; very useful bell curve approximation; array thinning system issues.

Lecture #4. Monday March 20; Array Errors:

AIR & MISSILE DEFENSE RADAR (AMDR)

S-BAND: AIR & MISSILE DEFENSE:

- ADAPTIVE DIGITAL BEAM FORMING
- 30X > TARGETS THAN SPY-1D(V)
- 30X > SENSITIVE THAN SPY-1D(V)
- RADAR MODULAR ASSEMBLIES (RAMs) ARE BUILDING BLOCKS
- LRU IN RAM REPLACED <6MIN, EASY, ONLY 2 TOOLS NEEDED
- 37 RAMs = SPY-1D(V)+15DB
- = ~14'x14' ≈ SIZE OF SPY-1D(V)
- GaN ARRAY, 4 FACED
- GaN 34% < \$ THAN GaAs
- GaN HAS 10⁸ HR MTBF
- RAYTHEON INVESTED \$150M IN GaN
- SCALABLE



ARLEIGH BURKE
DESTROYER

X-BAND: HORIZON SEARCH

(WIKIPEDIA PHOTO)

Effects of element phase and amplitude element errors and element failures; simple physical derivation of error effects; paired echo theory; subarray errors; quantization errors; examples.

Lecture #5. Monday March 27; Radiating Elements: Waveguide; dipole; slotted waveguide; microstrip patch; stacked patch; notch (wideband); spiral; matching (wide-angle); waveguide simulator; practical limitations, mutual coupling and array blindness; scattering matrix; design procedure; polarization mismatch loss.

X-BAND 25K ELEMENT AESA AN/TPY-2



8 DELIVERED, 3 MORE ON ORDER.

PHOTO COURTESY RAYTHEON

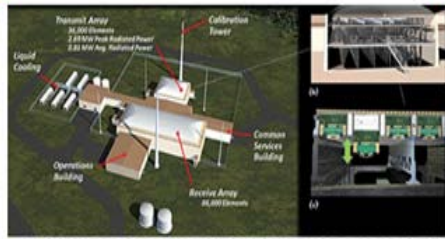
Lecture #6. Monday April 3; Active Phased Arrays: 2nd

generation solid state hybrid active electronically scanned array (AESAs) covered using PAVE PAWS as example, T/R Module Introduced, Cross Bent Dipole Element, Mutual Coupling, Array Blindness, Tour of PAVE PAWS (6 stories) via color slides. 3rd Generation AESAs: THAAD (TPY-2), SPY-3, IRIDIUM, F-15 APQ-63(V)2, APG-79, XBR, AMDR and upgraded Patriot; GaAs and GaN microwave integrated circuits (Monolithic Microwave Integrated Circuit, MMIC).

Lecture #7. Monday April 10; Array Feeds: Corporate and space fed; Reactive (lossless) and matched (Wilkinson); even/odd node analysis. Se-

rial; Ladder; Lopez; Blass; Radial, Butler matrix; microstrip/stripline; Rotman Lens; SLQ-32; PATRIOT space-fed array; reflectarray.

LM NEW SPACE FENCE RADAR USES DBF AT ELEMENT ON RECEIVE - 172,000 CHANNELS



a.) LOCKHEED MARTIN (LM) SPACE FENCE RADAR SITE, b.) CUTAWAY OF TRANSMIT ARRAY, c.) CROSS-SECTION OF RADAR-ON-A-BOARD TRANSMIT LRUs (MICROWAVE J. SEPT-2016: [HTTP://WWW.MICROWAVEJOURNAL.COM/ARTICLES/26872V](http://www.microwavejournal.com/articles/26872v))

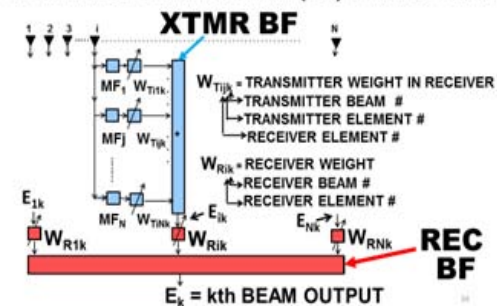
figure and system temperature taking into account array mismatch.

Phase Shifters: Diode switched-line, hybrid-coupled, loaded-line; ferrite phase-shifters: non-reciprocal latching; diode vs ferrite; MEMS (Micro-Electro-Mechanical Systems) and its potential for a low cost ESA.

Lecture #8. Monday April 24; Limited Scan (Limited Field of View [LFOV]) Arrays: Explained using simple high school optics for TPS-25, 1st Electronically Scanned Array (ESA) put in production. Fundamental Theorem specifying minimum number of phase shifters needed for a specified scan angle. Method for realizing this minimum using overlapped array antenna elements as with HIPSAF lens array system and Microwave

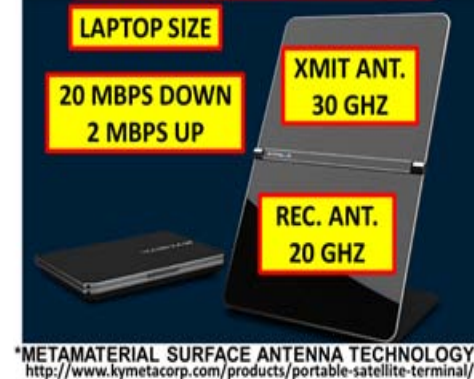
MIMO MONOSTATIC ARRAY

XTMR/REC BEAMFORMER (BF) IN RECEIVER



Landing System (MLS); reflector; randomized oversized elements; LFOV using sum and difference patterns; use of spatial filters to reduce grating lobes and sidelobes. Hemispherical Coverage Dome Antenna.

Lecture #9. Monday May 1; Phased Array Amazing Advances and Breakthroughs --



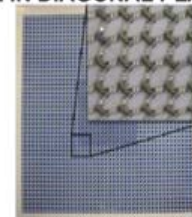
Part 1: SYS-TEMS: Patriot now has GaN active electronically scanned array (AESA) providing 360o coverage, now a 2015 state-of-the-art AESA radar system; S-band AMDR provides 30 times the sensitivity and number of tracks as SPY-1D(V); 3, 4, 6 faced "Aegis" radar systems developed by China, Japan, Australia, Netherlands, USA;

EXTREME MMIC: can now put on single chip 256-Element

TIGHTLY COUPLED DIPOLE ARRAY (TCDA)

- BANDWIDTH: 1:20
- THICKNESS: $\lambda/40$ AT LOWEST FREQ.
- DUAL POLARIZATION
- COLOCATED PHASE CENTERS
- GOOD POARIZATION IN DIAGONAL PLANE
- WAIM STRUCTURE

(RAYTHEON TECHNOLOGY TODAY, 2014, ISSUE 1)



60 GHz Transmit Phased Array, such arrays may be used for the internet-of-things and in cell phones which by 2020 is expected to number 50 billion, expect such single chip arrays to cost only few dollars in future; All the RF circuitry for mm-wave automobile radars being put on a chip, in future such radars could be produced for just a few dollars; Valeo Raytheon (now Valeo Radar) developed low cost, \$100s, car 25 GHz 7 beam phased array radar; ~2 million sold. LOW COST PACKAGING: Raytheon, Rockwell Collins, Lincoln-Lab./MA-COM and South Korea developing low cost flat panel S and X-band AESAs using commercial components, practices and printed circuit boards (PCBs); DIGITAL BEAM FORMING (DBF): Israel, Thales, Australia and Lockheed Martin(LM) have under

development array with an A/D for every element channel (LM array has 172,000 channels and A/Ds); Raytheon developing mixer-less direct RF A/D having >400 MHz instantaneous bandwidth, reconfigurable between S and X-band.

MOORE'S LAW: Not dead yet; Slowed down but has much more to go; potential advance via: graphene, spintronics, memristors, synaptic transistors and quantum computing.

MATERIALS: GaN can now put 5X to 10X the power of GaAs in same footprint, 38% less costly, 100 million hr MTBF, Raytheon invested \$200 million to develop GaN.

METAMATERIALS: Material custom made (not found in nature): 20 and 30 GHz metamaterial electronically steered antennas demonstrated December 2013 transmission to satellites and back, goal is \$1K per antenna, how this antenna works explained for first time; 2-20GHz stealthing by absorption simulated using <1 mm coating; target made invisible over 50% bandwidth at L-band using fractals; Focus 6X beyond diffraction limit at 0.38 μm ; 40X diffraction limit, $\lambda/80$, at 375 MHz; In cell phones provides antennas 5X smaller ($1/10\text{th } \lambda$) having 700 MHz-2.7 GHz bandwidth; The Army Research Laboratory in Adelphi MD has funded the development of a low profile metamaterial 250-505 MHz antenna having a $\lambda/20$ thickness; Provides isolation between antennas with 2.5 cm separation equivalent to 1 m separation; used for phased array WAIM.

Sidelobe Cancellers (SLC): The simple single-loop, feed-forward canceller is introduced in easy phys-

ical terms. This is followed by a discussion of the simple single-loop feedback canceller with and without hard limiting. The normalized feedback SLC will also be covered. Next the multiple-loop SLC (MSLC) will be covered. Applied to the MSLC will be the Gram-Schmidt, Givens and Householder orthonormal transformation methods. Systolic array implementations will be given.

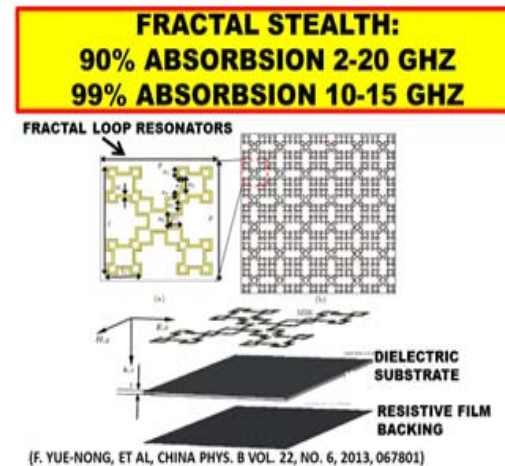
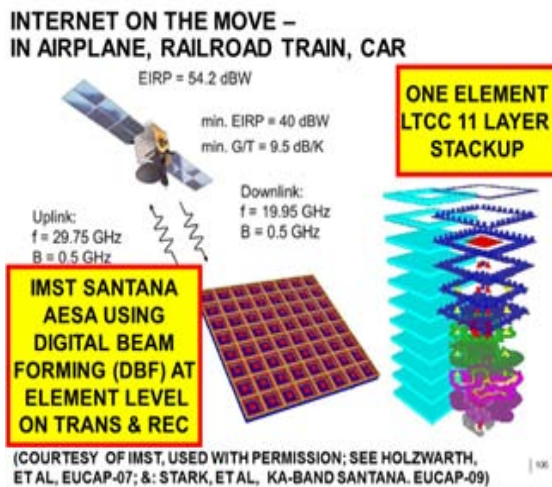
Lecture #10. Monday May 15; Fully Adaptive

Arrays: The optimum weight for a fully adaptive array is developed using a very simple derivation. Methods for calculating this optimum weight are given using the Sample Matrix Inversion (SMI) algorithm, the Applebaum-How-

ells adaptive feedback loop method, a recursive method, and Gram-Schmidt, Givens and Householder orthonormal transformations developed for the tracking problem and for the MSLC. The use of eigenvector beams and a whitening filter will also be developed. It will be shown how the latter reduces the transient response. Methods for obtaining the benefits of a fully adaptive array without its high computation and large transient time disadvantages are given. These are the adaptive-adaptive array processing procedures, the use of eigenbeam space, and the method of finding the largest eigenvectors and in turn their eigenbeams. The STAP algorithm covered.

Phased Array Amazing Advances and Breakthroughs --

Part 2: NEW MIMO (MULTIPLE INPUT MULTIPLE OUTPUT) ARRAYS: Explained in simple physical terms rather than with heavy math. Gives attendees an understanding of where it makes sense to



use. Contrary to what is claimed MIMO array radars do not provide 1, 2 or 3 orders of magnitude better resolution and accuracy than conventional array radars; also contrary to claims made MIMO should not provide better minimum detectable velocity for airborne radars.

MIMO and JAMMING: MIMO does not provide better barrage-noise-jammer, repeater-jammer or hot-clutter rejection than conventional array radars. SAR/ISAR: Principal Components of matrix formed from prominent scatterers track history used to determine target unknown motion and thus compensate for it to provide focused ISAR image. Technology and Algorithms: A dual polarized, low profile, ($\square/40$), wideband (1:20) antenna can be built using tightly coupled dipole antennas (TCDA); Lincoln Lab increases spurious free dynamic range of receiver plus A/D by 40 dB; MEMS: Has potential to reduce the T/R module count in an array by a factor of 2 to 4; Can provide microwave filters tunable from 8-12 GHz that are 200 MHz wide;

LOW COST PRINTED ELECTRONICS: 1.6 GHz printed diodes achieved (goal 2.4 GHz).

ELECTRICAL AND OPTICAL SIGNALS ON SAME CHIP: Will allow data transfer at the speed of light; IR transparent in silicon.

BIODEGRADABLE ARRAYS OF TRANSISTORS OR LEDS: Imbedded under skin for detecting cancer or low glucose.

QUANTUM RADAR: Has potential to defeat stealth targets.

NEW POLARIZATIONS: OAMS, (ORBITAL ANGU-

LAR MOMENTUM) unlimited data rate over finite band using new polarizations??

Your Registration Includes: 1 textbook; 15 Reprints; over 800 Vugraphs; trial license of MATLAB and Phased Array System Toolbox from MathWorks with examples demonstrating key array concepts covered in the course.

Your Registration Includes:

- **1 textbook**
- **15 Reprints**
- **over 800 Vugraphs**
- **trial license of MATLAB and Phased Array System Toolbox from MathWorks with examples demonstrating key array concepts covered in the course.**

**Decision (Run/Cancel) Date for this Course is
Monday, February 20, 2017**

Payment received by February 15

IEEE Members	\$300
Non-members	\$340

Payment received after February 15

IEEE Members	\$340
Non-members	\$370

<http://ieeeboston.org/phased-array-adaptive-array-fundamentals-recent-advances/>

Locally held IEEE Conferences

2017 IEEE International Symposium on
Technologies for Homeland Security
April 25 - 26, 2017
www.ieee-hst.org
(The technical program, conference
registration is now online)

2017 IEEE International Midwest
Symposium on Circuits and Systems
August 6 - 9, 2017
www.MWSCAS2017.org
(Call for Papers Deadline,
March 10, 2017)

2017 IEEE High Performance Extreme
Computing Conference HPEC '17
September 12 - 14, 2017
www.ieee-hpec.org
Submission deadline is
May 19, 2017

QA and Testing in DevOps Automation

Time & Date: 8AM - 5PM, Thursday, April 20 **(Please note new date!!!)**
Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA
Speaker: Rajkumar Joghee Bhojan, Wipro Technologies

Introduction: In most of the IT organizations, there are hundreds of applications are getting deployed per release. Currently, Agile projects release cycle duration is reduced dramatically. In this “Fail Fast” environment, choosing right test automation tool and its framework becomes imperative for delivering quality software. This day-long course (lecture/lab) will address the following questions: How to create new ways of adopting QA and testing in their core software? Are we able to deliver better product using existing testing methodologies?

Format: lecture/lab

Topics

- Comprehend the need of automated testing.
- Employ TestNG and Eclipse to execute and write tests.
- Develop a group of test classes with the use of WebDriver.
- Building POM framework
- Running Tests in Parallel
- Understanding how to use Jenkins and GitHub for Selenium Tests
- Design tests to minimize code using inheritance

Target Audience: IT Professionals, Students both UG and PG with Computer Knowledge and Researchers

Benefits of Attending the Course:

- Learning recent technologies in Test Automation space.
- Will get knowledge of Selenium and its techniques in trending technologies
- * **Gain Hands-on experience in Selenium WD.**
- Latest technologies used in Software Testing

- Participants can directly implement the taught methodologies in their software projects

Speaker Bio: Rajkumar J.Bhojan is a Test Architect (TA), Wipro Technologies, Quincy, MA, USA. He has over two decades of professional experience in both IT and Academics. He holds M.Sc., (Phy), MCA, and M.Phil (CS). He has executed IT projects in diverse geographies including India, Australia & USA. He has worked as a QA Manager, Scrum Master, Corporate Trainer and Principal Consultant in reputed organizations. He has presented many technical papers at International conferences, Journals, IEEE forums and Google Tech Talks. He is a Certified Scrum Master and has rich experience in Agile/scrum Methodologies. He is a member in IEEE and ACM.

http://sites.ieee.org/sem/files/2013/07/May_2014-WL_Rev1.pdf

<http://www.atagg.agiletestingalliance.org/speakers.html>. <http://princetonacm.acm.org/tcfpro/>

He also spoke at Google Tech Talks (GTAC-2016). <https://www.youtube.com/watch?v=RfQi5PNO4L8>.

Course Materials, PPT - deck, Working notes and Sample Scripts.

Decision (Run/Cancel) Date for this Course is Wednesday, April 12, 2017

Payment received by April 10

IEEE Members \$230

Non-members \$255

Payment received after April 10

IEEE Members \$255

Non-members \$275

<http://ieeeboston.org/qa-testing-devops-automation/>

Call for Articles

Now that the Reflector is all electronic, we are expanding the content the publication. One of the new features we will be adding are technical and professional development articles of interest to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional articles will be reviewed by the publications committee for suitability. The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to;
ieeebostonsection@gmail.com

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Contact Kevin Flavin or 978-733-0003 for more information on rates for Print and Online Advertising

Advanced Embedded Linux Optimization

Time & Date: 6 - 9PM, Wednesdays, May 10, 17, 24, 31

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand debugging, profiling and testing high performance Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.
- To give students the confidence to apply these concepts to their next Embedded Linux project.

Course Schedule Day 1

Getting Started with Embedded Linux
 Embedded Linux Training Overview
 Terminology
 Linux Versioning
 The GPL
 Building the Kernel Source Code
 Embedded Linux Kernels
 BSPs and SDKs
 Linux References (Books and Online)
 A Development Cycle Focused on Performance
 A Basic Optimization Process
Basic Debugging Review
 Embedded Applications Debug
 GDB, GDB Server and the GDB Server Debugger
 Other Debuggers
 An Eclipse Remote Debug Example
 Debugging with printk, syslog, syslogd and LTTng
System-Level Debug
 System-Level Debug Tools
 The /proc and /sys Filesystems
 Basic Logging
 KDB and KGDB
 Crash Dumps and Post-Mortem Debugging
Debugging Embedded Linux Systems
 Backend Debuggers
 In-Circuit Emulators
 Hardware Simulators
 Analyzers

Course Schedule Day 2

Requirements Development
 Performance Requirements
 Derived Requirements

Testability and Traceability

Reviewing Requirements

Designing for Performance

Design for Test (DFT)

Agile Software Design

Software and Linux Decomposition

Memory Management

CPU and OS Partitioning

Design Reviews

Coding for Performance

Coding Standards and Consistency

Languages, Libraries and Open Source

Components

Learning Magic Numbers

Letting Compilers Work For You

Global, Static and Local Variables

Code Reviews

Software Testing

Unit-Level Testing

System-Level Testing

Code Coverage Tools

gcov

Automated Testing

Some Embedded Linux Test Recommendations

DebugFS

Configuring DebugFS

DebugFS Capabilities

Advanced Logging

LogFS

Using Logwatch and Swatch

Using syslogd and syslog-ng

Tracing

ptrace and strace

New Tracing Methods

SystemTap

Ftrace, Tracepoints and Event Tracing

Tracehooks and utrace

Profiling

Basic Profiling

gprof and Oprofile

Performance Counters

LTTng

Another DDD Example

Manual Profiling

Instrumenting Code

Output Profiling

Timestamping

Course Schedule Day 3

Addressing Performance Problems

Types of Performance Problems

Using Performance Tools to Find Areas for Improvement

Application and System Optimization

CPU Usage Optimization

Memory Usage Optimization

Disk I/O and Filesystem Usage Optimization

Measuring Embedded Linux Performance

Some Ideas on Performance Measurement

Common Considerations

Uncommon Considerations

Using JTAG Methods

BootLoader Measurements

Boot Time Measurements

The Perf Tool

Origins of Perf

The Perf Framework

Perf Commands and Using Perf

Listing Events

Counting Events

Profiling with Perf

Static Tracing with Perf

Dynamic Tracing with Perf

Perf Reporting

Performance Tool Assistance

Recording Commands and Performance

System Error Messages and Event Logging

Dynamic Probes

Jprobes and Return Probes

Kernel Probes

Kexec and Kdump

Improving Boot Performance

Boot Time Optimization

The Linux Fastboot Capability

Building a Smaller Linux

Building a Smaller Application

Filesystem Tips and Tricks

Some Notes on Library Usage

Course Schedule Day 4Improving Kernel Performance

Kernel Hacking

CONFIG_EMBEDDED

Configuring printk

Test Code

Configuring Kernel and IO Scheduling

Improving CPU Performance

Run Queue Statistics

Context Switches and Interrupts

CPU Utilization

Linux Performance Tools for CPU

Process-Specific CPU Performance Tools

Stupid Cache Tricks

Improving System Memory Performance

Memory Performance Statistics

Linux Performance Tools for Memory

Process-Specific Memory Performance Tools

More Stupid Cache Tricks

Improving I/O and Device Driver

Performance

Disk, Flash and General File I/O

Improving Overall Performance Using theCompiler

Basic Compiler Optimizations

Architecture-Dependent and Independent Optimization

Code Modification Optimizations

Feedback Based Optimization

Application Resource Optimization

The Hazard of Trust

An Iterative Process for Optimization

Improving Development Efficiency

The Future of Linux Performance Tools

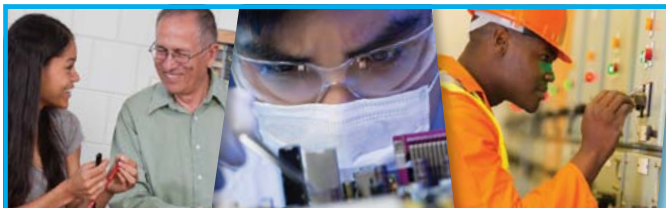
Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

**Decision (Run/Cancel) Date for this Courses is
Monday, May 1, 2017**

Payment received by April 28**IEEE Members \$395****Non-members \$415****Payment received after April 28****IEEE Members \$415****Non-members \$435**

<http://ieeeboston.org/embedded-linux-optimization/>



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Last Notice Before Course Begins, Please Register now and Save \$\$\$!!!

Introduction to Embedded Linux

Time & Date: 6 - 9PM, Mondays, March 20, 27, April 3, 10

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4 day course introduces the Linux Operating System and Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part of the course covers testing, booting and configuring of Embedded Linux systems including embedded cross-development and target board considerations.

Who Should Attend - The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives

- To provide a basic understanding of the Linux OS and the Eclipse IDE framework.
- To understand the complexities of Embedded Linux Distributions in embedded systems.
- To learn how to configure, boot and test Embedded Linux distributions and applications running on Embedded Linux target systems.
- To give students the confidence to apply these concepts to their next Embedded Linux project

Hardware and Software Requirements - The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ installation or prior knowledge of C-based Makefiles is useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials

- Linux Kernel Development by Robert Love
- Linux System Programming by Robert Love
- Embedded Linux Primer by Christopher Hallinan
- Pro Linux Embedded Systems by Gene Sally
- Embedded Linux Development Using Eclipse by Doug Abbott
- Linux Device Drivers by Jonathan Corbet et al
- Essential Linux Device Drivers by Sreekrishnan Venkateswaran

Course Schedule Day 1

Embedded Development Basics

Embedded Systems Characteristics

Embedded Real-Time Systems

Embedded Linux Systems and the Internet of Things (IOT)

Embedded Linux Basics

Embedded Linux Training Overview

Linux Terminology, History and Versioning

The Linux Community: Desktop & Embedded
Linux and the GPL

Linux References (Books and Online)

Getting Started in Embedded Linux

Kernel Source Code

Building the Kernel

Embedded Linux Kernels

Linux 2.6, 3.x and 4.x

Embedded Linux Kernel Overview

Process and Threads Management

Signals and System Calls

Synchronization, IPC and Error Handling

Timing and Timers

Memory Management and Paging

The I/O Subsystem: A Tale of Two Models

Modularization

Debugging

Process-Level and System-Level Debug

GDB, GDB Server and the GDB Server Debugger

Other Debug and Test Tools

An Eclipse Remote Debug Example

Advanced Debug with printk, syslogd and LTTng

System-Level Debug

System-Level Debug Tools

The /proc Filesystem

Advanced Logging Methods

KGDB and KDB

Crash and Core Dumps

Course Schedule Day 2

Process & Threads Management

What are Processes and Threads?

Virtual Memory Mapping

Creating and Managing Processes and Threads

Thread-Specific Data (TSD)

POSIX

The Native POSIX Threading Library (NPTL)

Kernel Threads

Signals in Embedded Linux

System Calls in Embedded Linux

Scheduling

Linux 2.4 and 2.6 Scheduling Models

The O(1) Scheduler

The Completely Fair Scheduler (CFS)

Synchronization

Via Global Data

Via Semaphores, Files and Signals

Condition and Completion Variables

Mutexes and Futexes

Inter-Process Communications (IPC)

Message Queues

Semaphores Revisited

Shared Memory

Pipes and FIFOs

Remote Procedure Calls

Networking

Course Schedule Day 3

Memory Management and Paging

Linux, Demand Paging and Virtual Memory

Allocating User and Kernel Memory

Mapping Device Memory

The Slab Allocator

The OOM Killer

Managing Aligned Memory

Anonymous Memory Mappings

Debugging Memory Allocations

Locking and Reserving Memory

Huge Pages

Memory in Embedded Systems

Error Handling

errno and perror

strerror and strerror_r

oops, panics and Segmentation Faults

Timing

How Linux Tells Time

Kernel, POSIX and Interval Timers

High-Resolution Timers (HRTs)

Sleeping

Sleep Waiting and Spinlocks

Using Timers

Embedded Recommendations for Timing

Modularization

Creating and Building a Module

A Simple Kernel Module

Module Loading

Module Dependencies

Module Licensing

Shared Libraries

A Shared Library Example

Static and Dynamic Libraries

Interrupt and Exception Handling

Bottom Halves and Deferring Work

Course Schedule Day 4

The I/O Subsystem: A Tale of Two Models

The UNIX Device Driver Model

The Standard I/O Interface

Major and Minor Numbers

Configuring the Device Driver

The Evolution of the New Device Driver

Model

The Initial Object-Oriented Approach

Platform Devices, Busses, Adapters and Drivers

A Generic Subsystem Model

The Generic Subsystem Model in Detail

Subsystem Registration

The Probe and Init Functions

The Show and Store Functions

User Access via the /sys Filesystem

Configuring the New Device Driver

The udev Linux Application

Comparing the Two Driver Models

Advanced I/O Operations

Standard UNIX I/O Operations

Scatter-Gather and Asynchronous I/O

Poll/Select and Epoll

Memory-Mapped I/O

File Advice

I/O Schedulers and inotify

The Linux Boot Process

The Root Filesystem

Desktop Linux Boot

Bootloaders and U-Boot

Embedded Linux Boot Methods

Building and Booting from SD Cards

Managing Embedded Linux Builds

Configuring and menuconfig

Oldconfig, menuconfig, xconfig and gconfig

Building Custom Linux Images

Target Image Builders

The Open Embedded Project and the Yocto Project

System Architecture Design Approaches

Deploying Embedded Linux

Choosing and Building the Root Filesystem

Module Decisions

Final IT Work

Embedded Linux Trends

Development Trends

Monitoring Trends

Testing Trends

Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

**Decision (Run/Cancel) Date for this Courses is
Friday, March 10, 2017**

Payment received by March 8

IEEE Members \$400

Non-members \$430

Payment received after March 8

IEEE Members \$430

Non-members \$455

<http://ieeeboston.org/introduction-embedded-linux-2/>

Embedded Linux BSPs and Device Drivers

Time & Date: 6 - 9PM, Wednesdays, April 12, 19, 26, May 3

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the development of Embedded Linux Board Support Packages (BSPs), Device Drivers and Distributions. The first part of the course focuses on BSP and Software Development Kit (SDK) development in an Embedded Linux context with a focus on application performance measurement and improvement. The latter part of the course covers Embedded Linux Device Driver development including key device driver decisions and deployment considerations for Embedded Linux BSPs.

Who Should Attend - The course is designed for real-time engineers who are developing Embedded Linux BSPs and Device Drivers for Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Linux BSP and Device Driver development.

Course Objectives

- To gain an understanding of the complexities of BSP and SDK development and their uses in Embedded Linux systems.
- To provide a basic understanding of the Linux I/O Subsystem and the Device Driver Models provided with Embedded Linux distributions.
- To gain an in-depth understanding of character-based device drivers in Embedded Linux
- To understand key device driver subsystems including relatively slow I/O interconnects such as I2C, SPI and USB as well as high-speed interfaces

such as USB 3.0 and PCIe

- To give students the confidence to apply these concepts to their next Embedded Linux project.

Course Schedule Day 1

Getting Started with Embedded Linux

Linux and the GPL

Building the Kernel Source Code

Embedded Linux Kernels

BSPs and SDKs

Linux References (Books and Online)

Embedded Linux BSP Development Basics

BSP Requirements

U-Boot and Bootloader Development

Basic BSP Development

Files and Filesystem Support

The I/O Subsystem: Talking to Hardware

Memory Management and Paging

Error Handling in Embedded Linux BSPs

Timing and Timers

Interrupt Handling in BSPs

BSP Deployment Issues and Practices

Embedded Linux SDK Basics

The 3 Pieces of an SDK

Embedded Linux Distributions

The GNU Compiler Collection (GCC)

Other Embedded Linux Development Tools

Library Support

Glibc and Alternatives

SDK Deployment and Support

Debugging

GDB, GDB Server and the GDB Server Debugger

Other Debug Tools
 An Abatron Board Bring-Up Example
 An Eclipse Remote Debug Example
 Advanced Debug with printk, syslogd and LTTng
 System-Level Debug
 System-Level Debug Tools
 The /proc Filesystem
 Advanced Logging Methods
 KGDB and KDB
 Crash Dumps

Course Schedule Day 2

Configuring Embedded Linux
 Config Methods
 Config Syntax
 Adding Code to the Linux Kernel
 Booting Embedded Linux
 The Linux Boot Process
 NFS and RAMdisk Booting
 Root and Flash File System Development
 Building the RAMdisk
 Busybox Development
 Testing and Debug of Embedded Linux BSPs
 Kernel Debug and Kernel Probes
 Kexec and Kdump
 The Linux Test Project (LTP)
 Performance Tuning Embedded Linux BSPs
 User Mode Linux and Virtualization
 Measuring Embedded Linux BSP
Performance
 Common Considerations
 Uncommon Considerations
 BootLoader Optimizations
 Boot Time Measurements
 Effective Memory and Flash Usage
 Filesystem Performance Issues
 Some Ideas on Performance Measurement

Course Schedule Day 3

The Original Device Driver Model
 The fops struct and Char Drivers
 The inode and dentry structs
 Major and Minor Numbers
 Embedding Channel Information
 Deferring Work

The /proc Filesystem
 Configuring the Device Driver
 Modularization Revisited
 The New Device Driver Model
 An Object-Oriented Approach
 Platform Devices and Drivers
 Subsystem Registration
 The Probe and Init Functions
 The Show and Store Functions
 The /sys Filesystem
 Configuring the New Device Driver

Comparing the Two Driver Models

The Flattened Device Tree (FDT)
 openBoot and its Effect on Embedded Linux
 The Device Tree Script (dts) File
 The Device Tree Compiler (dtc)
 The Device Tree Blob (dtb) File
 Building a dtb File
 Hybrid Device Drivers
 Other fops Functions
 The Need for ioctl
 A Simulated Char Device Driver
 The SIM Device Driver
 Initialization
 Open and Close
 Read and Write
 The /proc Driver Interface
 MMAP Support

Course Schedule Day 4

Linux Device Driver Subsystems
 Serial Drivers
 The RTC Subsystem
 Watchdogs
 I2C & SPI
 Block Devices
 PCI
 USB
 VME
 Video
 Sound
 What's Missing?
 Memory Technology Devices

What is an MTD?

NAND vs NOR Flash Interfaces

The Common Flash Interface (CFI)

Driver and User Modules

Flash Filesystems

Drivers in User Space

Accessing I/O Regions

Accessing Memory Regions

User Mode SCSI, USB and I2C

UIO

High-Speed Interconnects

PCIe

GigE

iSCSI

Infiniband

FibreChannel

Serial RapidIO

Debugging Device Drivers

kdb, kgdb and JTAG

Kernel Probes

Kexec and Kdump

Kernel Profiling

User Mode Linux and Kernel Hacking

Performance Tuning Device Drivers

Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at LinuxWorks, Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based software development tools, training and consulting services for the embedded systems market.

**Decision (Run/Cancel) Date for this Courses is
Monday, April 3, 2017**

Payment received by March 31

IEEE Members \$395

Non-members \$415

Payment received after March 31

IEEE Members \$415

Non-members \$435

<http://ieeeboston.org/embedded-linux-bsps-device-drivers/>

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Determining and Communicating Project Value Return on Investment (ROI)

ROI Value Modeling™ for Decision Making

Date & Time: Wednesday, May 24; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

Companies are demanding reliable financial measures of proposed projects' value. Yet, project managers often don't know how to identify, calculate, or communicate a project's REAL ROI™ (Return on Investment). Traditional ROI calculations increasingly are being criticized for telling only part of the necessary story. The difficulty afflicts all types of projects but often is greatest in areas like IT, where benefits may seem intangible and frequent overruns impact estimates' credibility. This interactive workshop reveals 22 pitfalls that render common ROI determinations meaningless and shows instead how to identify full-story key effects on revenue and expense variables, reliably quantify tangible and intangible costs and benefits, and convincingly communicate the business value of project investments. Exercises enhance learning by allowing participants to practice applying practical techniques to a real case.

PARTICIPANTS WILL LEARN:

- * The financial information that business decision makers need and demand.
- * ROI and related calculations, strengths, weaknesses, and common pitfalls.

* Using ROI Value Modeling™ and Problem Pyramid™ to fully identify relevant costs and benefits.

* Quantifying intangibles, risk, flexibility, and opportunity.

* Professionally presenting credible business value measurements so people pay attention.

WHO SHOULD ATTEND: This course has been designed for business, systems, and project managers as well as analysts, implementers, users, and others who must know the return on project investments.

OUTLINE

WHAT MONEY HAS TO DO WITH IT

Project Manager role with regard to ROI
 Situations demanding ROI, their issues
 Difficulty of making convincing arguments
 Linking ROI to the business case
 Value Modeling™ Relationship Diagram
 Investment vs. expense
 Justification vs. objective analysis
 Meanings of "It costs too much"
 Total Cost of Ownership (TCO)
 Factors other than cost to be considered

Costs and benefits, revenues vs. expenses
 Return on Investment (ROI) calculations
 Net present value, discounted cash flow
 Payback period, annualized return
 Internal rate of return (IRR), hurdle rate
 'Telling the story' not just ROI calculations
 Failing to quantify 'intangibles' and risk
 Scenario approach to showing benefits
 Mistakenly thinking ROI does not apply

DETERMINING MEANINGFUL BENEFITS

Why it's important to find the benefits first
 Treacy's model of 5 revenue categories
 Problem Pyramid™ to find requirements
 Decision variable clarification chain
 Putting a dollar value on intangibles
 Opportunity, innovation, and flexibility
 Mandates, project with no apparent benefits

ESTIMATING CREDIBLE COSTS

Problem Pyramid™ ties costs to value
 Basing costs on implementation of design
 Business case framework
 Basic formula for estimating costs
 Main causes of poor estimates
 Top-down vs. bottom-up techniques
 Risks that afflict ROI calculations
 Three measurable ways to address risks
 Best-, worst-, most-likely-case scenarios
 Sources of parameter sizing assumptions
 Defining a reasonable scenario for success
 Getting reliable cost and revenue amounts

REPORTING AND MONITORING

Single vs. multiple scenario presentation
 Applying apples vs. apples, when you can't
 Scenario assumptions and parameters
 No change vs. proposed scenarios' ROIs

Measuring intangibles' monetary effects
 Continual, step-wise, and one-time changes
 Percentage-likelihood impact adjustments
 Presenting with spreadsheets
 ROI Value Dashboard™ modeling tool
 Caution about commercial ROI calculators
 Using value modeling to improve decisions
 Dashboard and scorecard-type notification
 Capturing, calibrating with project actuals
 Adjusting appropriately during project

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, *Discovering REAL Business Requirements for Software Project Success*, he regularly works with and trains business and systems professionals.

**Decision (Run/Cancel) Date for this Courses is
 Monday, May 15, 2017**

Payment received by May 9

IEEE Members	\$220
Non-members	\$245

Payment received after May 9

IEEE Members	\$245
Non-members	\$265

<http://ieeeboston.org/determining-communicating-project-value-return-investment-roi/>

Making You a Leader - Fast Track

Date & Time: Monday, May 22; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

We do projects to make change. Yet, change will not occur without leadership, and leaders are rare. Leaders make others want to do what the leader wants done. Leaders cause ordinary people to achieve extraordinary things. Managing is not the same as leading, and titles do not make leaders. Seminars can teach you to manage, but they cannot teach you to be a leader. Rather, making a leader takes special techniques—such as our personal development clinics—that can change deep-seated behaviors learned over a lifetime.

However, since clinics usually last about ten weeks, this mini-clinic was devised as a more convenient alternative. This format places responsibility upon the participant to carry out an extended informal follow-on program after completion of the formal seminar workshop session.

During the follow-on period, the participant uses time-condensed methods that simulate the lifetime learning which makes a leader. Therefore, commitment to carrying out these exercises is essential for successful transformation.

PARTICIPANTS WILL LEARN:

- Leadership characteristics and practices that are essential for project and personal success.
- Differences between management and leadership, how they conflict, and why leaders are so rare.
- Behaviors leaders use to influence others, up and down, to want to do what the leader wants them to do

- Special techniques personal development clinics use to change lifetime learning and make leaders.
- How to employ those special techniques in a follow-on mini-clinic to develop the leadership skills they need to make their projects successful.

WHO SHOULD ATTEND: This course has been designed for business and systems professionals who want to improve their ability to lead and influence other people.

LEADERSHIP CHARACTERISTICS & ROLE

How leadership looks and feels

Management vs. leadership

Leadership components of project success

Basic leadership practices; power sources

Real change leaders in organizations

TEAMS AND LEADERSHIP

Everyone feels leadership is lacking

Everyone thinks s/he is a leader

Results, not actions or intent

Workgroups, teams, and leaders

Situational leadership styles

Coaching and sports analogies to projects

INSPIRING AND MOTIVATING

Gaining commitment to project success

Communicating that influences others

Addressing negativism and groupthink

Conscious and unconscious messages

Greatest management principle

Hierarchy of needs effects on projects
 Hygiene factors vs. motivators
 Helping project players get their rewards
 Influencing up and down without authority
 Inspiring the extra efforts projects need
 Energizing the project team

SHARED VISIONS

Relating values and vision to projects
 Getting others to embrace one's vision
 Developing a motivating project vision

WHERE AND HOW LEADERS ARE MADE

Born or made? How do we know?
 Habits of thought that affect project success
 Overcoming self-limiting lifetime learning
 Leader's critical success factors
 Traditional education doesn't make leaders
 Special way—personal development clinics

SETTING AND ACCOMPLISHING GOALS

S.M.A.R.T. goals for self and project
 Action plans to achieve your goals
 Visualizing and emotionalizing

DEFINING THE FOLLOW-ON PROGRAM

Clarifying project leadership objectives
 Breaking into prioritized subgoals
 Establishing rewarding daily achievements
 Special techniques to change habits

CARRYING OUT THE MINI-CLINIC

Working with a follow-up support structure
 Mapping results regularly to goals
 Objectively recording leadership changes
 Self-leadership through the process

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, *Discovering REAL Business Requirements for Software Project Success*, he regularly works with and trains business and systems professionals.

**Decision (Run/Cancel) Date for this Courses is
 Friday, May 12, 2017**

Payment received by May 8

IEEE Members \$220

Non-members \$245

Payment received after May 8

IEEE Members \$245

Non-members \$265

<http://ieeeboston.org/making-leader-fast-track-2/>

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 April 25 - 26, 2017
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*(The technical program, conference
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2017 IEEE International Midwest
 Symposium on Circuits and Systems
 August 6 - 9, 2017
www.MWSCAS2017.org
*(Call for Papers Deadline,
 March 10, 2017)*

2017 IEEE High Performance Extreme
 Computing Conference HPEC '17
 September 12 - 14, 2017
www.ieee-hpec.org
 Submission deadline is
 May 19, 2017

Proactive user Acceptance Testing™ -- Confident Competence

The Testing Users need to be Confident the Software they Depend on Works

Date & Time: Thursday, May 25; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

Projects aren't complete until users/customers are sure the systems they depend on actually meet business requirements, work properly, and truly help them do their jobs efficiently and effectively. However, users seldom are confident or comfortable testing system acceptability. Project Managers and Testing professionals need to know how to guide and facilitate effective acceptance testing without usurping the user's primary role. This intensive interactive seminar shows what users need to know to confidently make the best use of their time planning and conducting acceptance tests that catch more defects at the traditional tail-end of development, while also contributing in appropriate ways to reducing the number of errors that get through the development process for them to catch in UAT. Exercises give practice using practical methods and techniques.

PARTICIPANTS WILL LEARN:

- * Appropriate testing roles for users, developers, and professional testers; and what each shouldn't test.
- * How Proactive Testin™ throughout the life cycle reduces the number of errors left to find in UAT.
- * Key testing concepts, techniques, and strategies that facilitate adaptation to your situation.

* Systematically expanding acceptance criteria to an acceptance test plan, test designs, and test cases.

* Supplementing with requirements-based tests, use cases, and high-level structural white box tests.* Techniques for obtaining/capturing test data and carrying out acceptance tests.

WHO SHOULD ATTEND: This course has been designed for business managers and system users responsible for conducting user acceptance testing of systems they must depend on, as well as for system and project managers, analysts, developers, quality/testing professionals, and auditors.

ROLE OF USER ACCEPTANCE TESTING

Why users may resist involvement
 Making users confident about testing
 Objectives, types, and scope of testing
 Acceptance testing as user's self-defense
 Why technical tests don't catch all the errors
 Essential elements of effective testing
 CAT-Scan Approach™ to find more errors
 Proactive Testing™ Life Cycle model
 Separate technical and acceptance test paths
 Place of UAT in overall test structure
 Making sure important tests are done first
 Developer/tester/user test responsibilities

DEFINING ACCEPTANCE CRITERIA

Defining acceptance test strategy up-front
 Source and role of acceptance criteria
 5 elements criteria should address
 Functionality the user must demonstrate
 How much, how often user must test
 Determining system quality
 Who should carry out acceptance tests
 How acceptance tests should be performed
 Added benefit, revealing requirements errors

DESIGNING ACCEPTANCE TEST PLANS

Expanding the acceptance criteria
 Allocating criteria to system design
 Refining the design to catch oversights
 Checklist of common problems to test
 Equivalence classes and boundary values
 Making quality factors (attributes) testable
 Structural testing applicable to users
 GUI features that always need to be tested
 Defining requirements-based tests
 Constructing use cases
 Cautions about use case pitfalls
 One- and two-column use case formats
 Turning use cases into tests
 Consolidating tests into efficient test scripts

CARRYING OUT ACCEPTANCE TESTS

Differentiating test cases and test data
 Traps that destroy value of acceptance tests
 Warning about conversions
 Documentation, training, Help tests
 Configuration, installation, localization

Security, backup, recovery tests
 Suitability of automating acceptance testing
 Performance, stress, load testing
 Issues on creating test conditions, data
 Capturing results, determining correctness
 User's defect tracking and metrics

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**Decision (Run/Cancel) Date for this Courses is
 Tuesday, May 16, 2017**

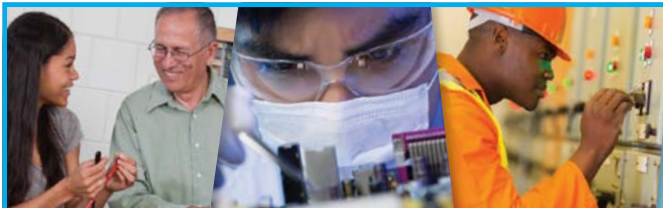
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<http://ieeeboston.org/proactive-user-acceptance-testing-confident-competence-testing-users-needconfident-software-depend-works/>



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Writing Agile User Story and Acceptance Test Requirements

Date & Time: Tuesday, May 23; 8:30AM - 5:00PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

Everyone complains that poor requirements are the major cause of project problems. Yet, like the weather, nobody does much about it, at least not effectively. Traditional approaches advocate writing voluminous requirements documents that too often don't seem to help much and may even contribute to difficulties. Agile goes to the opposite extreme, relying on brief requirements in the form of three-line user stories that fit on the front an index card and a few user story acceptance criteria that fit on the card's back. Surprise, as Mark Twain noted, in some ways it's even harder to write Agile's brief requirements effectively. This interactive workshop reveals reasons user stories and their acceptance tests can fall short of their hype, explains critical concepts needed for effectiveness, and uses a real case to provide participants guided practice writing and evaluating user stories and their acceptance criteria/tests.

PARTICIPANTS WILL LEARN:

- * Major sources of poor requirements that cause defects, rework, and cost/time overruns.
- * How Agile user stories and their acceptance criteria/tests address these issues.
- * Difficulties that still afflict requirements in Agile projects and why they persist.

- * Writing more effective user stories and acceptance criteria/tests.
- * What else is necessary to produce working software that provides real value.

WHO SHOULD ATTEND:

This course has been designed for product owners, analysts, developers, and other Agile (and other) project team members who are or should be involved in defining requirements.

AGILE, USER STORY FUNDAMENTALS

Agile Manifesto's relevant points
 Characterization of traditional approaches
 Waterfall and big up-front requirements
 Agile's sprints and backlogs alternative
 Agile project team roles
 User story "As a <role>..." (Card)
 User story acceptance criteria (Confirmation)
 Estimating user story size
 Splitting and refining
 Prioritizing and allocating to backlogs/sprint
 Constructing/implementing (Conversations)
 Reviewing, retrospectives
 Grooming backlog and reprioritizing
 Exercise: Write Needed User Stories
 Exercise: Define their Acceptance Criteria
 Exercise: Review Your User Stories/Criteria

**REQUIREMENTS ARE REQUIREMENTS—
OR MAYBE NOT**

User stories are backlog items, features
 Chicken and egg relation to use cases
 Issues and inconsistencies
 Business vs. product/system requirements
 “Levels Model” of requirements
 Other mistaken presumptions
 Requirements overview
 Where user stories should fit, do fit instead
 Conversation conundrum

WRITING MORE SUITABLE USER STORIES

Problem Pyramid™ tool to get on track
 Exercise: Using the Problem Pyramid™
 Exercise: Business Requirement
 User Stories
 Issues identifying requirements
 Product owner and business analyst roles
 Project team participation
 Dictating vs. discovering
 Data gathering and analysis
 Planning an effective interview
 Controlling with suitable questions
 Then a miracle occurs...

AND USER STORY ACCEPTANCE TESTS

Missed and unclear criteria
 Turning criteria into tests, issues
 How many tests are really needed
 Test design techniques
 Checklists and guidelines
 Decision trees, decision tables
 Boundary testing
 Testing is main means to control risk

Defects and new user stories
 Testing that user story focus misses
 Reactive vs. proactive risk analysis
 Given, when, then format

Exercise: Write User Story Acceptance Criteria
 Exercise: Design their Tests
 Exercise: Review Your User Stories/Tests

Speaker’s Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, *Discovering REAL Business Requirements for Software Project Success*, he regularly works with and trains business and systems professionals.

**Decision (Run/Cancel) Date for this Courses is
 Friday, May 12, 2017**

Payment received by May 8

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