BOSTON

THE REFLECTOR

ISSUE #7
JULY 2017

IEEE
Advancing Technology for Humanity

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It's Coming!

by Karen Panetta, Reflector Editor

"If a tree falls in the woods, and no one is around to hear it, does it make a sound?"

I remember being asked this question as an undergraduate student in a philosophy class. The class was needed to fulfill a graduation requirement. However, I would have preferred to take another programming or hardware design class to gain more of what I considered "real" engineering skills that would help me find a job.

I responded to the question by saying, "Of course it makes noise!" I then outlined the physics, waves and acoustics principles to support my position. I couldn't help but wonder why I was wasting time pondering ridiculous questions like this, when there were circuits to be built, programs to code and laboratory reports to be written. To a young undergraduate student, philosophy and engineering seemed like totally different universes, never destined to meet. I received a C+ for my response.

Little did I know then, that it was not the "yes/no" type of answer to the question that truly mattered. What was more important to consider was how our brains processed and analyzed questions like these and the introspective journey our minds travel as we solve problems.

Today's successful engineers must be well-rounded and fluent in the arts and humanities. Learning our craft does not just mean learning the technical tools and theories of our trade. It requires we give ourselves permission to allow unconstrained perspectives on problem solving beyond any boundaries.

I learned this lesson well when I traveled to the Czech Republic to speak at their Robotics conference. There, I met world renown philosophers and cognitive science experts. Their research looks at artificial intelligence, robots and human-machine interactions. Everyone may think of the evil "Terminator" type of robot bent on wiping out humans whenever we talk about the future of artificial intelligence and robots, but adding the philosophical point of view brings us back to just being human and how we think.

I am now sorry I didn't pay more attention in that philosophy class. If I understood more about how people think, I would have invested in those "fidget or finger spinner" toys that are all the rage now. They look like someone was smart enough to extract all the ball bearing assemblies out of discarded rollerblades and rebrand them as a toy, resulting in an outrageous profit margin. However, there are much better examples that demonstrate how understanding how the brain "thinks" can benefit humanity.

Recently, someone asked me about the goal of building humanoid robots to assist the elderly or differently abled persons. I can envision a robot to help me do the chores and heavy lifting I can't do or do not want to do, such as taking out the trash,

or carrying in groceries up flights of stairs. On the other hand, I do not envision keeping the company of a robot for companionship. It would be sad if an artificial human will be the only one that will tolerate being in my presence in my old age. If I get that desperate, I may as well revive the faithful "pet rock".

What would be even more useful, would be an intelligent information security agent that screened all those scam calls, emails and door to door solicitors that prey on the elderly. However, when it comes to cognitive science and deep learning, we should be thinking even bigger and beyond boundaries.

Using cognitive science, imagine being able to understand and model emotions, mental stress, drug addictions and memory impairment diseases like Alzheimer's to find cures and treatments. The possibilities are limitless and in this digital deep learning age, all of it can be realized.

The question is, as cognitive brain science and engineering becomes one of today's most attractive and important fields in advancing data science, are you ready for it? Our world needs us to be ready so we can take on the global challenges facing society right now.

Our IEEE Boston Section Computer Society and Computational Intelligence Society are already ahead of the curve on these topics and can help make sure you are ready too. To get started, check out one of the "Rock Star series" at https://www.computer.org/web/rockstars

IEEE Boston Section Online Courses:

(Students have 90 day access to all online, self-paced courses)

Verilog101:Verilog Foundations

Full course description and registration at ,
http://ieeeboston.org/verilog-101-verilog-foundations-online-course/

System Verilog 101: Design Constructs

Full course description and registration at ,
http://ieeeboston.org/systemverilog-101-sv101-design-constructs-online-course/

System Verilog 102: Verification Constructs

Full course description and registration at ,
http://ieeeboston.org/systemverilog-102-sv102-verification-constructs-online-course/

High Performance Project Management

Full course description and registration at ,
http://ieeeboston.org/high-performance-project-management-online-course/

Introduction to Embedded Linux Part I

Full course description and registration at ,
http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/

Embedded Linux Optimization - Tools and Techniques

Full course description and registration at ,
http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/ **NEW Online course**

Software Development for Medical Device Manufacturers

Full course description and registration at ,
http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/

Fundamental Mathematics Concepts Relating to Electromagnetics

Full course description and registration at ,
http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/

Reliability Engineering for the Business World

Full course description and registration at ,
http://ieeeboston.org/reliability-engineering-business-world-line-course/

Entrepreneurs" Network – 6:45PM, Thursday, 13 July

2017 BOSTON HARBOR NETWORKING CRUISE

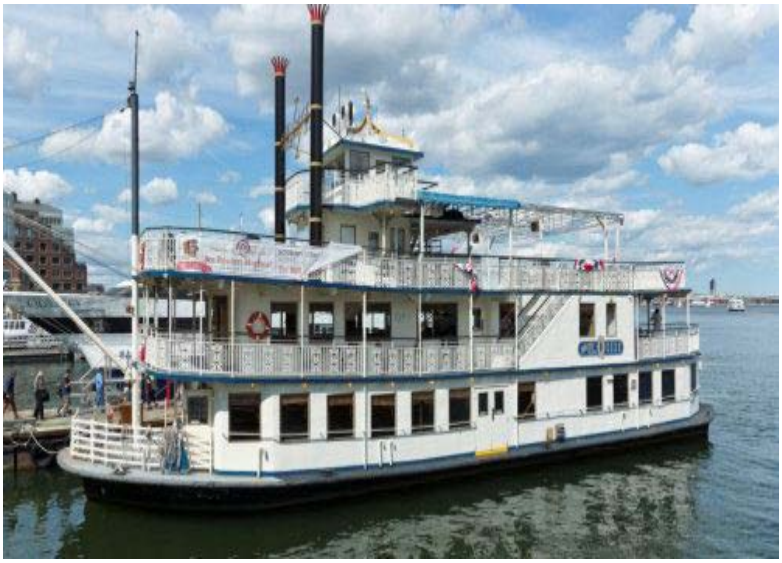
Time: 6:45 PM - 9:30 PM. Location: Rowes Wharf, Boston, MA

IEEE Boston Entrepreneurs' Network will hold its 14th annual Sunset Cruise & Networking Evening on Boston Harbor aboard the M/V Music City Queen, on Thursday, July 13, 2017. We board the boat at 6:45 p.m., and cruise from 7:15-9:30, with additional networking on the boat dockside until 10:00 pm. The event includes a light dinner catered again this year by the well respected Off the Vine Catering, who received many compliments for the food the last three years. There will also be a cash bar.

This year's cruise is sponsored by:
Peter E. O'Neil
617.817.7844
peter.oneil@hrknowledge.com
Employee Benefits/HR Support/Managed Payroll

Our ENET Sunset Cruise on Boston Harbor will be an enjoyable, casual wrap-up for the ENET 2016-2017 season, our 26th year. We again expect over 220 attendees and guests. This was a sold-out event so please register early! To enhance the networking opportunities, we have invited all ENET speakers whose presentations you enjoyed during the past year. We have also invited a number of angel and early stage venture capital investors to join us on the cruise. We will also be joined by members and guests of several other Massachusetts technology-based entrepreneurial groups, who are partnering with ENET for this "EntrepreneurSHIP 2017" including the MDG – the Medical Development Group, WIE - IEEE Women In Engineering, the EntreTech Forum and the Mass Bio Pharma Networking Group - MBPNG .
We will be cruising on the The M/V Music City Queen, an ornamental sternwheeler named after the city that sits along the banks of the Cumberland River (Nashville)! The Music City Queen is berthed at Rowes Wharf, behind the Boston Harbor Hotel on Atlantic Ave. in Boston. Parking is available for $7 at International Place garage across the street from Rowes Wharf and there are two "T" stops nearby.
Registration will begin on May 3th, 2017. You can register at the ENET meeting on May 3rd, by mail or at the ENET website. Your seat can be saved only by paid-up registration.

SPACE IS LIMITED AND WE SOLD OUT LAST



YEAR. So, you are encouraged to register soon so you won't miss out.

For ENET Members, the price is just $35 for the Member, and $35 for his/her spouse or significant other. For non-members of ENET, spouses/significant others, or guests, the price is $45.

If you join ENET now, you can get the above Member Rates for the boat cruise for yourself and spouse/significant other, and ENET Membership through August 31, 2018.

Membership cost is $85 for existing IEEE members (we need your IEEE membership number) and $95 for all others. Thus, IEEE members SAVE $40 by joining the ENET for this event and attending the cruise with your spouse or significant other. JOIN ENET and SAVE!

REGISTER:
ENET Member – $35.00
ENET Members register with your spouse or significant other. Price is $35 for ENET member + $35 for spouse/significant other.
Non-ENET Member – $45.00
Non-ENET members are invited to attend and enjoy the cruise for $45.

You can register or pay online or you can print and complete the form, and mail it with your check made payable to "IEEE Entrepreneurs' Network" to ENET Chairman and Boat Cruise coordinator, Robert Adelson, Engel & Schultz, LLP, One Federal Street, 21st Floor, Boston, MA 02110. For payment confirmation or questions (or to obtain forms if not available at the website), contact Robert Adelson, Chairman of ENET and Boat Cruise coordinator. His email is: radelson@engelschultz.com or if necessary call 617-951-9980 ext. 205 or fax 617-951-0048.

PARKING INFO:
Low cost parking is available after 5:00 pm at 1 International Place garage for just $7.00, just across Atlantic Ave. from Rowes Wharf (Go to http://bostonparking.spplus.com/Boston-1-International-Place-Parking-Parking-Coupon.html and print coupon to bring with you (you need the coupon for the reduced rate) and there are two T stops within a ten minute walk (Aquarium and South Station).
Earlier attendees have really enjoyed this great event. We hope you will join us July 13th!

Call for Articles

Now that the Reflector is all electronic, we are expanding the content the publication. One of the new features we will be adding are technical and professional development articles of interest to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.
To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional articles will be reviewed by the publications committee for suitability.The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!
Submissions should be sent to; ieeebostonsection@gmail.com

2017 IEEE WIE USA EAST FORUM

Call for Participation

November 30 – December 2, 2017 Baltimore, MD

Presentation Topics

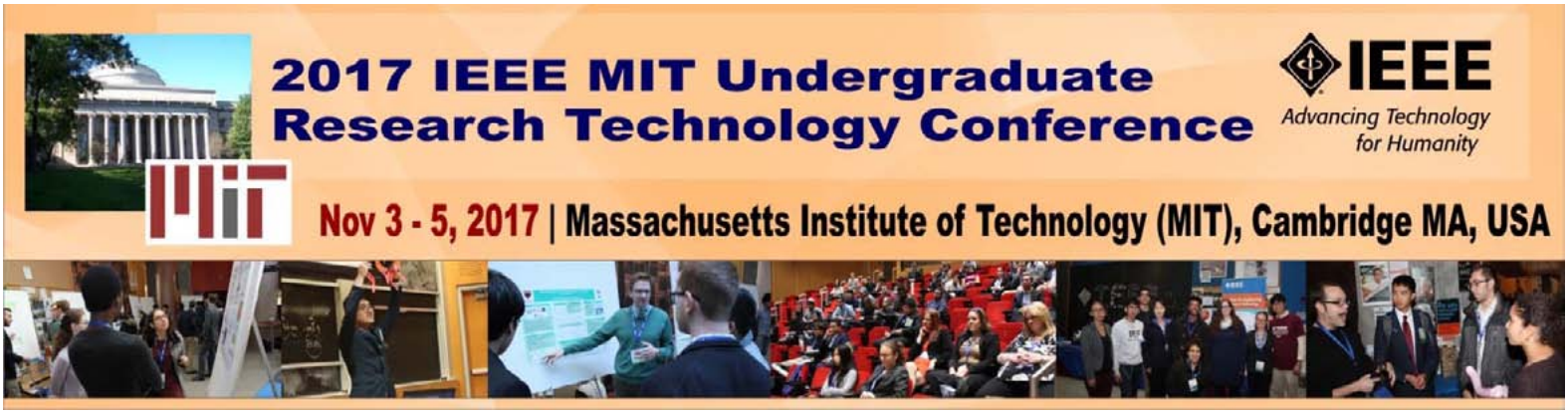
- Mentoring the next generation of female leaders
- Strategies for increasing equity in power and decision making
- Women as leaders in education, industry, and government
- Development: communication skills in written and spoken word, effective dialog
- Cross-cultural aspects of leadership
- What it takes to be a great leader - qualities that all successful leaders share
- Shaping the future by female leaders
- Training vs inherent skills: can leadership be learned?
- Work-Life balance: family systems traditions and changes
- Leadership development for women: overcoming stereotypes
- The design, implementation, and evaluation of leadership from a structural perspective
- Helping girls and young women become leaders - motivating to empower, empowering to motivate
- Exploring the attrition gap - why do women leave the engineering field and what can be done to prevent it

Submission Deadline

Presentation topic abstract suitable for program (up to 150 words), and extended abstract for evaluation (up to 2 pages) due 24 July 2017.

For more information, visit:
http://sites.ieee.org/wie-forum-usa-east/calls-for-participation/

IEEE WIE FORUM USA EAST 2017 IEEE IEEE-USA



Call for Submissions

Submission Deadline: June 30th, 2017

Envisioning a technical conference targeted towards undergraduate students all over the globe, the MIT IEEE Student Branch in 2015 inaugurated the IEEE MIT Undergraduate Research Technology Conference. This year we are organizing it again with the goal to make the conference a venue where undergraduate students can meet to present, discuss, and develop solutions advancing technology for humanity. Participants can attend a rich program with renowned speakers, technical sessions, a student design competition, exhibits, networking, and social activities, presenting a great opportunity for students to interact with leading industry experts.

The conference theme is "Meet Innovative Technology", and the six fields of focus are:

1. Machine Learning / Artificial Intelligence (AI)
2. Biological and Biomedical Engineering and Technology (BioEECS)
3. Robotics and Automation Technology
4. Systems and Networking
5. Embedded Technologies
6. Innovative Technologies and Others

Authors may submit content in the form of a technical paper, poster, or lightning talk.

All submissions must be written in English. Paper submissions must be no longer than 4 pages, single-spaced, with a minimum font of 10 point, and submissions may include figures, illustrations, and graphs. Abstract submissions for the poster and lightning talk are limited to 500 words.

All submissions will be peer-reviewed. Submissions are online, with a deadline of June 30th, 2017. Notification of acceptance will be sent via email by August 4th, 2017.

Please join the mailing list (MIT-Conference@ieee.org) for more information and updates on submission, the technical program, registration, and accommodation.

A conference proceeding of all the accepted papers that have been presented at the conference may be published and included in the IEEE Xplore journal. Electronic and online media containing all accepted submissions will be distributed to all registered attendees.

Meet Innovative Technology

Sponsored by MIT IEEE Student Branch and IEEE Boston Section

http://ieee.scripts.mit.edu/conference

Massachusetts Institute of Technology

IEEE BOSTON SECTION

Digital Signal Processing (DSP) for Wireless Communications - Under the Hood

Time and Dates: 6 - 9PM, Wednesdays, October 18, 25, November 1, 8, 14
(Note: Nov. 14 is a Tuesday)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Dan Boschen, Microsemi

Course Summary:

This course is a fresh view of the fundamental concepts of digital signal processing most applicable to practical real world problems and applications in radio communication systems. This course will build an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real world applications in GPS and mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges in both the analog and digital domains, and not a tutorial on working with specific DSP processor hardware.

Target Audience:

All engineers involved in or interested in signal processing applications. Engineers with significant experience with DSP will also appreciate this opportunity for an in depth review of the fundamental DSP concepts from a different perspective than that given in a traditional introductory DSP course.

Benefits of Attending/ Goals of Course:

Attendees will build a stronger intuitive understanding of the fundamental signal processing concepts involved with digital filtering and mixed signal communications system design. With this, attendees will be able to implement more creative and efficient signal processing architectures in both the analog and digital domains

Topics / Schedule:

Class 1:
Correlation
Fourier Transform
Laplace Transform

Class 2:
Sampling and A/D Conversion
Z –transform
D/A Conversion

Class 3:
IIR and FIR Digital filters
Direct Fourier Transform

Class 4:
Windowing, Digital Filter Design
Fixed Point vs Floating Point

Class 5:
Fast Fourier Transform
Multirate Signal Processing
Multi-rate Filters

Speaker's Bio:

Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 20 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave de

signing and developing transceiver hardware from baseband to antenna for wireless communications systems. Dan is currently at Microsemi (formerly Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page at: http://www.linkedin.com/in/danboschen

Decision (Run/Cancel) Date for this Courses is Monday, October 9, 2017

Payment received by October 6
IEEE Members $325
Non-members $360

Payment received after October 6
IEEE Members $360
Non-members $425

Registration will be online as of Augsut 1, 2017

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gamil.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Embedded Linux Optimization - Tools and Techniques (*Online Edition*)

Students have access to this self-paced course for 90 days!!

Registration fee: $250

Summary - This video course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand debugging, profiling and testing high performance Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.
- To give students the confidence to apply these concepts to their next Embedded Linux project.

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

Getting Started with Embedded Linux
Embedded Linux Training Overview
Terminology
Linux Versioning
The GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs
Linux References (Books and Online)
A Development Cycle Focused on Performance
A Basic Optimization Process

Basic Debugging Review
Embedded Applications Debug
GDB, GDB Server and the GDB Server Debugger
Other Debuggers
An Eclipse Remote Debug Example
Debugging with printk, syslog, syslogd and LTTng

System-Level Debug
System-Level Debug Tools
The /proc and /sys Filesystems

Basic Logging
KDB and KGDB
Crash Dumps and Post-Mortem Debugging
Debugging Embedded Linux Systems
Backend Debuggers
In-Circuit Emulators
Hardware Simulators
Analyzers
Requirements Development
Performance Requirements
Derived Requirements
Testability and Traceability
Reviewing Requirements
Designing for Performance
Design for Test (DFT)
Agile Software Design
Software and Linux Decomposition
Memory Management
CPU and OS Partitioning
Design Reviews
Coding for Performance
Coding Standards and Consistency
Languages, Libraries and Open Source Components
Learning Magic Numbers
Letting Compilers Work For You
Global, Static and Local Variables
Code Reviews

Software Testing
Unit-Level Testing
System-Level Testing
Code Coverage Tools
gcov
Automated Testing
Some Embedded Linux Test Recommendations
DebugFS
Configuring DebugFS
DebugFS Capabilities
Advanced Logging
LogFS
Using Logwatch and Swatch
Using syslogd and syslog-ng
Tracing
ptrace and strace
New Tracing Methods
SystemTap
Ftrace, Tracepoints and Event Tracing
Tracehooks and utrace
Profiling
Basic Profiling
gprof and Oprofile
Performance Counters
LTTng
Another DDD Example
Manual Profiling
Instrumenting Code
Output Profiling
Timestamping
Addressing Performance Problems
Types of Performance Problems
Using Performance Tools to Find Areas for Improvement
Application and System Optimization
CPU Usage Optimization
Memory Usage Optimization
Disk I/O and Filesystem Usage Optimization
Measuring Embedded Linux Performance
Some Ideas on Performance Measurement
Common Considerations
Uncommon Considerations
Using JTAG Methods
BootLoader Measurements
Boot Time Measurements
The Perf Tool
Origins of Perf
The Perf Framework
Perf Commands and Using Perf
Listing Events
Counting Events
Profiling with Perf
Static Tracing with Perf
Dynamic Tracing with Perf
Perf Reporting
Performance Tool Assistance
Recording Commands and Performance
System Error Messages and Event Logging
Dynamic Probes
Jprobes and Return Probes
Kernel Probes

Kexec and Kdump
- Improving Boot Performance
- Boot Time Optimization
- The Linux Fastboot Capability
- Building a Smaller Linux
- Building a Smaller Application
- Filesystem Tips and Tricks
- Some Notes on Library Usage
- Improving Kernel Performance

Kernel Hacking
CONFIG_EMBEDDED
Configuring printk
Test Code
Configuring Kernel and IO Scheduling

- Improving CPU Performance

Run Queue Statistics
Context Switches and Interrupts
CPU Utilization
Linux Performance Tools for CPU
Process-Specific CPU Performance Tools
Stupid Cache Tricks
- Improving System Memory Performance

Memory Performance Statistics
Linux Performance Tools for Memory
Process-Specific Memory Performance Tools
More Stupid Cache Tricks
- Improving I/O and Device Driver Performance
- Disk, Flash and General File I/O
- Improving Overall Performance Using the Compiler
- Basic Compiler Optimizations
- Architecture-Dependent and Independent Optimization
- Code Modification Optimizations
- Feedback Based Optimization
- Application Resource Optimization
- The Hazard of Trust
- An Iterative Process for Optimization
- Improving Development Efficiency
- The Future of Linux Performance Tools

Some Final Recommendations

http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/

IEEE Boston Section Social Media Links:

Twitter: https://twitter.com/ieeeboston

Facebook: https://www.facebook.com/IEEEBoston

YouTube: https://www.youtube.com/user/IEEEBostonSection

Google+: https://plus.google.com/107894868975229024384/

LinkedIn: https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about

Software Development for Medical Device Manufacturers *(Online Edition)*

New Online Course

Students have access to this self-paced course for 90 days!! ***Registration Fee : $125***

Course Description This course provides an introduction to the development of medical device software. The course is comprised of 4 modules that range from 30-45 minutes in duration. The focus is on complying with FDA Design Controls and IEC 62304 requirements.

This course is intended for software developers who are actively involved in developing medical device software.

Module 1

- Medical Device Definitions: FDA and European Union (EU)
- Regulatory Roadmap
- FDA/EU Device Classifications
- FDA QSR Regulation
- FDA Guidance Documents that pertain to medical device software

Module 2

- International Standards that pertain to medical device software
- Types of Software Regulated by FDA
- Quality System basics: Procedures, Work Instructions and Records
- ALL Software is Defective…

Module 3:

- Design Control Overview
- General Requirements
- Design and Development Planning
- Software Development Models
- Design Input
- About Requirements…
- Design Output
- Design Reviews

Module 4:

- Design Control (continued)
- Design Verification
- Software Verification Process
- Testing Overview
- Design Validation
- Software Validation Process
- Design Changes
- Design Transfer
- Design History File
- Course Summary

Speaker Bio:

Steven R. Rakitin has over 40 years experience as a software engineer including 25 years of experience in the medical device industry. He has worked with over 85 medical device manufacturers worldwide, from startups to Fortune 100 corporations. He has written several papers on medical device software risk management as well as a book titled: Software Verification & Validation for Practitioners and Managers.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE and a member of MassMEDIC. He is on the Editorial Review Board for the ASQ Journal Software Quality Professional.

As President of Software Quality Consulting Inc., he helps medical device companies comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/

Fundamental Mathematics Concepts Relating to Electromagnetics (*Online Edition*)

New Online Course

Students have access to this self-paced course for 90 days!!

Registration Fee: 150

Course Summary This course is designed for people wishing to refresh or to learn the fundamental mathematical concepts that are used to describe electromagnetic wave behavior. The modules address all of the basic math concepts covered in a traditional undergraduate electromagnetics course in an ECE curriculum. These concepts include Vector Basics, Integral Vector Calculus, Differential Vector Calculus, Fundamental Coordinate Systems and Complex Numbers. After completing these modules, a person should have sufficient math skills to pursue graduate studies in electromagnetics and/or be able to decipher the math presented in an upper-level text on the subject.

Target audience: This course is designed for people wishing to refresh or to learn the fundamental mathematical concepts that are used to describe electromagnetic wave behavior.

Course chapters

1. Vector Basics
2. Dot Product
3. Cross Product
4. Contour Integration
5. Vector Algebra
6. Surface Integration
7. Metric Coefficients
8. Coordinate Systems
9. Vector Coordinate Conversion
10. Del Operator and the Gradient
11. The Curl
12. Divergence
13. Stokes Theorem
14. Divergence Theorem
15. Laplacian
16. Complex Numbers

Instructor's Bio:

Dr. Kent Chamberlin is the Chair and a Professor in the Department of Electrical and Computer Engineering. In his more than thirty-five years in academia, he has performed research for more than twenty sponsors, including the National Science Foundation. He has received two Fulbright awards, including the prestigious Fulbright Distinguished Chair, which he served in Aveiro, Portugal. He has also served as an Associate Editor for the Institute for Electrical and Electronics Engineers, and he continues to be active in performing and publishing in a range of research areas.

http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/

Reliability Engineering for the Business World *(Online Edition)*

Students have access to this self-paced course for 90 days!!

Registration Fee: 320

Course Description

This course is about becoming a leader in reliability engineering. While statistics are the tools of reliability engineering, it takes knowledge not only of these tools but also of the business. Developing knowledge of the business, from sales, engineering, customer service, to supply chain management can determine how effective you can be in improving reliability.

Never take anything for granted, even some rules of thumb in reliability can be misleading, this course will show you how to prove what truly happens in the real world and how to effect change in any part of the business where it is needed. We will explore the balance sheet, organizational structure, customers, service, and high volume manufacturing. It's not just about how often things fail, it is also about where the defect came from, what is the financial effect, the recovery, when should a business take field action, effect of human error, failure analysis/material science, reliability testing, and much more. I will also discuss how you develop executive buy in for change. The course assumes a basic knowledge in reliability statistics. There are 12 sessions that cover the following topics.

Course Outline

Basics – Measurements
Business Model
Design Model (HW and SW)
HALT/RDT/Predictions
Manufacturing Model
Early Life Failures
Wear Out and Mid Life Crisis
Advanced Reliability

Course Objective

To teach you how to become the go to person in your business for objective business sensed reliability answers and requirements.

Instructor's Bio

Kevin is an innovative leader in reliability methodologies with more than 30 years experience in the storage industry. In his latest role as Director of Engineering, he developed a top down reliability/availability management process for design organizations developing mission-critical storage systems. Kevin previously directed the most extensive HALT/HASS operation in the industry, with over 300 chambers worldwide. He has written several papers, consulted with many companies, 3 patents awarded and 2 pending related to systems reliability and test.

His most recent work has been performing system architectural analysis to optimize system availability, serviceability and costs. Providing guidance to development to maximize system reliability and reduce service costs. He has provided consultation to many large companies such as EMC, CISCO, AT+T, HP, Seagate and many others. His position and experience has enabled him to perform extensive field studies and design of experiments. Kevin has developed many

http://ieeeboston.org/reliability-engineering-business-world-line-course/

Introduction to Embedded Linux
(Online Edition)

New Online Course

Students have access to this self-paced course for 90 days!! ***Registration Fee: 350***

Course Summary:
This first of a 2-part series introduces the Linux Operating System and the use of Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part covers the methods for booting Embedded Linux distributions including embedded cross-development and target board considerations.

Who Should Attend:
The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives:
To provide a basic understanding of the Linux OS and the Eclipse IDE framework.
To gain an understanding of the complexities of Embedded Linux Distributions and their use in embedded systems.
To give students confidence to apply these concepts to their next Embedded Linux project
Hardware and Software Requirements

The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ installation or prior knowledge of C-based Makefiles is useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials
Linux Kernel Development by Robert Love
Linux System Programming by Robert Love
Linux Debugging and Performance Tuning by Steve Best
Optimizing Linux Performance by Phillip G. Ezolt
Embedded Linux Primer by Christopher Hallinan
Pro Linux Embedded Systems by Gene Sally
Embedded Linux Development Using Eclipse by Doug Abbott
Linux Device Drivers by Jonathan Corbet et al
Essential Linux Device Drivers by Sreekrishnan Venkateswaran
Course Downloadable Content:

Video Lecture
Hands-On Lab Instructions
Hands-On Lab Solutions
Additional Related Materials

The Basics
Linux Terminology, History and Versioning
The Linux Community: Desktop & Embedded
The GPL
Linux References (Books and Online)

Getting Started
Kernel Source Code
Building the Kernel
Embedded Linux Kernels
Linux 2.6

Basic Kernel Capabilities
Process and Threads Management
Signals and System Calls

Synchronization, IPC and Error Handling
Timing and Timers
Memory Management and Paging
The I/O Subsystem: A Tale of Two Models
Modularization

Debugging
Process-Level and System-Level Debug
GDB and KGDB
GDB Server and Remote Debugging

An Eclipse Debug Example
Other Debug and Test Tools
Other System-Level Debug Approaches
Process & Threads Management
What are Processes and Threads?
Virtual Memory Mapping
Creating and Managing Processes and Threads
Thread-Specific Data (TSD) POSIX
The Native POSIX Threading Library (NPTL)
Kernel Threads

Signals
System Calls
Scheduling
Linux 2.4 and 2.6 Scheduling Models
The O(1) Scheduler
The Completely Fair Scheduler (CFS)

Synchronization
Via Global Data
Via Semaphores, Files and Signals

Inter-Process Communications (IPC)
Message Queues
Semaphores Revisited
Shared Memory
Pipes, FIFOs and Futexes
Remote Procedure Calls
Networking

Error Handling
errno and perror
strerror and strerror_r
oops, panics and Segmentation Faults
Timing
How Linux Tells Time
Kernel, POSIX and Interval Timers
High-Resolution Timers (HRTs)

Memory Management and Paging
Demand Paging and Virtual Memory
Allocating User and Kernel Memory
Mapping Device Memory
The Slab Allocator
The OOM Killer
Memory in Embedded Systems

Modularization
Creating a Module and Module Loading
Dependency Issues
In Embedded Systems

Shared Libraries
A Shared Library Example
Static and Dynamic Libraries

The I/O Subsystem: A Tale of Two Models
The Original Device Driver Model
The Standard I/O Interface
The New Device Driver Model and Kernel Object Classes
Initialization
Platform Devices, Busses, Adapters and Drivers
Comparing the Two Models

Embedded Linux Trends
Development, Monitoring and Testing

Some Final Recommendations

Lecturer:
Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based development tools, training and consulting for the embedded systems market.

http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/

Simulink Model based FPGA Digital Design and Digital Signal Processing

Time & Date: Course postponed until fall 2017

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speakers: Cherif Chibane, Rick Rosson; MIT Lincoln Laboratory

Description:

Over the last 30 years, applications for Field Programmable Gate Array (FPGA) designs have increased exponentially. FPGA's have moved from just digital designs to other areas such as embedded controllers, Digital Signal Processing, communication systems, and configurable computing. This has made exposure to and mastery of FPGA design crucially important for many people in industry and academia.

This course provides a detailed overview of FPGA technologies, a top-down design workflow, modeling and simulation, standard design tools, and applications. Using a mixture of theory and hands-on laboratories, the course provides students what they need to know in modeling, simulation, design, verification, and implementation of multi-disciplinary applications targeting FPGA's. This course provides plenty of hands-on lab exercises to reinforce the key concepts. While the material covered in this class targets Xilinx devices, it can be easily used for others devices such as ALTERA and other FPGA devices.

Presenters:

This course will be jointly presented by Cherif Chibane and Rick Rosson of MIL Lincoln laboratory. Their combined and complementary expertise will greatly benefit attendees from industry and academia.

Cherif Chibane is currently with MIT Lincoln laboratory as a research staff. He was one of the early adopters of FPGA's for configurable computing. Prior to MIT-LL, he was part of the BAE Systems team that pioneered the use FPGA's for Software Denied Radio (SDR). He has more than 25 years in the design of advanced configurable computing using FPGA's for DSP, digital logic, and embedded designs.

Rick Rosson is a senior modeling and simulation engineer at MIT Lincoln Laboratory. Prior to joining MIT-LL, Rick served as a senior applications engineer at MathWorks for 9 years, with a focus on digital signal processing, statistical signal processing, embedded systems design, modeling and simulation, and data analysis and visualization. Rick holds a Master of Science in Electrical Engineering from Boston University and a Master of Science in Management from the MIT Sloan School of Management.

Agenda

Session #1

- Course Overview
- Model based benefits in today's FPGA designs.
- Simulink/Matlab Overview
- Simulink Examples

Session #2
• FPGA Technologies Overview
• Xilinx ISE Overview
• Fixed point Vs floating point overview
• HDL/FPGA Examples

Session #3
• Preparing Simulink models for HDL code generation
• Generating HDL code from Simulink
• Verifying the generated code
• Code Generation Examples

Session #4
• Modeling Signal Processing and Communications Systems in Simulink®
• Signal Processing Examples
• Implementing Signal Processing Systems on FPGA's

Session #5
• Advanced Topics using FPGA's
• End-To-End Design and Verification
• End-To-End Design Example
• Course Summary

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gamil.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Patenting Outside of the U.S.

Date & Time: 6 – 9PM, Monday, October 23

Location: Tufts University, Halligan Hall, Room TBD., 161 College Ave, Medford, MA

Speaker: Christine Kuta, Kuta Intellectual Property Law, LLC

Course Overview: Most countries in the world have a patent office where one can apply for protection of inventive ideas. There is, however, no global patent that provides rights everywhere. Operating in the global economy, though, requires some patent protection beyond the U.S. borders. Therefore, understanding the systems and strategies for determining how and where to apply for protection outside the U.S. is critical for operating in the global economy. This class will provide information about systems and strategies for obtaining patent protection outside the U.S.

Description: The class will provide an overview of the laws and requirements, and explain the procedures in obtaining foreign patent rights. International treaties such as the Patent Cooperation Treaty (PCT) will be discussed. The PCT enables the applicant to begin the patent process in most of the world's countries simultaneously. The European Union (EU) unitary patent, the first multinational patent, and unified patent court will also be discussed. The EU unitary patent and the unified court have been in development for a number of years and is about to launch despite delays caused by Brexit. Foreign filing rights are easy to lose and costs can be difficult to contain, however, the class will also provide some strategies for effective foreign filing in spite of the difficulties.

Target Audience: Engineers in large and small companies with new ideas, inventors, entrepreneurs seeking to develop a patent strategy, anyone interested in learning about patents and how to obtain a patent outside the U.S.

Benefits of attending: Understanding the process and requirements for obtaining a foreign patent; information about how to leverage U.S. patents rights in the foreign application process; understanding the procedures in order to make effective business decisions and contain costs. Course will include handouts including a list of resources.

Course outline:

I. Patents

A. Quick overview of what patents protect and why patent protection should be pursued.

B. High level view of process

C. Foreign filing license

II. Foreign patents

A. Basis for foreign patent protection

B. Representation

C. Differences in the process as compared to U.S.

- i. Patent eligibility
- ii. Inventorship
- iii. Patent Types
- iv. Process
- v. Fees

III. International applications – i.e., starting the foreign application process in many countries at once

A. Patent Cooperation Treaty

B. Regional applications

IV. The Unitary Patent and Unified Patent Court -- new developments in the Old World

A. What it is and how it works

B. Proposed dates of implementation
C. Filing options

V. Protection strategies

VI. A few words about enforcement

Christine Kuta is an Intellectual Property lawyer. Her practice includes Intellectual Property strategy, portfolio development and management, and patent and trademark prosecution, search and opinions. Ms. Kuta counsels clients in a wide variety of technical areas including computer systems and software applications, medical devices, lighting systems, optics, materials and manufacturing processes, complex data management systems, electronics, energy management systems and energy storage including fuel cells, mechanical devices and consumer products including clothing and accessories.

Decision (Run/Cancel) Date for this Course is Monday, 16, 2017

Payment received by October 12
IEEE Members $50
Non-members $60

Payment received after October 12
IEEE Members $60
Non-members $70

Registration will be Online as of Augsut 1, 2017

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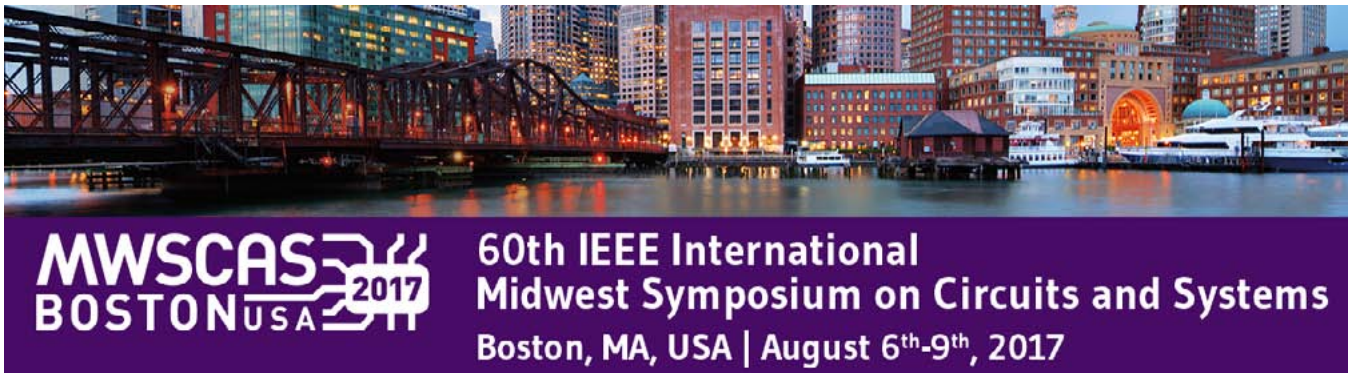


Register at mwscas2017.org

Register before July 6 for special rates

The 60th IEEE International Midwest Symposium on Circuits and Systems will be held on the Medford/Somerville campus of Tufts University, August 6 - 9, 2017. MWSCAS 2017 will include oral and poster sessions, student paper contest, tutorials given by experts in circuits and systems topics. Visit the conference website for full details.

Sessions

- Analog and Mixed-signal Circuits & Systems
- Digital Circuits and Systems
- Circuits & Systems for Communications
- RF and Wireless Circuits and Systems
- Technologies for Smart Sensors
- Sensor Fusion
- Converter Circuits and Systems
- Image & Multi-dimensional Signal Processing
- Biomedical and Life Science Circuits & Systems
- Photonics & Nanoelectronics
- MEMS/NEMS
- Energy Harvesting & Power Management
- Trust & Authenticity
- System Security Architecture
- Reconfigurable Circuits & FPGA Applications

Keynote Speakers:

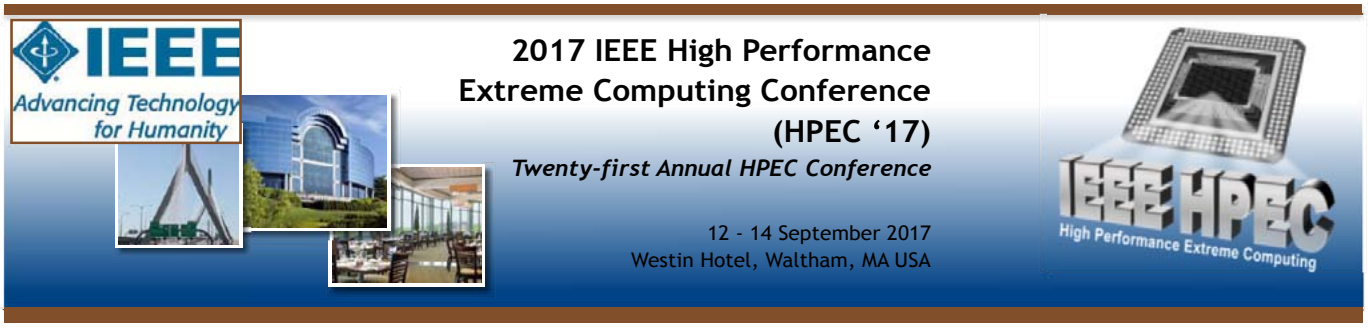
- Dr. Linton Salmon, DARPA
- Dr. Donhee Ham, Harvard University
- Dr. Jesse Wheeler, Draper

Tutorials

- Supercapacitor Based Embedded Energy Harvesters
- IC Power Management Circuits and Systems with Emphasis for Portable Devices
- Switching Noise Mitigation for Integrated DC-DC Converters
- Hybrid Microfluidic CMOS Systems for Life Science Applications
- Ultra-low Power/Energy SRAM Design for Internet-of-Things
- Signal Integrity Challenges in Emerging DDR Technologies
- Synthesis of BTI Reliable CMOS VLSI Systems in Nanometer Technologies
- Neuromorphic and Compressing Computing Circuits and Systems

Special Sessions

- Internet of Things: Sensors to Cybersecurity
- Emerging Neuromorphic Circuits for Enabling Deep Neural Networks
- Analog and Digital Circuit Design for the Internet of Everything
- Emerging Bio-interface Technologies for Life Science Applications



HPEC 2017

[Register Now!](#) [Preliminary Agenda Preview](#)

HPEC is the largest computing conference in New England and is the premier conference in the world on the convergence of High Performance and Embedded Computing. We are passionate about performance. Our community is interested in computing hardware, software, systems and applications where performance matters. We welcome experts and people who are new to the field.

Highlights Include:

Keynote Speakers

Dr. Ivan Sutherland (ACM Turing Award; IEEE John von Neumann Medal; NAE Fellow; NAS Fellow; ACM Fellow) - Clockless Computing
Mr. Andreas Olofsson (Program Manager - DARPA MTO) - Intelligent Design Automation, System Optimization, and Open Hardware

Invited Speakers

Mr. Trung Tran (Program Manager - DARPA MTO) - Machine Learning, Data Analytics, and Non-Conventional Computer Architecture
Dr. Merri Sanchez (AIAA Fellow; Chief Science and Technical Advisor - Air Force Space Command)
Prof. Barry Shoop (2016 IEEE President; Electrical Engineering Chair - United States Military Academy) - Innovation as an Ecosystem
Prof. Saman Amarasinghe (MIT Computer Science & AI Laboratory) - Making Sparse Fast
Prof. David Bader (IEEE Fellow; AAAS Fellow; Georgia Tech - Chair School of Computational Science and Engineering) - Massive-Scale Streaming Analytics
Dr. John Feo (Director - Northwest Institute for Advanced Computing) - HAGGLE – Hybrid Attributed Generic Graph Library Environment
Mr. John Goodhue (Executive Director - Massachusetts Green High Performance Computing Center)
Dr. Jeremy Kepner (MIT Lincoln Laboratory Fellow; Founder Lincoln Laboratory Supercomputing Center) - Convergence of Machine Learning, Big Data, and Supercomputing
Dr. Mark Ritter (Distinguished Research Staff - IBM Physical Sciences) - Heuristic Quantum Variational Algorithms on a Small Quantum Computer
Dr. Michael Vai (MIT Lincoln Laboratory Secure, Resilient Systems & Technology) - Bridging System Functionality and Cybersecurity

Special Events

GraphBLAS forum to define standard building blocks for graph algorithms; organizers: Dr. Aydın Buluç (Lawrence Berkeley National Laboratory); Dr. Scott McMillan (CMU Software Engineering Institute); Dr. Marcin Zalewski (Pacific Northwest National Laboratory)
Massachusetts and Exascale Computing; organizers: Dr. Chris Hill (Principal Research Engineer - MIT) & Prof. Patrick Dreher (North Carolina State)
Integrating Quantum Computing with High Performance Classical Computing; organizers: Dr. Tim Braje (MIT Lincoln Laboratory) & Dr. John Cortese (MIT Lincoln Laboratory)
Secure and Resilient Computing; organizers: Dr. Michael Vai (MIT Lincoln Laboratory Secure Resilient Systems & Technology) & Dr. George Kalb (JHU Information Security Institute)
OpenSuperComputing BoF; organizer: Mr. Kurt Keville (MIT ISN)

Tutorials

BigDAWG Big Data Working Group Tutorial; organizers: Dr. Vijay Gadepally (MIT Lincoln Laboratory Supercomputing Center), Kyle O'Brien (MIT Lincoln Laboratory Intelligence and Decision Technologies)
Introduction to CUDA and Machine Learning; Dr. Larry Brown (Solutions Architect - NVidia)
OpenMP programming; Dr. Tim Mattson (Principal Engineer - Intel)
Mathematics of Big Data: Spreadsheets, Databases, Matrices, and Graphs; organizer: Dr. Jeremy Kepner (MIT Lincoln Laboratory Supercomputing Center)

Presentations will be represented in the following topics:

High Performance Data Analysis
Machine Learning
Advanced Multi-core Software Technologies
Case Studies and Benchmarking of Applications
Automated Design Tools
Mapping and Scheduling of Parallel and Real-Time Applications
Computing Technologies for Challenging Form Factors
ASIC and FPGA Advances
Open System Architectures
Data Intensive Computing
Big Data and Distributed Computing
Interactive and Real-Time Supercomputing
Graph Analytics and Network Science
Fault-Tolerant Computing
Embedded Cloud Computing
Digital Front Ends
General Purpose GPU Computing
Advanced Processor Architectures

Quick Links:

- HPEC Home Page
- Committee
- Preliminary Program
- Conference Registration
- Conference Venue

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