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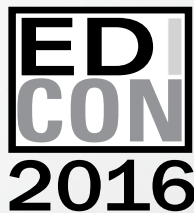
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IEEE Boston Section Online Courses:

Verilog101: Verilog Foundations

CLASS DESCRIPTION: Verilog is IEEE standard 1364. It is a Hardware Description Language that is the corner stone of much of the simulation world. Verilog Foundations is a comprehensive introduction to the IEEE 1364 (Verilog). The Verilog Foundations class has a slightly different approach to learning Verilog than other methods. There is a lecture section for each main topic. This presents a basic foundation for the language. There are nearly 100 labs/examples giving comprehensive "how to" examples of most Verilog language constructs. There are working solutions for each lab. All the work can be done independently by the engineers, at their own computer, and at their own pace. **Register at <http://www.ieeeeboston.org> and click on course title**

System Verilog 101: Design Constructs

CLASS DESCRIPTION: SytemVerilog is an extensive set of language constructs to the IEEE 1364-2001 standard. It's meant to aid in the creation and verification of models. There are over 100 labs/examples giving comprehensive "how to" examples of most SystemVerilog language constructs. There are working solutions for each lab and the students can use the lab database for developing their own models later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace. There are self-grading quizzes for each chapter that allow the student to see if he/she is learning the material. The lab database you will be able to download and is yours to keep. **Register at <http://www.ieeeeboston.org> and click on course title**

System Verilog 102: Verification Constructs

CLASS DESCRIPTION: SytemVerilog is an extensive set of language constructs to the IEEE 1364-2001 standard. It's meant to aid in the creation and verification of models. SV102, this class, covers verification constructs. SystemVerilog102, like all CBE classes, is lab based. There are over 30 verification labs/examples giving comprehensive "how to" examples of most SystemVerilog verification language constructs. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace. **Register at <http://www.ieeeeboston.org> and click on course title**

Introduction to Embedded Linux Part I

CLASS DESCRIPTION: This first of a 2-part series introduces the Linux Operating System and the use of Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part covers the methods for booting Embedded Linux distributions including embedded cross-development and target board considerations. **Register at <http://www.ieeeeboston.org>**

High Performance Project Management

CLASS DESCRIPTION: This 12 hour course (broken into short 10 to 20 minute independent modules) provides the project methodology, concepts, and techniques that ensure successful completion (on time, on budget, with the quality required) of projects, large and small. Participants learn the steps to take before, during, and at the end of a project to hone planning and execution to a strategically built process that delivers project success when used. **Register at <http://www.ieeeeboston.org>**

The Fog of Innovation

Kevin Flavin, 2016 Chair, IEEE Boston Section



It is November for me.
It is January for you.

As of this writing, Samsung has agreed to pay Apple a half-billion \$US to settle claims of misuse of intellectual property. Fed Chair Yellen and the Federal Reserve are threatening to raise rates in December. Terrorism continues to evolve into new forms, fuel

prices are dropping, the USD is stronger, personal drones are getting cheaper, and the will Chinese Yuan become a reserve currency in months.

Does Samsung's agreement signal a time of technical dust settling? Intellectual Property claims are getting straightened out, the great 'who owns what, where and when' is being decided. Is this an indication that massive innovation has slowed?

We are in the midst of digesting the changes in technology, and this inevitably improves our economic productivity. With productivity gains, we should see an increase in the economic production and expansion. It usually does. Hopefully. But is this time different; is this why Fed Chair Yellen has decided (with the other Fed Directors) to increase rates? Will this be the trigger for another recession? Only our future selves will know.

In addition to being an engineer, I am a marketer, so I listen to different wires than a typical engineer or scientist. On an immediately local level, Constant

Contact was scooped up - and so begins the consolidation of technology companies on the margins of industry. Meanwhile, a few hundred miles away, Yahoo is deciding to spin-out a part of their business. Naturally, since an ex-Gogler is running the ship there, there is a strong impulse to compare to Google and ask, "What would Google do?" Let the second-guessing begin!

This may be the pessimist speaking but these are all indicators of dust settling - reorganizing - re-categorizing - wealth creation without technical creation. I can't help but think about Richard Gere's Edward Lewis (Pretty Woman) piling up the glasses from the conference table dreaming of building ships.

On the other hand, we may still be in the fog and haze of an innovation cycle. A little more than ten years ago, Apple launched the non-Mac-only iPod. A little more than eight years ago, the iPhone was launched - and we are still innovating on that platform and similar. Notably, the use of an iPhone and other smart phones to control devices, i.e. drones, may be the next phase of innovation. Smart Phones as platforms for innovations in robotics, virtual reality and augmented reality seems like a natural next step. If Facebook users can manage a farm in a game, how far away is the idea of combining a game with augmented reality and 'Internet of Things' for real gamers to manage small crops (maybe without them realizing?). Is this the first step to The Matrix, where we are the overlords of...ourselves?

Considering the increasing impact of technology innovation on that last 30-40 years, we can see specific points of innovation that caused massive economic impact, e.g. the digital computer, personal computer, mobile phone, public access to the in-

ternet, GPS, cheap batteries, solar cells, etc. Each successive innovation, building on the past, seems to have a diminishing level of impact.

If the current trend continues, will our massive innovations hide amongst the news and distractions, only to be discovered by accident, over a longer period of time, as the innovations become part of the fabric of our normal lives, possibly becoming the 'platform' for further innovation? Will innovations happen and we won't even notice? Will innovations be incremental, take the form of platforms for making the changes we need to do? Will the 'innovation' come from the use of the innovations? Will the 'innovation' be solving problems of an environmental impact of humanity? Will a human flight to Mars spark the next wave of innovation: in propulsion, energy development and use, agriculture, human behavior, and poetry and literature? Or maybe, like today, the massive innovations of the past where

simply trying to solve an unrelated or smaller problem? Maybe the creation of the digital computer was simply (but not simple) to solve the need for radar to look beyond the horizon?

Maybe we need to believe that every little innovation, no matter how periphery, matters. Maybe not now, or soon, or substantively, but it does. It does matter.

Where are you on the innovation arc? Do you foresee the impact your work is creating for the future? We're engineers and scientists - working toward the future is what we do, we are very lucky to hold that responsibility. Our work matters. You matter.

So, welcome to 2016. I hope your 2016 builds on last year. I hope your next year is something that you can build on next year. All the best of luck and good fortune to you.

IEEE Boston Section Social Media Links:

Twitter: <https://twitter.com/ieeeboston>

Facebook: <https://www.facebook.com/IEEEBoston>

YouTube: <https://www.youtube.com/user/IEEEBostonSection>

Google+: <https://plus.google.com/107894868975229024384/>

LinkedIn: <https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about>



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Phased Array Systems and Technology
Revolutionary Developments in Phased Arrays



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18–21 October 2016

Westin Waltham Hotel, Greater Boston, Massachusetts, USA

www.array2016.org

About the Symposium

Phased array systems continue to be a rapidly evolving technology with steady advances motivated by the challenges presented to modern military and commercial applications. This symposium will present the most recent advances in phased array technology and present a unique opportunity for members of the international community to interact with colleagues in the field of Phased Array Systems and Technology.

Suggested Topics:

- System Architecture
- Aperture Design
- Antenna Elements
- Beamforming Techniques
- T/R Modules
- Signal Processing for Arrays
- Array Measurements
- Advanced Materials
- Packaging and Manufacturing
- Applied Computational Electromagnetics



Special Sessions

Please provide suggestions for special sessions to the Technical Program Chair at info@array2016.org

Paper Template and Submission Procedures

Template and submission procedures are available at

www.array2016.org/forauthors.htm

Publication Information

All accepted papers will be published on the conference CD-ROM and distributed to conference attendees. Selected papers meeting the publishing requirements will be published in IEEE Xplore as part of the IEEE Conference Publication Program.

Important Dates:

Summary (~1000 words + figures)	01 Feb 2016
Notification of Acceptance	15 Mar 2016
Final Papers (8 page max)	01 Jul 2016

Conference Committee

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Entrepreneurs' Network - 6:30PM, Tuesday, 5 January

Product Development in Life Science & High Tech Startups

Whether you want to sell a new kind of vehicle or a new app, you've got to develop your idea into a real product that customers are willing to pay for. Do you try to develop the product in house or do you outsource the development? How do you fund your product development? How do you make sure you're developing the right product for your market?

The panelists have broad and deep experience in developing many different types of products in life sciences and high tech fields and will offer guidance in matching your product to your market, practical suggestions for making the most of your development budget, and effective advice for avoiding product development pitfalls. And share a few stories from their own product development adventures. One of our speakers is a serial entrepreneur, inventor and Founder of a product development company focused on high tech fields, another is serial entrepreneur and CEO and angel investor in a broad array of life science ventures and our third speaker is a co-founder, co-inventor and CEO of a company that developed a product from scratch that it has successfully commercialized, building a team and obtaining investment along the way. Our moderator is a recognized attorney for startup companies and is the ENET



Chairman. Speaker: Steve Owens, founder of Finish Line PDS (www.finishlinepds.com)

Steve has over 30 years of successful product development experience in many different industries and is a sought-after adviser and speaker on the subject. Steve has founded four successful start-ups and holds more than twenty-five patents. Steve has worked for companies such as Halliburton and Baker Hughes. He has experience in the Internet of Things, M2M, oil and

gas, and industrial controls. Steve's insight into the product development process has generated millions of dollars in revenue for start-ups and small businesses. Finish Line PDS provides product and technology development management, mechanical design, and development of electronics, firmware and sensors, as well as design verification testing and other services. Finish Line PDS is a proud sponsor of the Boston ENET. https://twitter.com/FinishLine_PDS



Speaker: Richard Gill, PhD, Board Director and Investor, Launchpad Venture Group

<http://launchpadventuregroup.com/>

Dr. Gill is a seasoned entrepreneur, CEO, investor, and board member.

He is a longtime investor and director at Launchpad Venture Group, the largest angel investing group in the Northeast. Dr. Gill is active on the board of several startups. Dr. Gill's most recent operational role was President & CEO of TruTouchTechnologies, an alcohol testing and biometric device company, where he remains a board member. Prior to that he has been President & CEO at Genome Therapeutics, ActiveCyte, AnVil, Signet and ProNAi. He also held executive positions at Unilever and British Technology Group. He has executed business strategies, moved candidates into clinical trials, overseen M&A activities and much more. His degrees are in Physiology and Biochemistry, Chemistry plus a PhD in Endocrinology.



Speaker: Molly Farison, Co-founder and CEO at Lilypad Scales, <http://www.lilypadscales.com>

Molly is an experienced electrical engineer and product developer with significant product development history. She has experience in consum-

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er and healthcare markets working with factories in the U.S. from starting her present company, Lilypad Scales, which developed from scratch a functional and durable product with 5-star reviews on Amazon.com. Molly also led two capital raises and gave presentations that landed her company a spot in MassChallenge in 2013 and won the Babson BETA Challenge (\$20k prize) in 2014. Molly manages an interdisciplinary team that has included engineers, doctors, salespeople, and graphic designers. Molly had prior work experience at Altaeros Energies, Rockwell Automation and NASA. She graduated Olin College of Engineering, with a B.S., Electrical and Computer Engineering, and was co-inventor on the patent relating to Lilypad Scales' first product, the Lilypad Scale for Manual Wheelchairs.



Moderator: Robert Adelson, business and tax attorney, partner at Boston law firm of Engel & Schultz LLP (www.ExecutiveEmploymentAttorney.com), and Chairman of IEEE Boston Entrepreneurs' Network. Rob has been an attorney for over 30 years specialized in business, tax, stock and options,

employment, contracts, financings, trademarks and intellectual property. Rob began as an associate at major New York City law firms before returning home to Boston in 1985 where he has since been a partner in small and medium sized firms before joining his present firm in 2004. Rob represents entrepreneurs, start-ups and small companies, independent contractors and employees and executives. Rob is a frequent speaker on business law

topics and author of numerous articles published in Boston Business Journal, Mass High Tech and other publications. He has been named among the "Top 20 Boston Startup Lawyers" by Chubby-Brain.com, a website that provides tools for entrepreneurs. Rob has been on the ENET Board since 2002 and Chairman since 2009 and is also a Co-Founder and Board member of the 128 Innovation Capital Group. He holds degrees from Boston University, B.A., summa cum laude, Northwestern University (Chicago), J.D., Law Review, and New York University, LL.M. in Taxation.

Meeting Location: Constant Contact, Inc., Reservoir Place, Main Building InnoLoft Great Room, 1st Floor, 1601 Trapelo Rd., Waltham, MA (Exit 28B, I-95/Route 128)

Pre-meeting Dinner at 5:15 PM (sharp) at Bertucci's, Waltham, (Exit 27B, Route 128) Check for Updates at: Boston Entrepreneurs' Network Website at (<http://www.boston-enet.org>). Directions: <http://www.constantcontact.com/about-constant-contact/office-location-waltham.jsp>

Reservations: ENET Constant Contact meetings are free to ENET members and \$20 for non-members. No reservations are needed for the dinner. To expedite sign-in for the meeting, we ask that everyone -- members as well as non-members -- pre-register for the meeting online. Pre-registration is available until midnight the day before the meeting. If you cannot pre-register, you are welcome to register at the door.

Robotics and Automation Society – 6:00PM, Tuesday, 12 January

Development of "CorPath", the first surgical robot in production for Percutaneous Coronary Intervention, and the constructive methods used in its design

Dr. Nicholas Kottenstette & Brett Prince

Minimally invasive surgical robotic systems are typically classified as Class II medical devices by the FDA. The CorPath is the only robotic-assisted

percutaneous coronary intervention (PCI) System cleared by the FDA. As such, the CorPath has cleared a rigorous verification and validation pro-

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cess in order to achieve FDA approval. This process includes verifying the embedded control software used to control the robotic drive system.

Model based methods are presently being used to both simulate and deploy control software for our next generation robotic systems. Specifically the embedded control software has been derived using constructive methods in order to provide rigorous stability analysis which can be verified in deployment. We shall first provide an overview of Corindus Vascular Robotics and its flagship CorPath product. We shall then provide a more general discussion on how constructive methods can be used for networked control of robotic systems.

Constructive methods typically exploit physical properties of the system in order to construct low complexity controllers which in practice are easy to tune and robust to system uncertainty. Typically the discrete time implementation of the respective control system can be achieved at modest sampling rates. However, when lower sampling rates and significant time varying delays need to be considered then digital control networks consisting of wave variables can be used to control interior conic dissipative systems. Robotic systems are a special class of interior conic dissipative systems in which we shall demonstrate force feedback telemanipulation architectures which allows one to (in)directly exchange position information.

Dr. Nicholas Kottenstette is currently the Principal Control Systems Engineer at Corindus Vascular robotics. A senior member of IEEE, he holds a MS from the Mechanical Engineering Department at MIT and a PhD in Electrical Engineering from The University of Notre Dame. His research develops constructive resilient networked control principles for Cyber Physical Systems. The principles he has developed apply to nonlinear affine systems, including medical robotic systems, fixed wing aircraft, quadrotor aircraft, robotic, thermal, semiconductor

manufacturing, alternative energy generation, digital signal processing, and suspension systems. He has authored or coauthor of over 50 publications, including 14 US patents.

Brett Prince joined Corindus in September 2012, bringing significant Sales and Marketing experience, as well as his experience as Director of Product Management at Precision Therapeutics. While at General Electric he held a variety of sales and marketing leadership roles in both the life-sciences and imaging divisions. Mr. Prince holds a B.S. in Materials Science and Engineering from Cornell University and an M.B.A. from MIT Sloan.

Have more questions? Want to share a drink with the speaker? Want to network with fellow engineers and professionals? Just want to chat about the current goings-on in Robotics, or technology in general? Join us for dinner, where you can talk about Robotics in a more casual setting!

UNHOSTED DINNER

**Bertucci's, 1257 Highland Ave.,
Needham, MA 02492**

GENERAL INFORMATION

This and other RAS meetings are open to the general public. For more information about the RAS Boston Chapter, contact Chapter Chair Andy Vidan at chair@robotics-boston.org or visit <http://www.robotics-boston.org/>.

To assist us in planning this meeting, please pre-register at <http://www.ieeeboston.org/Register/>

**Doors open: 6:00 P.M.; Presentation: 6:30 P.M.;
Dinner: 8:00 P.M.**

Olin College, 1000 Olin Way, Needham, MA 02492; Milas Hall Auditorium

Life Members – 4:00PM, Wednesday, 13 January

Estate Planning, Wills, Trusts and Taxes

Estate Planning, Wills, Trusts and Taxes: Attorney Chew will discuss the components of a basic estate plan, which protects and preserves the goals and wishes of an individual through incapacity and post-death. She will then delve into a comparison between Wills and Trusts, explaining what typically dictates the usage of the latter instead of relying on the former. An outline of the probate process will be provided, as well as tips and tricks to avoid common pitfalls and to simplify the work to be done when someone dies. Finally, she will explain the roles played by the various relevant taxes--capital gains, income, and estate.

Nancy specializes exclusively in estate planning and elder law, and she has been in private practice since 1999. As an estate planner, Nancy provides particular expertise to clients with minor or disabled children, with taxable estates, and with ownership interests in business entities. In the field of elder law, Nancy possesses current and accurate knowledge of a complex area subject to an ever-changing regulatory climate. She is a member of the National Academy of Elder Law Attorneys – including its Massachusetts Chapter—as well as the Massachusetts Bar Association and the North Middlesex Bar Association. She is also an accredited attorney with Veterans Administration.

Nancy Catalini Chew is a graduate of Boston College Law School and was admitted to practice in Massachusetts in 1996. She earned her Bachelor of Arts degree in Geography, summa cum laude, from the University of New Hampshire, and she is a member of Phi Beta Kappa.

Nancy is frequently asked to speak at local Councils on Aging, Chambers of Commerce events, facilities for the elderly, and she has been featured on various local access cable television programs, all in an effort to educate the public with accurate information.

Nancy has served on the Board of Trustees for an area hospital and is also a member of its Ethics Committee. She has acted as a board member for various charitable entities, and currently acts as Town Moderator in her home town of Ashby, where she currently resides with her husband and their children.

For additional information, please visit her website: <http://www.attycatalinichew.com/> or contact her: email: attychev@attychev.com

The meeting will be held at the Lincoln Lab Auditorium, 244 Wood Street., Lexington, MA at 4:00 PM. Refreshments will be served at 3:30 PM. Registration is in the main lobby. Foreign national visitors to Lincoln Lab require visit requests. Please pre-register by e-mail to reception@ll.mit.edu and indicate your citizenship. Please use the Wood Street Gate.

For directions go to <http://www.ll.mit.edu/>; for other information, contact Steve Teahan, Chairman, at (978)763-5136, or Steve.F.Teahan@raytheon.com

To assist us in planning this meeting, please pre-register at <http://www.ieeeboston.org/Register/>.

Reliability Society – 5:30PM, Wednesday, 13 January

Reliability Growth Test

Planning and Data Analysis: What are the Real Final Results?

Milena Krasich of Raytheon IDS



Reliability growth of hardware through test and analysis has been a valuable industry tool for improvement of reliability of products for several decades. To provide a measure of this improvement, several mathematical models have been developed.

Two of the well-known models for planning and monitoring of reliability growth are Duane, known as graphical methodology, and AMSAA /CROW, known as analytical model. Regardless, the fact is that the two models are based on the same principle, but contain a serious error in planning of the test duration and consequently in test data analysis, reporting of the results, and the measure of reliability improvement.

The presentation will show how this mathematical -- and also theoretical -- error, unaddressed for decades, leads to incorrectly planned test duration and unrealistic overestimate of achieved reliability improvement.

Milena Krasich is a Senior Principal Systems En-

gineer in Raytheon Integrated Defense Systems, Whole Life Engineering in RAM Engineering Group, Marlborough, MA. Prior to joining Raytheon, she was a Senior Technical Lead of Reliability Engineering in Design Quality Engineering of Bose Corporation, Automotive Systems Division after her five-year tenure at the Jet Propulsion Laboratory in Pasadena, California. While in California, she was a part-time professor at the California State University Dominguez Hills, graduate school, and the Cal Poly Pomona, undergraduate programs. She holds a BS and MS in Electrical Engineering from the University Of Belgrade, Yugoslavia, and is a California registered Professional Electrical Engineer. She is Technical Advisor (Chair) to the US Technical Advisory Group (TAG) of the IEC Technical Committee, TC56, Dependability.

Meeting Location: MIT Lincoln Laboratory, 3 Forbes Road, Lexington, MA 02420

Admission: No charge.

To assist us in planning this meeting, please pre-register at
<http://www.ieeeboston.org/Register/>.

2016 IEEE International Symposium on Phased Array Systems & Technology
 October, 18 - 21 2016
www.array2016.org
(Abstract submission deadline, February 1, 2016)

Save the travel costs and participate in these IEEE conferences held locally.

2016 IEEE High Performance Extreme Computing Conference
 September 13 - 15 2016
www.ieee-hpec.org
(Abstract submission deadline is May 16, 2016)

2016 IEEE Symposium on Technologies for Homeland Security
 May 10 -12 2016
www.ieee-hst.org
(Abstract submission deadline is January 4, 2016)

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Photonics Society Meeting – 6:30PM, Thursday, 14 January

Recent advancement of LDPC Codes for High-speed Optical Communications

Dr. Toshiaki Koike-Akino - Mitsubishi Electric Research Laboratories



Low-density parity-check (LDPC) codes have been one of essential sub-systems to realize near error-free fiber-optic communications. In this seminar, we introduce recently developed design/decoding methods to improve performance of LDPC codes suited for low-power optical communications.

Toshiaki Koike-Akino received the B.S. degree in electrical and electronics engineering, M.S. and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 2002, 2003, and 2005, respectively.

During 2006–2010, he was a Postdoctoral Researcher with Harvard University, and since 2010, he has been with Mitsubishi Electric Research Laboratories, Cambridge, MA, USA. His research interests include digital signal processing for data communications and sensing. He received the IEEE GLOBECOM'08 Best Paper Award and the IEEE GLOBECOM'09 Best Paper Award.

This meeting begins at 6:30 PM Thursday, Janu-

Entrepreneurs' Network Cambridge Meeting – 6:00PM, Tuesday, 19 January

Incubator, Accelerator and Shared Work Spaces Expo

Meeting location: Microsoft NERD Center, 1 Memorial Drive, Cambridge, MA

Like last year, the Boston Entrepreneurs' Network offers our annual Expo of accelerators, incubators, and co-working spaces who will showcase rapid development options to entrepreneurs in the Greater Boston Area. We at ENET hope that you will join us at our Expo this year!

ary 14th, 2016 and will be located 3 Forbes Road (an MIT Lincoln Laboratory facility), Lexington, MA, 02420. The meeting is free and open to the public. All are welcome. Prior to the seminar there will be social time and networking from 6:30 – 7:00PM. Dinner will also be provided. The seminar will begin at 7:00PM.

For more information contact Jade Wang, Boston IEEE Photonics Society Chapter chair at jpwang@ll.mit.edu, or visit the Boston IEEE Photonics Society website at www.bostonphotonics.org.

Directions to Forbes Rd Lincoln Laboratory: (from interstate I-95/Route 128). Take Exit 30B onto Marrett Rd in Lexington – Merge into left lane. Make the first Left onto Forbes Rd.

Proceed straight through the small rotary and enter the parking lot. The entrance is on your right.

To assist us in planning this meeting, please pre-register at

<http://www.ieeeboston.org/Register/>.

The Expo will be held on Tuesday, January 19, 2016, 6-9 p.m. at the Microsoft New England Research and Development Center (NERD), 1 Memorial Drive, Cambridge, MA. The NERD is within easy walking distance of the Kendall Square Red Line T Station. Beverages and pizza will be served. Last year, over 100 entrepreneurs attended the event and more than 20 incubators exhibited.

Each exhibitor will host a table with up to two rep-

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representatives to answer your questions, distribute promotional materials and business cards. During the Expo, exhibitors will have up to 2 minutes to present their elevator pitch in front of the attendees.

Come and join us on January 19th for a great chance to meet New England's leading entrepreneurial business incubators. In addition, you can network with other founders and participants who, like you, are on their way to the top!!



Meeting Co-Organizer: Christina J. Inge, is the founder of ThoughtLight and is the CEO of Sleek Marketing University, www.sleekmarketingu.com. Twitter: @christinainge, LinkedIn: <http://www.linkedin.com/in/christinainge>

Christina is a marketing consultant with over 20 years experience in content creation, web technologies, and project management. Her areas of expertise include the design of social media marketing campaigns that boost brand recognition and affiliation. Through best practices SEO, she teaches methods that enhance click-through experiences, improve conversion rates and increase organic search rankings. She helps companies with product go-to-market plans, email marketing strategy and implementation, online lead conversion and lead generation analysis and optimization, and product positioning.

Through Sleek Marketing University she teaches the latest digital marketing techniques to help startups, businesses, and nonprofits reach new audiences cost-effectively. Subjects addressed include SEO, Google Analytics, social media, marketing automation and many others.



Meeting Co-Organizer: Maureen Mansfield, ALM, Chief Contract Officer, MANSFIELD LAW, MANSFIELD LAW, Twitter: @MaureenManALM.

Maureen Mansfield, ALM, is a business development, corporate development, and strategy professional for companies in the the private and public sectors. Currently, Maureen is at Mansfield Law where she works with entrepreneurs, inventors, artists, startups, and emerging growth companies. Previously, she cofounded a boot strapped startup that has progressed to a \$10 million term sheet agreement. She currently serves as an advisor and mentor for several startups and related entrepreneurial ventures. She is a member of the Executive Board of The Boston Entrepreneurs' Network (Boston ENET), where she leads Alliance Partnerships.

Prior to joining Mansfield Law in 2009, Maureen was a New England Director of Business Development for the award-winning firm Syska & Hennessy, Inc., With S&H, she focused on business development and corporate management strategy for major accounts locally, nationally, and internationally. After helping to bring in its most successful year, Maureen was awarded a seat on the board of directors. Previously, Maureen was a Senior National Accounts Manager at Abbott Laboratories where she focused on contract compliance, increasing revenues, and sales. She initiated and innovated contract management and auditing procedures that resulted in a new nationwide cost center the produced annual savings of over \$1 million. She also helped cofound two holiday charities that continue today.

Maureen received two BAs from the University of Iowa., one in Journalism and one in Communication. Maureen also received a Master of Liberal Arts (ALM) in Management with a Concentration in Finance & Control from Harvard University.

Where: Microsoft NERD Center, 1 Memorial Drive, Cambridge, MA

Directions: <http://microsoftcambridge.com/About/Directions/tabid/89/Default.aspx>
For updates please monitor: www.boston-enet.org

Computer Society, GBC/ACM and BostonCHI - 7:00 PM, Thursday, 21 January

Beyond the UX Tipping Point

Jared M. Spool, Founding Principal, User Interface Engineering



For the longest time, making a great experience for the user was a luxury item in a business's strategy. It was a nice-to-have, after identifying a customer need and fulfilling it with a working product. The product had to work and it had to ship. If it was a great experience, well all the better. Times have changed.

The cost of creating and delivering a product is no longer a barrier to entry. Quality is no longer a differentiator.

What's left? The experience of using the product. If you're going to be truly competitive in today's markets, your products and services better have a great experience. To do that, a fundamental shift has to occur inside your organization. It's no longer acceptable to ship a product with a poor experience or to deliver poor customer service. Every part of the organization has to be infused with an understanding of great user experience. Your organization has to cross the UX Tipping Point.

Jared M. Spool is the founder of User Interface Engineering and a co-founder of Center Centre. If you've ever seen Jared speak about user experience design, you know that he's probably the most effective and knowledgeable communicator on the subject today. He's been working in the field of usability and experience design since 1978, before the term "usability" was ever associated with computers.

Jared spends his time working with the research teams at User Interface Engineering, helps clients understand how to solve their design problems, explains to reporters and industry analysts what the current state of design is all about, and is a top-rated speaker at more than 20 conferences every year. With Dr. Leslie Jensen-Inman, he is starting Center Centre, a new school in Chattanooga, TN to create the next generation of industry-ready UX Designers. In 2014, the school, under the nickname of

the Unicorn Institute, launched a Kickstarter project that successfully raised more than 600% of its initial goal. He is also the conference chair and keynote speaker at the annual UI Conference and UX Immersion Conference, and manages to squeeze in a fair amount of writing time. He is author of the book, *Web Usability: A Designer's Guide* and co-author of *Web Anatomy: Interaction Design Frameworks that Work*. You can find his writing at uie.com and follow his adventures on the twitters at [@jmspool](https://twitter.com/jmspool).

The meeting will be held in the new meeting auditorium at the Verizon Technology Center. The address is 60 Sylvan Road, Waltham, MA 02451. The entrance is by the far corner - with the picnic tables out front - and not the tower or the new building. It is most easily reached by the West Street entrance.

Networking and limited refreshments provided by BostonCHI at 6:30 Verizon Labs, Waltham, MA . Verizon requires us to provide a list of attendees in advance, so if you want to come, you need to register at <http://jaredspooljan2016.eventbrite.com>, but admission is free.

We will be taking Jared to dinner at Green Papaya after the talk at about 9pm.

Up-to-date information about this and other talks is available online at <http://ewh.ieee.org/r1/boston/computer/>. You can sign up to receive updated status information about this talk and informational emails about future talks at <http://mailman.mit.edu/mailman/listinfo/ieee-cs>, our self-administered mailing list.

For more information contact Peter Mager (p.mager@computer.org)

[Admission is free, but you must register at <http://jaredspooljan2016.eventbrite.com>]

To assist us in planning this meeting, please pre-register at

<http://www.ieeeboston.org/Register/>.

Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>

Consultants Network – 6:30PM, Wednesday, 27 January

Tax Information and Tax Pits for 2015 Reporting

Brad Capland

Brad is both a CPA and Registered Representative affiliated with Bay State Financial. His experience includes all areas of tax planning and tax preparation for individuals and small businesses, with an emphasis on closely held and family businesses.

- General Information
- Tax Reporting
- Tax Preparation
- Reporting Issues for Independent Consultants
- What to Look for in a CPA or Professional Tax Preparer
- What Not to Look For
- Tax Tips
- Tax Pitfalls

PLEASE NOTE: The meeting is open to the public. No charge for Consultants Network members or employees of Constant Contact; \$5 entrance fee for all others. Casual dress.

Registration

- (no registration required)

The Consultants Network meeting starts at 6:30 PM. The meeting will take place at Constant Contact, Reservoir Place - 1601 Trapelo Road, Waltham, MA 02451, Great Room on the first floor.

Driving Directions

Follow I-95/route 128 to Trapelo Rd in North Waltham, Waltham. Take exit 28 from I-95/route 128. (<https://goo.gl/maps/tvn3l>)

Consultants Network meetings generally take place on the fourth Wednesday of each month, but are not held during the summer months. Check the Consultants Network website for meeting details and last-minute information.

<http://www.boston-consult.com/calendar.php>

For more information, e-mail cn.boston@ieee.org or chairman@boston-consult.com; or contact the chairman Heinz Bachmann, at 978-637-2070. The Consultants Network website is at www.boston-consult.org.

Geoscience and Remote Sensing Society – 5:30PM, Thursday, 28 January

Using Satellite FTS-IR Measurements of Tracers to Quantify the Strength of the Mean Overturning Circulation of the Stratosphere

Marianna K. Linz, fourth year PhD student in the MIT-Woods Hole Oceanographic Institute Joint Program in Physical Oceanography.



The Brewer-Dobson circulation is the overturning circulation of the stratosphere and was originally inferred from observations of ozone and water vapor. It is critical for the stratospheric ozone distribution and for troposphere-stratosphere coupling. The consensus from climate models is that the Brewer-Dobson circulation will

intensify under global warming scenarios.

Although the general structure of the circulation can be qualitatively assessed from ozone and water vapor, the quantitative strength of the circulation has been much more difficult to measure. Certain trace gases, SF₆ and CO₂, can be used to estimate the “age” of air, or how long on average air has been in the stratosphere since upwelling through the tropi-

Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>

cal tropopause. I will present a new time-dependent theory for quantitatively assessing the magnitude of the stratospheric circulation using this theoretical age.

The speaker will show results from an idealized atmospheric model with a seasonal cycle, which reveal the required spatial and temporal sampling necessary to observe the circulation. Then she will use measurements from the ACE and MIPAS FTS-IR limb sounders in this theoretical framework to determine the magnitude and variability of the circulation of the stratosphere. Between 2007 and 2011, while there was little change in the strength of the circulation in the lowermost stratosphere, the upper stratosphere exhibited changes in SF6 concentrations consistent with a 20% weakening of the strength of the overturning circulation.

Marianna Linz is a fourth year PhD student in the

MIT-Woods Hole Oceanographic Institute Joint Program in Physical Oceanography, where she studies the stratospheric circulation with her advisor Alan Plumb. She completed her bachelors in Chemistry and Physics and Earth and Planetary Sciences at Harvard University in 2011. She is currently a National Defense Science and Engineering Graduate Fellow. She is interested in climate dynamics, and has previously worked on ocean eddies, large-scale ocean heat transport, and the representation of El Nino in climate models.

Meeting Location: MIT Lincoln laboratory - Forbes Road Cafeteria - 3 Forbes Road Lexington, MA 02421.

To assist us in planning this meeting, please pre-register at <http://www.ieeeboston.org/Register/>.

IEEE Boston Section Social Media Links:

Twitter: <https://twitter.com/ieeeboston>

Facebook: <https://www.facebook.com/IEEEBoston>

YouTube: <https://www.youtube.com/user/IEEEBostonSection>

Google+: <https://plus.google.com/107894868975229024384/>

LinkedIn: <https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about>

Introduction to Embedded Linux

Time & Date: 6 - 9PM; Mondays, March, 7, 14, 21, 28

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Overview - This 4 day course introduces the Linux Operating System and Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part of the course covers testing, booting and configuring of Embedded Linux systems including embedded cross-development and target board considerations.

Who Should Attend – The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives

- To provide a basic understanding of the Linux OS and the Eclipse IDE framework.
 - To understand the complexities of Embedded Linux Distributions in embedded systems.
 - To learn how to configure, boot and test Embedded Linux distributions and applications running on Embedded Linux target systems.
 - To give students the confidence to apply these concepts to their next Embedded Linux project
- Hardware and Software Requirements** – The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ installation or

prior knowledge of C-based Makefiles is useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials

- Linux Kernel Development by Robert Love
- Linux System Programming by Robert Love
- Embedded Linux Primer by Christopher Hallinan
- Pro Linux Embedded Systems by Gene Sally
- Embedded Linux Development Using Eclipse by Doug Abbott
- Linux Device Drivers by Jonathan Corbet et al
- Essential Linux Device Drivers by Sreekrishnan Venkateswaran

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at LynuxWorks, Tiler, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based development tools, training and consulting for the embedded systems market.

OUTLINE

Course Schedule Day 1

The Basics
Linux Terminology, History and Versioning
The Linux Community: Desktop & Embedded Linux and the GPL
Linux References (Books and Online)
Getting Started

Building the Kernel Source Code
 Embedded Linux Kernels
 Linux 2.6 and 3.x
 Basic Kernel Capabilities
 Process and Threads Management
 Signals and System Calls
 Synchronization, IPC and Error Handling
 Timing and Timers
 Memory Management and Paging
 The I/O Subsystem: A Tale of Two Models
 Modularization
 Debugging
 Process-Level and System-Level Debug
 GDB, GDB Server and the GDB Server Debugger
 Other Debug and Test Tools
 An Eclipse Remote Debug Example
 Advanced Debug with printk, syslogd and LTTng
 System-Level Debug
 System-Level Debug Tools
 The /proc Filesystem
 Advanced Logging Methods
 KGDB and KDB
 Crash and Core Dumps

Course Schedule Day 2

Process & Threads Management
 What are Processes and Threads?
 Virtual Memory Mapping
 Creating and Managing Processes and Threads
 Thread-Specific Data (TSD)
 POSIX
 The Native POSIX Threading Library (NPTL)
 Kernel Threads
 Signals
 System Calls
 Scheduling
 Linux 2.4 and 2.6 Scheduling Models
 The O(1) Scheduler
 The Completely Fair Scheduler (CFS)
 Synchronization
 Via Global Data
 Via Semaphores, Files and Signals
 Condition and Completion Variables
 Mutexes and Futexes
 Inter-Process Communications (IPC)

Message Queues
 Semaphores Revisited
 Shared Memory
 Pipes and FIFOs
 Remote Procedure Calls
 Networking

Course Schedule Day 3

Memory Management and Paging
 Demand Paging and Virtual Memory
 Allocating User and Kernel Memory
 Mapping Device Memory
 The Slab Allocator
 The OOM Killer
 Memory in Embedded Systems
 Advanced Memory Operations
 Linux and Memory
 Managing Aligned Memory
 Anonymous Memory Mappings
 Debugging Memory Allocations
 Locking and Reserving Memory
 Error Handling
 errno and perror
 strerror and strerror_r
 oops, panics and Segmentation Faults
 Timing
 How Linux Tells Time
 Kernel, POSIX and Interval Timers
 High-Resolution Timers (HRTs)
 Modularization
 Creating a Module and Module Loading
 Dependency Issues
 In Embedded Systems
 Shared Libraries
 A Shared Library Example
 Static and Dynamic Libraries
 The I/O Subsystem: A Tale of Two Models
 The Original Device Driver Model
 The Standard I/O Interface
 Major and Minor Numbers
 Configuring the Device Driver
 The Evolution of the New Device Driver Model
 The Initial Object-Oriented Approach
 Platform Devices, Busses, Adapters and Drivers
 Comparing the Two Driver Models

Course Schedule Day 4

Advanced I/O Operations
 Standard I/O Operations
 Scatter-Gather and Asynchronous I/O
 Poll, Select and Epoll
 Memory-Mapped I/O
 File Advice
 I/O Schedulers
 Interrupt and Exception Handling
 Bottom Halves and Deferring Work
 The Linux Boot Process
 The Root Filesystem
 Desktop Linux Boot
 Bootloaders and U-Boot
 Embedded Linux Boot Methods
 Building and Booting from SD Cards
 Managing Embedded Linux Builds
 Configuring and menuconfig
 Building Custom Linux Images
 Target Image Builders

LTIB and Yocto
 System Architecture Design Approaches
 Deploying Embedded Linux
 Choosing and Building the Root Filesystem
 Useful Embedded Filesystems
 Module Decisions
 Final IT Work
 Embedded Linux Trends
 Some Final Recommendations

**Decision (Run/Cancel) Date for this Courses is
 Friday, February 26, 2016**

Payment received by Feb. 23

Members	\$400
Non-members	\$430

Payment received after Feb. 23

IEEE Members	\$430
Non-members	\$455

To Register, <http://ieeeboston.org/event/introduction-embedded-linux-spring-2016>

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups. If you have an expertise that you feel might be of interest to our members, please

submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is <http://ieeeboston.org/course-proposals/> . Alternatively, you may contact the IEEE Boston Section office at sec.boston@ieee.org or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>



CALL FOR PAPERS Dates Extended
2016 IEEE International Symposium on
Phased Array Systems and Technology
Revolutionary Developments in Phased Arrays



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18–21 October 2016

Westin Waltham Hotel, Greater Boston, Massachusetts, USA

www.array2016.org

About the Symposium

Phased array systems continue to be a rapidly evolving technology with steady advances motivated by the challenges presented to modern military and commercial applications. This symposium will present the most recent advances in phased array technology and present a unique opportunity for members of the international community to interact with colleagues in the field of Phased Array Systems and Technology.

Suggested Topics:

- System Architecture
- Aperture Design
- Antenna Elements
- Beamforming Techniques
- T/R Modules
- Signal Processing for Arrays
- Array Measurements
- Advanced Materials
- Packaging and Manufacturing
- Applied Computational Electromagnetics



Special Sessions

Please provide suggestions for special sessions to the Technical Program Chair at info@array2016.org

Paper Template and Submission Procedures

Template and submission procedures are available at www.array2016.org/forauthors.htm

Publication Information

All accepted papers will be published on the conference CD-ROM and distributed to conference attendees. Selected papers meeting the publishing requirements will be published in IEEE Xplore as part of the IEEE Conference Publication Program.

Important Dates:

Summary (~1000 words + figures).....	01 Feb 2016
Notification of Acceptance	15 Mar 2016
Final Papers (8 page max).....	01 Jul 2016

Conference Committee

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Hans Steyskal, Arcon
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CALL FOR PAPERS



2016 IEEE High Performance Extreme Computing Conference (HPEC '16)

Twentieth Annual HPEC Conference

13 - 15 September 2016
Westin Hotel, Waltham, MA USA



www.ieee-hpec.org

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The IEEE High Performance Extreme Computing Conference (HPEC '16) will be held in the Greater Boston Area, Massachusetts, USA on 13 – 15 September 2016. The HPEC charter is to be the premier conference in the world on the confluence of HPC and Embedded Computing.

The technical committee seeks new presentations that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- Advanced Multicore Software Technologies
- Case Studies and Benchmarking of Applications
- Automated Design Tools
- Mapping and Scheduling of Parallel and Real-Time Applications
- Computing Technologies for Challenging Form Factors
- ASIC and FPGA Advances
- Open System Architectures
- Data Intensive Computing
- Big Data and Distributed Computing
- Interactive and Real-Time Supercomputing
- Graph Analytics and Network Science
- Fault-Tolerant Computing
- Embedded Cloud Computing
- Digital Front Ends
- General Purpose GPU Computing
- Advanced Processor Architectures
- Secure Computing & Anti-Tamper Technologies
- New Application Frontiers

HPEC accepts two types of submissions:

1. Full papers (up to 6 pages, references not included), and
2. Extended abstracts (up to 2 pages, references included).

Preference will be given to papers with strong, quantitative results, demonstrating novel approaches or describing high quality prototypes. Authors of full papers can mark their preference for a poster display or an oral presentation. Presenters who wish to have hardware demonstrations are encouraged to mark their preference for a poster display. Accepted extended abstracts will be displayed as posters.

All paper and extended abstract submissions need to use the approved IEEE templates. Full paper submissions with the highest peer review ratings will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions and extended abstracts are published on ieee-hpec.org. Vendors are encouraged to sign up for vendor booths. This will allow vendors to present their HPEC technologies in an interactive atmosphere suitable for product demonstration and promotion.

We welcome input (hpec@ieee-hpec.org) on tutorials, invited talks, special sessions, peer reviewed presentations, and vendor demos. Instructions for submitting will be posted on the conference web site shortly.

Call for Papers, Posters, and Tutorials

2016 IEEE International Symposium on Technologies for Homeland Security

10 – 12 May Westin Hotel, Waltham, MA
<http://ieee-hst.org/>



Co-sponsors:



Call for Papers, Posters & Tutorials

The 15th annual IEEE Symposium on Technologies for Homeland Security (HST '16), will be held 10 – 12 May, in the Greater Boston, Massachusetts area. This symposium brings together innovators from leading academic, industry, business, Homeland Security Centers of Excellence, and government programs to provide a forum to discuss ideas, concepts, and experimental results.

Produced by IEEE with technical support from DHS S&T, IEEE, IEEE Boston Section, and IEEE-USA and organizational support from MIT Lincoln Laboratory, Raytheon, Battelle, and MITRE, this year's event will once again showcase selected technical paper and posters highlighting emerging technologies in the areas of:

Cyber Security

Biometrics & Forensics

Land and Maritime Border Security

Attack and Disaster Preparation, Recovery and Response

We are currently seeking technical paper, poster and tutorial session submissions in each of the areas noted above. Submissions should focus on technologies with applications available for implementation within about five years. All areas will cover the following common topics:

- Strategy and threat characterization, CONOPs, risk analysis,
- Modeling, simulation, experimentation, and exercises & training, and
- Testbeds, standards, performance and evaluations.

Contact Information

For more detailed information on the Call for Papers, Posters & Tutorials, as well as Sponsorship and Exhibit Opportunities, visit the website: <http://ieee-hst.org/> or email: information@ieee-hst.org. Submissions should be made at the following website: <https://cmt.research.microsoft.com/HST2016/>

Important Dates

Paper Abstract Deadline: (final deadline)	January 4, 2016
Paper, Poster and Tutorial Acceptance Notification	February 15, 2016
Final Paper Submission Deadline:	April 1, 2016

All deadlines are by midnight Eastern Time.

Organizing Committee

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<i>Cyber Security</i>
David Balenson, SRI International
Emily Frye, MITRE

Introduction to Embedded Android

Date & Time: Mondays, January 4, 11, 18, 25, 2016, 6 - 9PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Last Notice Before the Course Begins, Register Now!!!

Course Summary - This course introduces the student to the use of Android in Embedded Systems and the use of Embedded Android Distributions. The first part of the course focuses on acquiring an understanding of basic Android concepts and on how Android is hosted by the Linux Operating System, highlighting areas of concern for Embedded Android systems development such as overall system design, boot performance and customization. The latter part of the course covers the differences between the standard Android Open Source Project and Embedded Android distributions.

Who Should Attend - The course is designed for real-time engineers who are building Embedded Android solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Android. This course will clearly demonstrate both the strengths and weaknesses of the use of Android in Embedded Systems.

Course Objectives

- To provide a basic understanding of Android and its use in Embedded Systems
- To gain an understanding of the complexities of Embedded Android Distributions
- To learn how to configure, build, boot and deploy Embedded Android solutions
- To understand the differences between the AOSP and Embedded Android build approaches
- To give students confidence to apply these concepts to their next Embedded Android project

OUTLINE

Course Schedule Day 1

The Basics
 What Android Is and What It Is Not
 Android Terminology, History and Versioning
 The Android Community: Phones, Tablets and Embedded Systems
 Android, the GPL and the Apache Harmony Project
 Android and Linux References (Books and Online)
 Getting Started
 The Android Open Source Project

Android Hardware Requirements
 Embedded Linux Usage in Android
 Java Usage in Android
 The Android API
 The Dalvik Virtual Machine (VM)
 The Android Runtime and Zygote
 The Java Native Interface (JNI)
 Binder and System Services
 Key Android Libraries

Debugging in Android
 Process-Level and System-Level Debug
 ADB, DDMS and Monkey
 GDB and KGDB
 GDB Server and Remote Debugging
 An ADB Example

Course Schedule Day 2

Applications Development Overview
 Eclipse-Based Application Development
 The .apk File
 The Android Emulator
 Linux Modifications to Support Android
 Wakelocks
 Low-Memory Killer
 Binder
 Anonymous Shared Memory (ashmem)
 Alarm
 Logger
 More Androidisms
 Android Internals
 Hardware Support
 Native User Space
 More on Dalvik and Java in Android
 System Services and Binder
 Useful AOSP Packages
 System Startup Overview

The AOSP
 The Android Development Host
 AOSP Basics
 Building and Running Android
 ADB and the Emulator

Course Schedule Day 3

The AOSP Build System
 Comparison with Other Builders
 Configuration and Functions
 The envsetup.sh File
 Make Recipes
 Cleaning
 Modules in Android

Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>

The Default Build
 Basic Build Recipes
 AOSP Build Recipes
 The Build Commands
 Building the Software Development Kit (SDK)
 Building the Compliance Test Suite (CTS)
 Building the Native Development Kit (NDK)
 API Updates
 Building a Single Module
 Building Out-of-Tree and In-Tree
 Linaro
 The Linaro Organization
 Key Members and Participants
 The Linaro Mission Objective
 The Linaro Android Distribution Approach
 Getting the Latest Linaro Distribution
 The Linaro Distribution and Desktop Requirements
 The Linaro Repository
 The Linaro Maintainer Tools
 The Linaro Image Tools
 The Linaro Distribution for the i.MX53
 Top Level Hierarchy
 The GCC Tools for Linaro
 The abi, android-toolchain-eabi and bionic Directories
 The bootable and build Directories
 The cts, dalvik and development Directories
 The device Directory
 The docs and external Directories
 The frameworks and hardware Directories
 The kernel Directory
 The libcore and linaro-kernel-config Directories
 The ndk, packages and prebuilt Directories
 The sdk Directory
 The system Directory
 U-Boot in Linaro
 The Linaro Build Process
 The Linaro SD Creation Process
 The Linaro Tarballs

Course Schedule Day 4

Native User Space
 The Android Filesystem
 The Android Root Directory
 The system and data Directories
 Building the Linux and Android Filesystems
 SD Card Layout
 The Android Init Process
 Operation and Configuration
 Global Properties and ueventd
 The Boot Logo
 The Android Command Line
 The Shell
 Toolbox
 Native Utilities and Daemons
 Framework Utilities and Daemons
 Adding Capabilities to the Android Filesystem

The Linux Console Shell
 The bash and ash Shells
 Busybox
 Linux Daemons Used by Android
 Adding Capabilities to the Linux Filesystem
 The Android Framework
 Framework Startup
 Core Building Blocks
 System Services and Binder
 Boot Animation
 Dex Optimizations
 Application Startup
 Utilities and Commands
 Support Daemons
 The Hardware Abstraction Layer (HAL)
 Advanced Android Customizations
 Adding New Hardware Support
 Customizing the Default Packages
 More Init Customizations
 Embedded Android Trends
 Moving to a Generic User Interface
 Easier Development for Non-Phones
 Debugging Embedded Android
 Better Documentation and Training
 Some Final Recommendations

Lecturer Bio – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 25-year electronics veteran, he has held various positions at LynuxWorks, Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based development tools, training and consulting for the embedded systems market.

**Decision (Run/Cancel) Date for this Courses is
 Monday, December 28, 2015**

Payment received by Dec. 21

IEEE Members	\$390
Non-members	\$420

Payment received after Dec. 21

IEEE Members	\$420
Non-members	\$440

To Register, <http://ieeeboston.org/event/introduction-to-embedded-android-fall-2015/>

Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>

Advanced Embedded Linux Optimization

Time & Date: 6 - 9PM, Mondays, April 4, 11, 18, 25

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand methods for debugging, profiling and testing Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.
- To give students the confidence to apply these concepts to their next Embedded Linux project.

OUTLINE

Course Schedule Day 1

Getting Started with Embedded Linux
Linux and the GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs

Linux References (Books and Online)

Basic Debugging Review
Embedded Applications Debugging
GDB, GDB Server and the GDB Server Debugger
An Eclipse Remote Debug Example
Debugging with printk and LTTng
System Logs
Other Debuggers
System-Level Debug
System-Level Debug Tools
The /proc and /sys Filesystems
Basic Logging
KGDB and KDB
Crash Dumps and Post-Mortem Debugging
Debugging Embedded Linux Systems
Backend Debuggers
JTAG and In-Circuit Emulators
Hardware Simulators
Analyzers
Debugging Device Drivers
Kernel Probes
Kexec and Kdump
Kernel Profiling

Course Schedule Day 2

Testing
Design for Test
Agile Software Design
Unit-Level Testing
System-Level Testing
Code Coverage Tools
gcov
Automated Testing
DebugFS
Configuring DebugFS
DebugFS Capabilities
Advanced Logging
LogFS
Using Logwatch and Swatch
Using syslog and syslog-ng

- Kernel Hacking
- Configuring Kernel Hacking
- Kernel Hacking Capabilities
- Tracing
- ptrace and strace
- New Tracing Methods
- SystemTap
- Ftrace, Tracepoints and Event Tracing
- Tracehooks and utrace

Course Schedule Day 3

- Profiling
- Basic Profiling
- gprof and Oprofile
- Performance Counters
- LTTng
- Another DDD Example
- Manual Profiling
- Instrumenting Code
- Output Profiling
- Timestamping
- Measuring Embedded Linux Performance
- Some Ideas on Performance Measurement
- Common Considerations
- Uncommon Considerations
- Using JTAG Methods
- BootLoader Optimizations
- Boot Time Measurements
- Effective Memory and Flash Usage
- Filesystem Choices
- Addressing Performance Problems
- Types of Performance Problems
- Using Performance Tools to Find Areas for Improvement
- Application and System Optimization
- Device Driver Optimization
- CPU Usage Optimization
- Memory Usage Optimization
- Disk I/O and Filesystem Usage Optimization
- The Perf Tool
- Improving Boot Performance
- Boot Time Optimization
- The Linux Fastboot Capability
- Building a Smaller Linux
- Building a Smaller Application
- Filesystem Tips and Tricks
- Some Notes on Library Usage
- Performance Tool Assistance
- Recording Commands and Performance
- System Error Messages and Event Logging
- Dynamic Probes
- User Mode Linux and Virtualization

Course Schedule Day 4

- Improving CPU Performance
- Run Queue Statistics
- Context Switches and Interrupts
- CPU Utilization
- Linux Performance Tools for CPU
- Process-Specific CPU Performance Tools
- Stupid Cache Tricks
- Improving System Memory Performance
- Memory Performance Statistics
- Linux Performance Tools for Memory
- Process-Specific Memory Performance Tools
- More Stupid Cache Tricks
- Improving I/O and Device Driver Performance
- Disk, Flash and General File I/O
- Improving Overall Performance Using the Compiler
- Basic Compiler Optimizations
- Architecture-Dependent and Independent Optimization
- Code Modification Optimizations
- Feedback Based Optimization
- Application Resource Optimization
- The Hazard of Trust
- An Iterative Process for Optimization
- Improving Development Efficiency
- The Future of Linux Performance Tools
- Some Final Recommendations

Lecturer Bio – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 25-year electronics veteran, he has held various positions at LynuxWorks, Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratix Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based development tools, training and consulting for the embedded systems market.

**Decision (Run/Cancel) Date for this Courses is
Friday, March 26, 2016**

Payment received by March 23

IEEE Members	\$395
Non-members	\$435

Payment received after March 23

IEEE Members	\$435
Non-members	\$470

To Register, <http://ieeeboston.org/event/advanced-embedded-linux-optimization-spring-2016>

Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>

Flexible Electronics - Packaging Design, and Materials Analysis for Aerospace, Military, Medical & High end Consumer Products

Time & Date: 8AM - 5PM; Thursday, March 31, 2016

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Tina Barclay, , Chief Technical Officer, TAS Consulting

Prerequisites:

Assume Student can read schematics, understand component usages and has some basic thermal analysis capability.

Class Summary:

This is a one-day session focusing on the advanced packaging needed for a flexible board design. This course will not cover schematic layout and circuit design. It will cover what you do with the completed schematic. It will address layout issues to avoid and what components work best in a flexible design. It will show what methods are available and almost available to package the flexible circuit board.

What materials work best for which industry?

What analysis should be performed to assure the design will work in the intended environment?

Who should attend?

This course is designed for Engineers involved in the above design elements of a project. This course will demonstrate the work needed to review the materials and environment for designs using flexible circuits.

Course Objectives:

- Understand circuit board layout changes for flexible electronics
- Show how to remove Heat in a flexible board.

- Review, Show, Typical Analysis needed for Reliability concerns
- Review electronics Packaging Issues and How to handle them
- Introduce Solder Fatigue concepts and what to do about it
- Review different Industry needs and show the key indicators for each.

Course Schedule:

1. Review student backgrounds and industries – course will be pushed toward the industries represented. (1/2 hr.)
2. Basic background on flexible boards (1/2 hr.)
3. Review schematic layouts – what works and what doesn't – this will be industry specific. (1/2 hr.)
4. Review analysis needed: structural, thermal, reliability, solder fatigue (1 hr.)
5. Walk through analysis for each of the above. (1 hr.)
6. Show issues of each of the analysis types, work-arounds, show stoppers, and realistic answers to some industry concerns. (1 ½ hr.)
7. Review solder fatigue differences for different solders. (1/2 hr.)
8. Review any additional industry needs specific to student's industries and questions. (1 hr.)
9. Lab Time- Students to work on project – can bring one or work on one provided. (1 ½ hr.)

Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>

Instructor:

Tina Barclay has over 30 years of experience in electronic packaging, testing, and analysis (BS Engineering – Thermal and Materials and MS – Systems Engineering and program management. Tina worked for aerospace companies (ITT, TRW, Perkin Elmer, Goodrich and Aerojet), NASA (Marshall Space Flight Center), automotive (both Ford and Chrysler), military black boxes (Singer Librascope, Army, Navy and Air Force modules) as well as high end medical and commercial (Spectracom, MKS, Kodak, etc.). She has run and created testing labs, procedures, designs, fixes for designs, and the first BGA used in high temperature environments. Tina has R&D experience, proposal experiences, and program management experience in all the above industries. She has 21 US patents — all in electronics packaging, materials, and thermal. . Her experience has included all levels of

parts reliability for systems ranging from 6-month to 10-year reliabilities. She is a frequent speaker at industry-specific conferences like IMAPS (International Microelectronics and Packaging Society) and ASE (Automotive Society of Engineers) and is on the IPC (IPC - Association Connecting Electronics Industries) Specification Review Panel.

**Decision (Run/Cancel) Date for this Courses is
Wednesday, March 16, 2016**

Payment received by March 14

IEEE Members	\$235
Non-members	\$260

Payment received after March 14

IEEE Members	\$260
Non-members	\$285

To Register, <http://ieeeboston.org/event/flexible-electronics-spring-2016>

Phased - Array and Adaptive-Array Fundamentals and their Recent Advances

Time & Date: 6 - 9PM; Mondays, March 14, 21, 28, April, 4, 25, May 9, 16, 23, June 6, 13

Location: MITRE Corporation, 202 Burlington Road, Bedford, MA (tentative)

Speaker: Dr. Eli Brookner, Raytheon Company (Retired)

**PRACTICAL
PHASED ARRAY
ANTENNA SYSTEMS**



ELI BROOKNER

All Attendees of the class will receive a trial license of MATLAB and Phased Array System Toolbox from MathWorks in addition to a set of examples which help demonstrate the key radar concepts covered in the course material.

Text: “Practical Phased Array Antenna Systems”, Dr. Eli Brookner, Editor, Artech House, 1991 Hardcover, 258 pages, List Price \$179, Hardcover, 258 pages. Covers array fundamentals: phase and time-delay steering; grating lobes for 1- and 2-dimensional arrays; effects of errors and failures on gain, sidelobes and angle accuracy; array weighting, thinning, blindness, mutual coupling, elements, phase-shifters and feeds; limited field of view (LFOV) arrays; SPY-1; example design.

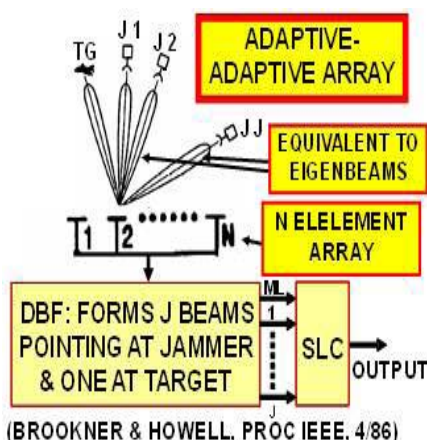
Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>

This course is based on the book entitled Practical Phased Array Antenna Systems by Dr. Eli Brookner. The book covers array basics and fundamentals which do not change with time. The course, the book and the notes will provide an ideal introduction to the principles of phased array antenna design and adaptive arrays. The course material and notes cover in addition recent developments in phased arrays updated to 2016.

With the explicitly tutorial approach the course and book offers a concise, introductory-level survey of the fundamentals without dwelling on extensive mathematical derivations or abstruse theory. Instead a physical feel will be given. The book provides extensive curves, tables and illustrative examples.

Covered in easy terms will be sidelobe cancellation, full adaptive array processing without suffering its computation complexity (through the use of adaptive-adaptive array processing also called beam-space processing and eigenbeam processing). Finally, Space-Time Adaptive Array (STAP) for airborne platforms will be explained and related to the displaced phase center antenna (DPCA).

This course is intended for the engineer or scientist not familiar with phased-array antennas as well as the antenna specialist who wants to learn about other aspects of phased-array antenna systems. The major emphasis will be on the system aspects of phased-array systems.



Lecture #1. Monday March 14; Phased Array Fundamentals: Fundamental Principles of Electronically Scanned Array (ESA) explained with tube COBRA DANE used as example. Covered will be: Near and Far Field Definitions, Phased Steering, Switched-Line Phase Steering; Time Delay Steering, Subarraying, Array Weight-

ing, Monopulse, Duplexing, Array Thinning, Embedded Element, dual polarized circular waveguide element, advantage of triangular lattice over square lattice, Tour of COBRA DANE (6 stories high) via color slides.

PATRIOT UPGRADES

- 2012: \$400 M UPGRADE MADE IT 2012 STATE-OF-THE-ART; US ARMY FIELDING TO 2048*
- 2015: GaN AESA; 360° COV.**

- >200 BUILT
- 13 NATIONS
- 5000 EL PER/FACE
- C-BAND

(*FEB. 19, 2015/PRNEWSWIR1520E; **MICROWAVE&RF, AUG 2015, P. 24)



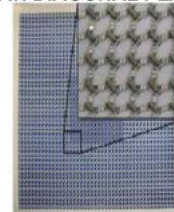
PHOTO COURTESY RAYTHEON

Lecture #2. Monday March 21; Linear Array Fundamentals: Conditions for no grating lobes; beamwidth vs scan angle; sine space; Array Factor; sidelobe level vs antenna beamwidth; directivity; antenna efficiency

factors; array weightings; array frequency scanning; array bandwidth.

TIGHTLY COUPLED DIPOLE ARRAY (TCDA)

- BANDWIDTH: 1:20
- THICKNESS: $\lambda/40$ AT LOWEST FREQ.
- DUAL POLARIZATION
- COLOCATED PHASE CENTERS
- GOOD POLARIZATION IN DIAGONAL PLANE
- WAIM STRUCTURE



(RAYTHEON TECHNOLOGY TODAY, 2014, ISSUE 1)

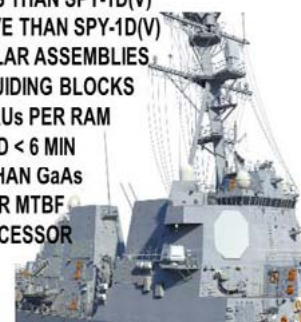
Lecture #3. Monday March 28; Planar Arrays: Array Factor; array separability; sine-space ($\sin\alpha\text{-}\sin\beta$ space, T-space); grating lobes location for triangular and rectangular lattice; directivity; very useful bell curve approximation; array

thinning system issues.

AIR & MISSILE DEFENSE RADAR (AMDR)

- S-BAND: AIR & MISSILE DEFENSE
- X-BAND: HORIZON SEARCH
- ADAPTIVE DIGITAL BEAM FORMING
- 30X > TARGETS THAN SPY-1D(V)
- 30X > SENSITIVE THAN SPY-1D(V)
- RADAR MODULAR ASSEMBLIES (RAMs) ARE BUILDING BLOCKS
- 4 TYPES OF LRUs PER RAM
- LRU REPLACED < 6 MIN
- GaN 34% < \$ THAN GaAs
- GaN HAS 10⁸ HR MTBF
- COTS x86 PROCESSOR
- SCALABLE

PICTURE COURTESY RAYTHEON



Lecture #4. Monday April 4; Array Errors: Effects of element phase and amplitude element errors and element failures; simple physical derivation of error effects; paired echo theory; subarray errors; quantization errors; examples.

Lecture #5. Monday April 25; Radiating Elements: Waveguide; dipole; slotted waveguide; microstrip patch; stacked patch; notch (wideband); spiral; matching (wide-angle); waveguide simulator; practical limitations, mutual coupling and array blindness; scattering matrix; design procedure; polarization mismatch loss.

Lecture #6. Monday May 9; Active Phased Arrays: 2nd generation solid state hybrid active electronically scanned array (AESAs) covered using PAVE PAWS as example, T/R Module Introduced, Cross Bent Dipole Element, Mutual Coupling, Array Blindness, Tour of PAVE PAWS (6 stories) via color slides. 3rd Generation AESAs: THAAD, SPY-3, IRIDIUM, F-15 APQ-63(V)2, APG-79, XBR, AMDR and upgraded Patriot GaAs and GaN microwave integrated circuits (Monolithic Microwave Integrated Circuit, MMIC).

CJR TEAM CELEBRATE A
SUCCESSFUL FIRST LIVE-LAUNCH



PHOTO COURTESY RAYTHEON

Lecture #7. Monday May 16; Array Feeds: Corporate and space fed; Reactive (lossless) and matched (Wilkinson); even/odd mode analysis. Serial; Ladder; Lopez; Blass; Radial, Butler matrix; microstrip/stripline;

Rotman Lens; SLQ-32; PATRIOT space-fed array; reflectarray. System Considerations: sequential detection, beam shape loss; receiver and A/D dynamic range; polarization mismatch loss; array noise figure and system temperature taking into account array mismatch. Phase Shifters: Diode switched-line, hybrid-coupled, loaded-line; ferrite phase-shifters: non-reciprocal latching; diode vs ferrite; MEMS (Micro-Electro-Mechanical Systems) and its potential for a low cost ESA.

Lecture #8. Monday May 23; Limited Scan (Limited Field of View [LFOV]) Arrays: Explained using simple high school optics for TPS-25, 1st Electronically Scanned Array (ESA) put in production. Fundamental Theorem specifying minimum number of

phase shifters needed for a specified scan angle. Method for realizing this minimum using overlapped array antenna elements as with HIPSAT lens array system and Microwave Landing System (MLS); reflector; randomized oversized elements; use of sum and difference patterns; use of spatial filters to reduce grating lobes and sidelobes. Hemispherical Coverage Dome Antenna.

X-BAND 25K ELEMENT AESA AN/TPY-2



8 DELIVERED, 3 MORE ON ORDER.

PHOTO COURTESY RAYTHEON

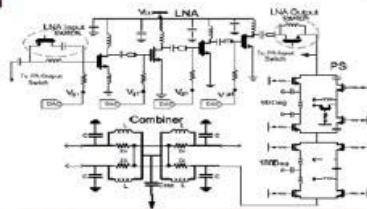
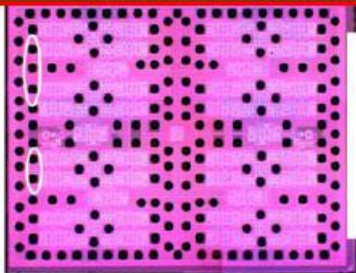
Lecture #9. Monday June 6; Phased Array Amazing Advances and Breakthroughs -- Part 1: Systems: Patriot now has GaN active electronically scanned array (AESA) providing 360° coverage, now a 2015 state-of-the-art AESA

radar system; S/X-band AMDR provides 30 times the sensitivity and number of tracks as SPY-1D(V); JLENS aerostat radar system now deployed over Washington DC; 3, 4, 6 faced "Aegis" radar systems developed by China, Japan, Australia, Netherlands, USA; Low Cost, Low Power Extreme MMIC (Moore's law at Microwave and mm-waves): 4 T/R modules on single chip at X-band costing ~\$10 per T/R module; Intel single chip 32-Element 60 GHz Tx/Rx Phased Array, full phased array on wafer at 110 GHz; on-chip built-in-self-test (BIST), will be used in the internet-of-things and in cell phones which by 2020 is expected to number 50 billion, expect such single chip arrays to cost only few dollars in future; All the RF circuitry for mm-wave automobile radars at 25 GHz and 77 GHz are being put on a chip with some believing that such arrays and radars will soon be produced for just a few dollars; Valeo Raytheon (now Valeo Radar) developed low cost, \$100s, car 25 GHz 7 beam phased array radar; about 2 million sold already, more than all the radars ever built up to a very few years ago. Digital Beam Forming (DBF): Israel, Thales and Australia AESAs have under development array with an A/D for every element channel; Raytheon develop-

ing mixer-less direct RF A/D having >400 MHz instantaneous bandwidth, reconfigurable between S and X-band; Radio Astronomers looking at using arrays with DBF. Materials: GaN can now put 5X to 10X the power of GaAs in same footprint, 38% less costly, 100 million hr MTBF, Raytheon invested \$150 million to develop GaN; SiGe for backend, GaN for front end of T/R module. MIMO (Multiple Input Multiple Output): Where it makes sense; contrary to what is claimed MIMO array radars do not provide 1, 2 or 3 orders of magnitude better resolution and accuracy than conventional array radars; MIMO does not provide better barrage-noise-jammer, repeater-jammer or hot-clutter rejection than conventional array radars; contrary to claims MIMO

tion. Methods for calculating this optimum weight are given using the Sample Matrix Inversion (SMI) algorithm, the Applebaum-Howells adaptive feed-back loop method, a recursive method, and Gram-Schmidt, Givens and Householder orthonormal transformations developed for the tracking problem and for the MSLC. The use of eigenvector beams and a whitening filter will also be developed. It will be shown how the latter reduces the transient response. Methods for obtaining the benefits of a fully adaptive array without its high computation and large transient time disadvantages are given. These are the adaptive-adaptive array processing procedures, the use of eigenbeam space, and the method of finding the largest eigenvalues and in turn their eigenbeams. The STAP algorithm will be introduced.

INTEL 32-ELEMENT SINGLE CHIP 60 GHZ TX/RX PHASED ARRAY



EXTREME MMIC

- Based on work with UCSD (we helped them a lot)
- Flip-chip packaging – CMOS from TSMC.
- Does not contain baseband circuitry for Gbps communications

PROF. GABRIEL M. REBEIZ
IEEE Phased Array Symposium Short Course, October 2013 – © UCSD and IEEE

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should not provide better minimum detectable velocity for airborne radars.

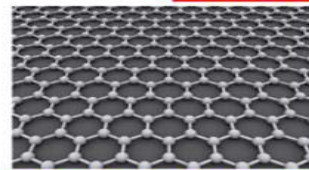
Sidelobe Cancellers (SLC): The simple single-loop, feed-forward canceller is introduced in easy terms. This is followed by a discussion of the simple single-loop feedback canceller with and without hard limiting. The normalized feedback SLC will also be covered. Presented will be their performance; transient response and cancellation ratio. Next the multiple-loop SLC (MSLC) will be covered. Applied to the MSLC will be the Gram-Schmidt, Givens and Householder orthonormal transformation methods. Systolic array implementations will be given.

Lecture #10. Monday June 13; Fully Adaptive Arrays: The optimum weight for a fully adaptive array is developed using a very simple deriva-

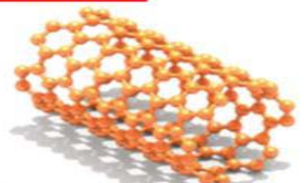
Phased Array Amazing Advances and Breakthroughs -- Part 2: Metamaterials: Material custom made (not found in nature): using 20 and 30 GHz metamaterial electronically steered antennas about the size of a laptop developed for transmission to satellites and back was demonstrated December 2013, goal is \$1K per antenna, remains to prove low cost and reliability, how this antenna works explained for first time; 2-20GHz stealthing by absorption simulated using <1 mm coating; target made invisible over 50% bandwidth at L-band; Focus 6X beyond diffraction limit at 0.38 μm ; 40X

GRAPHENE & CARBON (C) NANOTUBES (CNT): HOPE FOR MOORE'S LAW CONTINUATION

THZ CLOCK SPEED



GRAPHENE: 1 ATOM THICK C CRYSTAL; STRONGEST MATERIAL



CNT: MANUFACTURE ON COMOS DEMO'D

T. SIMONITE, MIT TECHNOLOGY REVIEW, SEPT-OCT, 2014, p. 17; ALSO E. BROOKNER, "RECENT ACHIEVEMENTS", IEEE ARRAY-2013; E. BROOKNER, "BREAKTHROUGHS IN PHASED ARRAYS & RADAR", IEEE ARRAY-2010.

diffraction limit, $\lambda/80$, at 375 MHz; In cell phones provides antennas 5X smaller ($1/10\text{th } \lambda$) having 700 MHz-2.7 GHz bandwidth; The Army Research Laboratory in Adelphi MD has funded the develop-

ment of a low profile metamaterial 250-505 MHz antenna having a $\lambda/20$ thickness; Provides isolation between antennas with 2.5 cm separation equivalent to 1 m separation; used for phased array WAIM; n-doped graphene has negative index of refraction, first such material found in nature; Digital Processing and Moore's Law: Not dead yet; Slowed down but has much more to go; Expect increase in transistors density by about a factor of ~ 50 in the next 30 years and reduction in signal processing power consumption by factor of ~ 75 ; and then there is graphene which has potential for terahertz transistor clock speeds, manufacture on CMOS demonstrated, could allow Moore's law to march forward using present day manufacturing techniques; there is also spintronics which could revolutionize the computer architecture away from the John von Neumann model; and there is finally doing computation the way the brain efficiently and amazingly does perhaps by using synaptic transistors and/or memristors, remember the brain only weighs about 2-3 pounds and uses only ~ 20 W, we have a long way to go; Low Cost Packaging: Raytheon funding development of low cost flat panel X-band AESA using COTS type printed circuit boards (PCBs); Rockwell Collins doing it for airborne AESA; Lincoln-Lab./MA-COM developing low cost S-band flat panel array using PCBs, overlapped subarrays and a T/R switch instead of a circulator; SAR/ISAR: Principal Components of matrix formed from prominent scatterers track history used to determine target unknown motion and thus compensate for it to provide focused ISAR image. Technology and Algorithms: A dual polarized, low profile, ($\lambda/40$), wideband (1:20) antenna can be built using tightly coupled dipole antennas (TCDA); Lincoln Lab increases spurious free dynamic range of receiver plus A/D by 40 dB; MEMS: reliability reaches 300 billion cycles without failure; Has potential to reduce the T/R module count in an array by a factor of 2 to 4; Can provide microwave filters 200 MHz wide tun-

able from 8-12 GHz; MEMS Piezoelectric Material = piezoMEMS: Enables flying insect robots; Printed Electronics: Low cost 1.6 GHz (goal 2.4 GHz) diodes printed with Si and NbSi₂ particles; Electrical and Optical Signals on Same Chip: IR beams could be used for transporting on computer chips digital information at the speed of light; COSMOS: DARPA revolutionary MMIC program: Allows integration of III-V, CMOS and opto-electronics on one chip without bonded wires leading to higher performance, lower power, smaller size, components; Graphene and Carbon Nanotube (CNT): potential also for non-volatile memory, flexible displays and camouflage clothing, self-cooling, IBM producing 200 mm wafers with RF devices; Superconductivity: We may still achieve superconductivity at room temperature; Superconductivity recently obtained for first time with iron compounds; Biodegradable Array of Transistors or LEDs: Imbedded for detecting cancer or low glucose; can then dispense chemotherapy or insulin; Quantum Radar: See stealth targets; New polarizations: OAMs, (Orbital Angular Momentum) unlimited data rate over finite band using new polarizations?? Bio: Biodegradable array of transistors or LEDs for detecting cancer or low glucose, can then dispense chemotherapy or insulin; Can now grow functioning non-rejecting kidney and heart for rats.

**Decision (Run/Cancel) Date for this Courses is
Wednesday, March 7, 2016**

Payment received by March 3

IEEE Members \$300

Non-members \$340

Payment received after March 3

IEEE Members \$340

Non-members \$370

To Register, <http://ieeeboston.org/event/phased-array-and-adaptive-array-fundamentals-and-their-recent-advances-spring-2016>

Please take this short survey, <https://www.surveymonkey.com/r/B8R2DYL>

Software Development for Medical Device Manufacturers - An intensive two-day course

Time & Date: 8:30AM - 4:30PM; Wednesday & Thursday, March 30 & 31, 2016

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Steven Rakitin, Quality Software Consulting

SUMMARY:

Developing software in compliance with FDA, EU regulations and international standards is challenging. This two-day intensive course provides practical guidance and suggestions for developing software that complies with applicable FDA and EU regulations, guidance documents and international standards such as IEC 62304 and ISO 14971. The focus of this course is interpreting Design Controls for software. Each section of the Design Controls regulation (820.30) is discussed from the software perspective. Corresponding requirements from IEC 62304 are woven into the flow.

In-depth discussion of critical topics such as Requirements, Software Verification & Validation, Risk Management and Fault Tree Analysis are included. In addition, techniques for validating software development tools and software used in Manufacturing and Quality Systems are also discussed. Interactive group exercises are included to facilitate discussion and learning.

WHO SHOULD ATTEND

Software and firmware engineers, software managers, RA/QA staff, validation engineers, and project managers. Anyone interested in learning how to develop medical device software in compliance with regulations, standards and guidance documents.

COURSE OUTLINE

• Introduction

- Medical Device Definitions – FDA and EU
- Regulatory Roadmap and FDA/EU Device Classification Schemes
- FDA Regulations and Guidance Documents for Software
- Standards – ISO 13485, IEC 62304, ISO 14971, EN-14971, IEC 60601, and IEC 62366-1
- All Software is Defective

• Interpreting Design Controls for Software

- Software Development Models
- Design and Development Planning
- Design Inputs
 - About Requirements...
 - Requirements Exercise
- Design Outputs
- Design Reviews
- Design Verification
 - Software Verification Techniques
- Design Validation
 - Software Validation Process
 - Validation Exercise
- Design Transfer
- Design Changes
- Design History File

• Validation of...

- Software Tools used to develop Medical

Device Software

- Software used in Manufacturing
- Software used in Quality Systems

• Risk Management

- Standards and Regulations
- Terms and Concepts
- Risk Management Process
- Risk Management Tools and Techniques
 - Fault Tree Exercise
- Data Collection and Analysis
- Documentation Requirements

• Summary**• Comprehensive reference materials included**

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Life Senior member of IEEE and a member of MassMEDIC.

He is on the Editorial Review Board for the ASQ Journal Software Quality Professional.

As President of Software Quality Consulting Inc., he helps medical device companies comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

Speaker Bio:

Steven R. Rakitin has over 40 years experience as a software engineer and software quality manager. He helped write the first IEEE Software Engineering Standard (IEEE-STD-730 Standard for Software Quality Assurance Plans) as well as the current revision IEEE 730-2014. He is also a member of the working group writing IEEE Standard 1012 (System Verification & Validation). He has written several papers on medical software risk management as well as a book titled: Software Verification & Validation for Practitioners and Managers.

**Decision (Run/Cancel) Date for this Courses is
Monday, March 21, 2016**

Payment received by March 3

IEEE Members	\$465
Non-members	\$495

Payment received after March 3

IEEE Members	\$495
Non-members	\$545

To Register, <http://ieeeboston.org/event/software-development-for-medical-device-manufacturers-spring-2016>

Antennas and Propagation for Wireless Communications

Time & Date: 6:30 - 9PM; Tuesdays, March 22, 29, April 12, 19, 26, May 3, 10, 17

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Dr. Steven R. Best, MITRE Corporation

Summary: This course provides participants with comprehensive coverage of a wide variety of antenna and propagation topics. The course provides an understanding of basic antenna property definitions, antenna design fundamentals and considerations, numerous antenna types and RF propagation fundamentals. The course also provides an overview of how antenna properties and propagation characteristics affect communication system performance. Topics covered include fundamental antenna performance properties, antenna specifications and data sheets, basic antenna types, elementary antennas, electrically small antennas, wireless device antennas, medical device antennas, low profile antennas, aperture and reflector antennas, circular polarized antennas, antenna arrays, propagation channel characteristics, antenna diversity and MIMO, and an overview of different antennas used in today's wireless communication systems and markets.

Learning Objectives:

Upon completing the course, the participant will be able to:

- Understand the concepts associated with antenna performance, operation and classification.
- Understand, evaluate and define antenna performance specifications.
- Describe and understand a broad spectrum of antenna types.
- Illustrate antenna operating principles with a factual knowledge of antenna theory.

- Understand the basic performance trade-offs associated with antenna design.
- Understand how to design basic antenna elements.
- Understand basic principles associated with the implementation of antenna arrays.
- Understand and describe how antenna performance and the RF propagation environment impact wireless communication system performance.
- Understand the basic types of antennas that are used in today's wireless communications markets.

Target Audience: Anyone working within the field of general RF systems, wireless, cellular and microwave systems will benefit from this comprehensive coverage of antenna properties and design. The course is well suited for design engineers and program managers who require an understanding of antenna principles and design concepts. Basic mathematical and computing skills are a prerequisite for this course. An electrical engineering background or equivalent practical experience is recommended but not required.

Outline:

Part 1:

Basic RF Concepts

- Review of fundamental RF Concepts • Basic design and performance requirements of a wireless

communication system

Basic Antenna Concepts

• Definitions of basic antenna properties: impedance, VSWR, bandwidth, directivity, gain, radiation patterns, polarization, etc.

Types of Antennas

• Resonant antennas • Traveling wave antennas • Frequency Independent antennas • Aperture antennas • Phased arrays • Electrically small antennas • Circularly polarized antennas

Classification of Antenna Types

• By frequency • By size • By directivity

Fundamental Antenna Elements

• The monopole • The dipole • The loop • The folded dipole • The slot

Microstrip Antennas

• Element types • Microstrip element design • Design trade-offs • Designing and 802.11 microstrip patch

Baluns

Ground Plane Considerations

• Vertically polarized antennas • horizontally polarized antennas • The impact of the surrounding environment on antenna performance

Part 2:

Circularly Polarized Antennas

• Achieving circular polarization • The helix antenna • The crossed dipole antenna • The microstrip patch • The quadrifilar helix

Aperture Antennas

• Aperture design concepts • The horn antenna • The reflector antenna • The corner reflector

Impedance Matching

• Impedance matching networks

Broadband Antennas

• Monopole configurations • Feed considerations • Dipole configurations • Bandwidth improvement techniques

Frequency Independent Antennas

• The log-periodic antenna • The spiral antenna

Electrically Small Antennas

• Impedance, bandwidth and quality factor of antennas • Defining electrically small • Fundamental

performance limitations • The small dipole • The small loop • Design and Optimization of small antennas

Part 3:

Antenna Arrays

• Fundamental array theory • Types of antenna arrays • Feed network design considerations • Beam steering and shaping concepts • Performance trade-offs • Microstrip patch arrays • Dipole element arrays

Friis Equation and Link Budget

• The communication link • Understanding and calculating path loss • Receiver Sensitivity and antenna noise figure • Link budget calculations

Receiving Properties of Antenna

• How does an antenna capture power • Aperture area and efficiency • Coupling between antennas

Fractal Antennas

• Fractal antenna types • Performance properties of fractal antennas

RFID Antennas

• RFID system basics • Performance properties of RFID antennas

Ultra Wideband (UWB) Antennas

• Time domain considerations in antenna design • Antenna performance requirements in UWB systems

Low Profile Antennas

• The inverted L and inverted F antennas • The planar inverted F antenna (PIFA)

Device Integrated Antennas

• Antennas commonly used in wireless device applications

Part 4:

Propagation Channel Considerations

• RF path loss • Reflection, multipath and fading • Noise and interference • Polarization distortion • Diversity implementation • MIMO

Types of Antennas used in Communications Systems

• Wireless base station antennas • Wireless handset and portable device antennas • GPS antennas • HF, UHF and VHF communication antennas • Earth station and satellite communication antennas

Numerical Modeling of Antennas

• Software packages • Comparison with measurements

Antenna Design and Simulation Examples Using Commercial Antenna Design Software

Speaker Bio: Steven R. Best is a Senior Principal Sensor Systems Engineer with the MITRE Corporation in Bedford, MA. He received the B.Sc. Eng and the Ph.D. degrees in Electrical Engineering in 1983 and 1988, respectively, from the University of New Brunswick in Canada. Dr. Best has over 28 years of experience in business management and antenna design engineering in both military and commercial markets. Prior to joining MITRE, Dr. Best was with the Air Force Research Laboratory (AFRL) at Hanscom AFB, where his research interests included electrically small antennas, wideband radiating elements, conformal antennas, antenna arrays and communications antennas. Prior to joining AFRL, he was President of Cushcraft Corporation in Manchester, NH from 1997 to 2002. He was Director of Engineering at Cushcraft from 1996 to 1997. Prior to joining Cushcraft, he was co-founder and Vice President and General Manager of Parisi Antenna Systems from 1993 through 1996. He was Vice President and General Manager of D&M/Chu Technology, Inc. (formerly Chu Associates) from 1990 – 1993. He joined Chu Associates as a Senior Electrical Engineer in 1987.

Dr. Best is the author or co-author of 3 book chapters and over 100 papers in various journal, conference and industry publications. He frequently presents a three-day short course for the wireless industry titled “Antennas and Propagation for Wireless Communication”, he is the author of a CD-ROM series on antenna theory and design, and he has presented several Webinars on antenna topics. He has also authored an IEEE Expert Now module on electrically small antennas. Dr. Best is a former Distinguished Lecturer for IEEE Antennas and Propagation Society (AP-S), a former member of the AP-S AdCom, a former Associate Editor for the IEEE Transactions on Antennas and Propagation, and Senior Past Chair of the IEEE Boston Section. He is also a former Editor-in-Chief for AP-S Electronic Communications. Dr Best is a Fellow of the IEEE and a Past-President of the IEEE Antennas and Propagation Society.

Decision (Run/Cancel) Date for this Courses is Friday, March 11, 2016

Payment received by March 8

IEEE Members	\$425
Non-members	\$455

Payment received after March 8

IEEE Members	\$455
Non-members	\$475

To Register, <http://ieeeboston.org/event/antennas-and-propagation-for-wireless-communications>