BOSTON

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IEEE
Advancing Technology for Humanity

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Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

IEEE Boston Section Online Courses:

Verilog101:Verilog Foundations CLASS DESCRIPTION: Verilog is IEEE standard 1364. It is a Hardware Description Language that is the corner stone of much of the simulation world. Verilog Foundations is a comprehensive introduction to the IEEE 1364 (Verilog). The Verilog Foundations class has a slightly different approach to learning Verilog than other methods. There is a lecture section for each main topic. This presents a basic foundation for the language. What makes Verilog Foundations exciting is the emphasis on labs/examples. There are nearly 100 labs/examples giving comprehensive "how to" examples of most Verilog language constructs. There are working solutions for each lab and the students can use the lab database for developing their own models later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace.
(Register at http://www.ieeeboston.org) and click on course title

System Verilog 101: Design Constructs CLASS DESCRIPTION: SytemVerilog is an extensive set of language constructs to the IEEE 1364-2001 standard. It's meant to aid in the creation and verification of models. There are two parts to the language extension. The first part covered by this class, is new design constructs. The second part of SystemVerilog is verification constructs, covered by SystemVerilog102. There are over 100 labs/examples giving comprehensive "how to" examples of most SystemVerilog language constructs. There are working solutions for each lab and the students can use the lab database for developing their own models later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace. There are self-grading quizzes for each chapter that allow the student to see if he/she is learning the material. The goals of this course are to make you familiar with the new part of the language. Students taking SystremVerilog101 will have a 90-day access to it. The lab database you will be able to download and is yours to keep. **(Register at http://www.ieeeboston.org) and click on course title**

System Verilog 102: Verification Constructs CLASS DESCRIPTION:SytemVerilog is an extensive set of language constructs to the IEEE 1364-2001 standard. It's meant to aid in the creation and verification of models. There are two parts to the language extension. The first part covered by SV101, is new design constructs. SV102, this class, covers verification constructs. SystemVerilog102, like all CBE classes, is lab based. There are over 30 verification labs/examples giving comprehensive "how to" examples of most SystemVerilog verification language constructs. There are working solutions for each lab and the students can use the lab database for developing their own assertions later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace. **(Register at http://www.ieeeboston.org) and click on course title**

Introduction to Embedded Linux Part I CLASS DESCRIPTION: This first of a 2-part series introduces the Linux Operating System and the use of Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part covers the methods for booting Embedded Linux distributions including embedded cross-development and target board considerations.

High Performance Project Managment CLASS DESCRIPTION: This12 hour course(broken into short 10 to 20 minute independent modules) provides the project methodology, concepts, and techniques that ensure successful completion (on time, on budget, with the quality required) of projects, large and small. Participants learn the steps to take before, during, and at the end of a project to hone planning and execution to a strategically built process that delivers project success when used. Additionally, the course provides the interpersonal and leadership techniques to ensure everyone involved with the project whether a team member, organization member, or outside of the organization commits to the success of the project—voluntarily—and provides the support and assistance to ensure its success. In addition to learning how to master the technical skills that have evolved over thousands of years of project implementation and practice, the course provides the advanced team building, leadership, and interpersonal skills that ensure the technical skills can be used, they way they are designed to be used, resulting in a process that delivers the on time, on or under budget, with the quality required completed project consistently.

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Computer Society and GBC/ACM - 7:00 PM, Thursday, 18 August

The Technical Challenge of Hate Speech, Incitement and Extremism in Social Media

Andre Oboler, Online Hate Prevention Institute

This talk is being sponsored by the IEEE Computer Society Distinguished Visitor program.

The primary challenge is working out how to identify incitement and hate speech given: (a) the volume of content creation in social media (b) the use of videos, images, coded language, local references etc (c) the changing nature of the expression over time (d) limitations that prevent governments demanding access to non-public data

Further, without knowing what the public is reporting to the social media platforms, how can a governments judge if social media platforms are responding adequately? This has come up in cases like the murder of Leigh Rigby (the Telegraph reports: “Facebook ‘could have prevented Lee Rigby murder’”, Sky News “Facebook Failed To Flag Up Rigby Killer’s Message”) it’s also been a hot topic in the US Congress e.g. ABC News reports, “Officials: Facebook, Twitter Not Reporting ISIS Messages”. The latest, is from Israel where Internal Security Minister Gilad Erdan said Facebook has blood on its hands for not preventing recent killings. He is quoted by Al-Monitor as saying, “[The Facebook posts] should have been monitored in time, and [the murder] should have been averted. Facebook has all the tools to do this. It is the only entity that, at this stage, can monitor such a tremendous quantity of materials. It does it all the time for marketing purposes. The time has come for Facebook to do the same thing to save lives.”

The approach my organisation uses relies on crowd sourcing, artificial intelligence and cloud computing. It enables content to be evaluated by people, but then quality controls the response of the crowd through AI. It allow empirical results to be gathered, such as those reflected in this report we produced for the Israeli Government on antisemitism in social media:http://mfa.gov.il/MFA/ForeignPolicy/AntiSemitism/Pages/Measuring-the-Hate-Antisemitism-in-Social-Media.aspx

Dr Andre Oboler is CEO of the Online Hate Prevention Institute, an Australian charity combating racism, bigotry and extremism in social media. He also serves as an expert on the Australian Government’s Delegation to the International Holocaust Remembrance Alliance, co-chair of the Working Group on Antisemitism on the Internet and in the Media for the Global Forum to Combat Antisemitism, and as a Vice Chair of the IEEE Computer Society’s Member and Geographic Activities Board. Dr Oboler holds a PhD in Computer Science from Lancaster University (UK), a Juris Doctor from Monash University (Australia) and completed a Post Doctoral Fellowship in Political Science at Bar-Ilan University (Israel). His research interests include empirical software engineering, process improvement, hate speech in social media and the social implications of technology. Web: Online Hate Prevention Institute www.ohpi.org.au; personal website www.oboler.com.

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

This joint meeting of the Boston Chapter of the IEEE Computer Society and GBC/ACM will be held in MIT Room E51-325. E51 is the Tang Center on the corner of Wadsworth and Amherst Sts and Memorial Dr.; it's mostly used by the Sloan School. You can see it on this map of the MIT campus. Room 325 is on the 3rd floor.

Up-to-date information about this and other talks is available online at http://ewh.ieee.org/r1/boston/computer/. You can sign up to receive updated status information about this talk and informational emails about future talks at http://mailman.mit.edu/mailman/listinfo/ieee-cs, our self-administered mailing list.

Electromagnetic Compatibility Society - 7PM , Wednesday, 24 August
EEE Distinguished Lecturer for the EMC Society

Bringing Precision to Measurements for Millimeter-wave 5G Wireless

(conducted and free-field modulated-signal measurements)

Speaker: Dr. Kate Remley from NIST

At millimeter-wave frequencies and for wide modulation bandwidths, the hardware performance of both modulated-signal sources and vector receivers becomes increasingly nonideal.

These nonidealities make test and validation of devices, circuits and systems not only more important, but also more difficult. This is especially true because future systems will likely push the limits of modulation complexity and bandwidth to increase data throughput. We will discuss calibration and measurement techniques to correct millimeter-wave modulated-signal measurements illustrating that traditional assumptions at microwave frequencies may not be adequate at millimeter-wave frequencies

Kate A. Remley (S'92-M'99-SM'06-F'13) was born in Ann Arbor, MI. She received the Ph.D. degree in Electrical and Computer Engineering from Oregon State University, Corvallis, in 1999. From 1983 to 1992, she was a Broadcast Engineer in Eugene, OR, serving as Chief Engineer of an AM/FM broadcast station from 1989-1991. In 1999, she joined the RF Technology Division of the National Institute of Standards and Technology (NIST), Boulder, CO, as an Electronics Engineer. She is currently the leader of the Metrology for Wireless Systems Group at NIST, where her research activities include development of calibrated measurements for microwave and millimeter-wave wireless systems, characterizing the link between nonlinear circuits and system performance, and developing standardized test methods for RF equipment used by the public-safety community.

Dr. Remley was the recipient of the Department of Commerce Bronze and Silver Medals, an ARFTG Best Paper Award, and is a member of the Oregon State University Academy of Distinguished Engineers. She was the Chair of the MTT-11 Technical Committee on Microwave Measurements from 2008 - 2010 and the Editor-in-Chief of IEEE Microwave Magazine from 2009 - 2011, and is the Chair

of the MTT Fellow Nominating Committee.

Meeting Details: The meeting of the EMC Society will be held on Wednesday, August 24, 2016 at Bose Corp., 100 The Mountain Road, Framingham, MA. The technical presentation will commence at 7:00PM following a social hour at 6:00 PM Food is provided.
DIRECTIONS TO BOSE CORPORATE HEADQUARTERS:
The address is;100 The Mountain Road, Framingham, MA, 01701

From Mass Pike (I-90); Take Exit 12 (Route 9 West) toward Worcester. Keep left at the fork on the ramp and get on Route 9 West. At the first set of lights take a right onto California Ave. (sign reads "Framingham Technology Park"). Go straight, over the railroad tracks, and through the next set of lights. The road curves around to a stop sign at the foot of the mountain. Take a left onto the Mountain Road and follow it to the next stop sign at the top of the mountain. The tall glass building before you is the Bose Corporate Center. Take a right at the stop sign, drive past the front of the Corporate Center and then park.

For more information, please contact Mike Royer at Michael_Royer@bose.com

Locally held IEEE Conferences

2016 IEEE High Performance Extreme Computing Conference
September 13 - 15 2016
(Conference and hotel registration now open!!!)
www.ieee-hpec.org

2017 IEEE International Symposium on Technolgies for Homeland Security
April 25 - 26, 2017
www.ieee-hst.org
(Note new paper submission schedule: Submission deadline is October 17, 2016)

2016 IEEE International Symposium on Phased Array Systems & Technology
October, 18 - 21 2016
(Conference and hotel registration now open!!!)
www.array2016.org

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Hey!!! There's a Constitutional Amendment on Your Next IEEE Elec-tion Ballot

What!!? There's an IEEE Constitution? Someone wants to change it? Do I care?

Maybe these thoughts went through your mind when you read the title. Legitimate questions all. For most of us the IEEE Constitution doesn't really seem to be of much significance, being mainly for activists, people seeking office and staff. The IEEE runs itself pretty well and is in the more than adequate hands of the volunteer leaders, staff and paid executives. It's not of much interest technically.

I certainly agree, but there is a catch. It only works well because we, the members have a lot to say about how this pretty big (should I say huge?) organization runs. I am sure we would like to continue that and keep it working for us.

Hence, like anywhere else that there is a constitution, change can be hazardous and needs careful thought and consideration. Even the placement of a comma can fundamentally change the meaning of a provision.

It's incumbent on all of us to consider how this upcoming amendment will affect the future of IEEE and not just accept what the corporate staff thinks, or what a friend thinks, for example. We should make up our own mind and vote intelligently and thoughtfully.

The link below takes you to the official IEEE page which has a lot of information, including some statements in opposition to the amendment. You can also search for IEEE Constitutional Amendment on the search engine of your choice.

There is a lot of information here and it's admittedly a little hard to understand the significance of it all. I'm hardly an IEEE "Constitutional Scholar", but a few points stand out.

First of all there does not seem to be any straight amendment offered, only a compendium of changes in a number of formats integrated into the existing Constitution. Maybe this is okay giv-en the complexity of the issue, but unless you look at everything it's a bit hard to understand.

Some other issues with the amendment as presented are:

- There seems to have been little real discussion or visibility into this amendment in local organ-izations.
- Dissenting comments cannot be presented from a group, but are attributed to a single member, reducing the impact of a group with the same dissent.
- Only one dissenter on individual points of disagreement is posted, in spite of the high probability that there are multiple views on each issue, both positive and negative.
- We are not privy to any of the internal discussions of the Board, so we do not know how they individually feel or how passionate is the defense or support for any element of this amend-ment.

Law, constitutional change and sausage have a lot in common as the old saying goes. It's a lot easier to sit back and simply consume the result. But it also suggests that you need to carefully read the ingredients and know a bit about the process. If the marketing materials look a little too slick, maybe it is best not to buy into it today and get smart first.

https://www.ieee.org/about/corporate/election/2016_constitutional_amendment.html

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

So here's my bottom line - Please take a very careful look at this amendment before you vote.

If you have any doubts, vote No. Voting No doesn't make the change disappear forever, but it does let the framers know the issue needs to be thought out more and re-presented. The old constitution has served us well until now. We do not seem to be proposing solutions to urgent problems; more discussion over the next couple of years couldn't hurt anything. It might even convince some of us dissenters that this will make things better.

On the other hand if you totally agree that this is solving an urgent need for change, won't hurt, and won't get any better through more discussion and consideration, then you have the option of voting Yes.

It's all up to us, it really is.

Fausto Molinet, Past Chair of the Boston Section and Chair of the Boston Section Publi-cations Committee

This year, the IEEE election includes an important amendment that alters the management structure of the IEEE.

Your review of this issue requires your attention as to how it impacts your membership.

In the August Digital Reflector, there are materials and some perspective on this Amendment.

The Constitutional Amendment which will be voted on in this year's election, I implore you so deeply read this Amendment and the included comments, as well as discuss it with your other IEEE colleagues.

Here, then, are links to a variety of background materials that could help you decide on your position on the impending amendment:

1. The proposed changes to the Constitution are posted at:
https://www.ieee.org/about/corporate/election/2016_constitutional_amendment.html

2. Separately, information about the IEEEin2030 effort to evolve the IEEE organizational structure is posted at:
https://www.ieee.org/about/corporate/ieeein2030_archive_m.html

3. There is also information on the amendment posted at:
https://ieeeconstitutionamendment.wordpress.com/

4. Those opposing the 2016 IEEE Constitutional Amendment have posted information why they are opposed at:
https://ieee2016blog.wordpress.com/
and
https://ieee2016blog.wordpress.com/category/opposition-statements/

5. The IEEE governing documents, including the Constitution and Bylaws, are posted at:
http://www.ieee.org/about/corporate/governance/index.html

When you vote on your ballot in August, please consider the impact on your membership and the future of the leadership of the IEEE.

Kevin Flavin
2016 Chair, IEEE Boston Section

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Modern Topics in Power Amplifiers

Times and Dates: 6 - 8PM, Tuesdays, Sept. 27, Oct. 4, 11, 18, 25

Location: MIT Lincoln Laboratory, 5 Forbes Rd, Lexington, MA 02421

Overview

This five week lecture series is intended to give a tutorial overview of the latest developments in power amplifier technology. It begins with a review of RF power amplifier concepts then teaches the modern MMIC design flow process. Efficiency and linearization techniques are discussed in the following weeks. The course is concluded with a hands on demonstration and exercise, brought to you by National Instruments, where participants will see how DPD and envelope tracking are implemented with actual hardware.,

Target audience

The material is taught at a level that any electrical engineer should be able to understand. If your memory of RF amplifier concepts is a little rusty, make sure to catch the first lecture on September 27th.

Goals/Benefits of attending

This course aims to give a broad overview of state-of-the-art PA techniques with practical hardware demonstrations.

Schedule/Outline

<u>September 27th</u>

Amplifier Basics, by Dr. Nestor Lopez of MIT Lincoln Laboratory

- RF Amplifier Characteristics
- Linearity
- Efficiency
- Modes of Operation
- LNA vs. HPA
- Amplifier Classes
- Amplifier Implementation
- Small Signal Theory
- Large-Signal Transistor Characterization
- Bias Networks
- Power Combining

<u>October 4th</u>

MMIC Design Flow, by Dr. Youngho Suh of MIT Lincoln Laboratory

– Foundry selection with PDK availability
– Frontend Design
• Bias selection with loadline / loadpull, reliablility
• Drive budget estimation for multi-stage cascade design
• Periphery estimation for target specification
• Matching topology selection
– Circuit Simulation
• Small signal linear simulation
• Large signal linear simulation (Cripps method)
• Large signal nonlinear simulation
– Layout and EM simulation
• Real estate war!
• Package interface
• 2 and 3D EM simulation tools
– Verification
• DRC and LVS
– Sensitivity, yields, stability…etc

<u>October 11th</u>

High Efficiency Architectures, by Dr. Andrew Zai of MIT Lincoln Laboratory

- Fundamental Equations of Linearity and Efficiency
- Classes of Amplifiers and their Theoretical Efficiencies
  - Class A, AB, B, C
- Compression and Switched Mode PAs
  - Compression
  - Class D, Class F/F^-1
- High Efficiency Architectures

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

- Outphasing
- Doherty
- Envelope Tracking

Digital Transmitter, Dr. Rui Ma of Mitsubishi Electric Research Labs
-Class-S mode
- GaN for Digtial TX
- Power encoding
- Delta-sigma Modulation
- Pulse Width Modulation
- Implementation of Digital TX
- FPGA
- ASIC

October 18th
Predistortion Techniques, by Dr. Andrew Bolstad of MIT Lincoln Laboratory
- Why nonlinear systems?
- Linear vs. Nonlinear Systems
- Predistortion and Equalization
- Nonlinear System Models
- AM/AM and AM/PM
- Box Models
- Memory Polynomials and Generalized Memory Polynomials
- Volterra Kernels
- Pruned / Sparse Volterra Kernels
- Identification of Model Parameters
- Direct / Indirect Learning
- Training signals

Digital Predistortion System and Demo, by Dr. Kevin Chuang of NanoSemi, Inc.
- DPD System Architecture and Consideration
- Real-Time DPD Demonstration
o Traditional Linearization based on Static DPD and Generalized Memory Polynomials
o NanoSemi's Ultra-Wideband Proprietary Linearization
- Benefits of NanoSemi's Linearizer

October 25th
Presentation and Hands on Hardware Demonstration from National Instruments on Digital Predistortion and Envelope Tracking
ET/DPD Measurement System Introduction
o Instrumentation requirements for testing ET/DPD-enabled PA's
o [Hands-on] PA measurement walk-through (EVM, ACLR/SEM, AM-AM/AM-PM)
o [Demo] Effects of synchronization misalignment
o [Hands-on] ET shaping function
o [Hands-on] DPD model identification
FPGA-based DPD reference design
o Motivation
-DPD potentially becoming a part of component test
- Prototyping algorithms
o Software-based DPD algorithm considerations
-Stimulus/response time, phase, amplitude alignment
-Model extraction
o Overview of system platform
-Vector Signal Transceiver (VST) architecture
-A look at the instrument's DSP chain
o FPGA Algorithm
-Predistorter implementation
-Demo
-Efficient time/phase/amplitude alignment algorithm
-Demo
Linearize your own PA
o Attendee brings their own non-linear PA to test with measurement hardware

Light snacks will be provided

Decision (Run/Cancel) Date for this Courses is Tuesday, September, 20, 2016

Payment received by September 15
IEEE Members $150
Non-members $180

Payment received after September 15
IEEE Members $180
Non-members $195

http://ieeeboston.org/modern-topics-power-amplifiers/

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Digital Signal Processing (DSP) for Wireless Communications - Under the Hood

Time and Dates: 6 - 9PM, Wednesdays, October 19, 26, November 2, 9, 16

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Dan Boschen, Microsemi

Course Summary:

This course is a fresh view of the fundamental concepts of digital signal processing most applicable to practical real world problems and applications in radio communication systems. This course will build an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real world applications in GPS and mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges in both the analog and digital domains, and not a tutorial on working with specific DSP processor hardware.

Target Audience:

All engineers involved in or interested in signal processing applications. Engineers with significant experience with DSP will also appreciate this opportunity for an in depth review of the fundamental DSP concepts from a different perspective than that given in a traditional introductory DSP course.

Benefits of Attending/ Goals of Course:

Attendees will build a stronger intuitive understanding of the fundamental signal processing concepts involved with digital filtering and mixed signal communications system design. With this, attendees will be able to implement more creative and efficient signal processing architectures in both the analog and digital domains

Topics / Schedule:

Class 1:
Correlation
Fourier Transform
Laplace Transform

Class 2:
Sampling and A/D Conversion
Z –transform
D/A Conversion

Class 3:
IIR and FIR Digital filters
Direct Fourier Transform

Class 4:
Windowing, Digital Filter Design
Fixed Point vs Floating Point

Class 5:
Fast Fourier Transform
Multirate Signal Processing
Multi-rate Filters

Speaker's Bio:

Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 20 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technol-

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

ogies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems. Dan is currently at Microsemi (formerly Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page at: http://www.linkedin.com/in/danboschen

Decision (Run/Cancel) Date for this Courses is Tuesday, October 11, 2016

Payment received by October 5
IEEE Members $325
Non-members $360

Payment received after October 5
IEEE Members $360
Non-members $425

http://ieeeboston.org/digital-signal-processing-dsp-wireless-communications/

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Open Source Tools for Computational Biomechanics

Times & Dates: 8AM – 5PM, Thursday, September, 15, 2016

Location: MIT Media Lab, Biomechatronics 75 Amherst Street Cambridge, MA 02139

Speakers: Kevin Moerman, Centre for Extreme Bionics, MIT Media Lab.
Steve Maas, University of Utah, Scientific Computing and Imaging Institute
Christopher Dembia, Stanford University

Overview

Computational biomechanics is a rapidly evolving field. New software tools have enabled detailed investigation of the biomechanical behavior of human soft tissue as well as the study of human motion and musculoskeletal biomechanics. These tools are now being used for patient-specific biomechanical analysis, medical device design, and rehabilitation research.

This course provides an introduction to a set of free and open source tools for computational biomechanics, namely GIBBON, FEBio and OpenSim. GIBBON provides a MATLAB framework for image segmentation, model construction and meshing. GIBBON also interfaces with FEBio, enabling advanced subject-specific and inverse finite element analysis. The OpenSim project allows one to simulate whole-body movements and estimate muscle activity, forces, and energetics.

Examples presented will include MRI based model creation, meshing, inverse material parameter estimation, patient specific medical device optimization. For a hands-on portion of the course participants will be invited to bring their own data, enabling them to initiate the use of the tools presented for their particular research areas.

The course will feature three speakers: Dr. Kevin Moerman (MIT Media Lab), GIBBON developer, Steve Maas (University of Utah), FEBio developer, and Christopher Dembia (Stanford University), who works on the OpenSim project.

Outline

- **Setting up the software environments**

- **GIBBON (The Geometry and Image-Based Bioengineering add-On)**
  - o Data and model visualization
  - o Image-based modelling
  - oSurface modelling and surfaces mesh improvement
  - o Surface and solid meshing techniques
  - o Finite element analysis and FEBio integration

- **FEBio (Finite Elements for Biomechanics**
  - o Material models (hyperelastic, visco-hyperelastic, biphasic)
  - o Boundary conditions and contact modeling
  - o Analysis types (static, transient, dynamic)
  - o Plugin development

- **OpenSim**
  - o Estimating muscle activity from motion capture data
  - o Predictive simulation: combining optimization and simulation
  - o Survey of research studies combining OpenSim with finite element modeling.

- **Workshop and hands-on session**

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Target Audience

The course is targeted towards students, academics, and professionals in biomedical engineering, whose research involves soft tissue biomechanics.

Benefits of Attending

Attendees may benefit from the course by:
1) Being introduced to computational methods for soft tissue biomechanics (including image-based modelling, meshing, and finite element analysis).
2) Gaining hands-on experience in the use of free and open source software tools to solve problems in biomedical research

Speakers' Bios

Kevin M. Moerman is a biomechanical and design engineer. He holds a Bachelor in Mechanical Engineering, and a Masters and PhD in Bioengineering. He is currently program manager for mechanical interfaces at the Biomechatronics department of the MIT Media Lab, where he works on prosthetic socket design. He also holds a visiting research fellow position at Trinity College Dublin collaborating on computational modelling of soft tissue mechanical behavior. During his academic career he has amassed a wealth of computational tools for image-based modelling and inverse finite element analysis, resulting in the creation of his GIBBON open-source software project which he maintains on a voluntary basis. Kevin has shared his work at international conferences and is often involved in the organization of special sessions and workshops.

Steve Maas is a research associate at the University of Utah's Scientific Computing and Imaging Institute. He holds a Master's degree in Physics and is currently finishing his PhD in Computer Science. He is the lead software developer for the FEBio project, a finite element analysis package for soft tissue biomechanics, and has been an integral member of the project's development team since it started in 2006. Since then FEBio has grown into a new standard for finite element analysis in computational biomechanics. It offers tools that are highly relevant for the biomechanics and bioengineering research communities and that are hard to come by in traditional finite element software. Another important aspect of the FEBio project is its focus on outrearch to its users' community, which continues to grow and is currently thousands of members strong. Mr. Maas has presented numerous times on the use of FEBio and given workshops at several international conferences.

Christopher Dembia is a doctoral student at Stanford University in Prof. Scott Delp's Neuromuscular Biomechanics Lab. His research focuses on applying the latest optimal control methods to understand the effect of assistive devices on the metabolic cost of walking. He is also a core software developer for the OpenSim musculoskeletal modeling and simulation package, and works on incorporating the new optimal control methods into OpenSim. OpenSim was first released in 2007 as a GUI and a set of command line tools that allowed one to estimate muscle activity and forces from experimental data of a movement. Today, OpenSim allows users to develop their own custom studies and analyses via MATLAB, Python, and C++ interfaces. The OpenSim software is part of the National Center for Simulation in Rehabilitation Research, which provides workshops, pilot project grants, and webinars related to OpenSim.

Materials for Course: A course handout will be made available covering the course outline, and links the relevant GIBBON, FEBio, and OpenSim examples and documentation.

Decision (Run/Cancel) Date for this Courses is Thursday, September 8

Payment received by September 5
IEEE Members $150
Non-members $185

Payment received after September 5
IEEE Members $185
Non-members $200

http://ieeeboston.org/open-source-tools-computational-biomechanics

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Making You a Leader - Fast Track

Date & Time: **Wednesday, November 30; 8:30AM - 5:00PM**

Location: **Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA**

Speaker: **Robin Goldsmith, President, GoPro Management**

We do projects to make change. Yet, change will not occur without leadership, and leaders are rare. Leaders make others want to do what the leader wants done. Leaders cause ordinary people to achieve extraordinary things. Managing is not the same as leading, and titles do not make leaders. Seminars can teach you to manage, but they cannot teach you to be a leader. Rather, making a leader takes special techniques—such as our personal development clinics—that can change deep-seated behaviors learned over a lifetime.

However, since clinics usually last about ten weeks, this mini-clinic was devised as a more convenient alternative. This format places responsibility upon the participant to carry out an extended informal follow-on program after completion of the formal seminar workshop session.

During the follow-on period, the participant uses time-condensed methods that simulate the lifetime learning which makes a leader. Therefore, commitment to carrying out these exercises is essential for successful transformation.

Participants will learn:

- Leadership characteristics and practices that are essential for project and personal success.
- Differences between management and leadership, how they conflict, and why leaders are so rare.
- Behaviors leaders use to influence others, up and down, to want to do what the leader wants them to do
- Special techniques personal development clinics use to change lifetime learning and make leaders.
- How to employ those special techniques in a follow-on mini-clinic to develop the leadership skills they need to make their projects successful.

WHO SHOULD ATTEND: This course has been designed for business and systems professionals who want to improve their ability to lead and influence other people.

LEADERSHIP CHARACTERISTICS & ROLE
How leadership looks and feels
Management vs. leadership
Leadership components of project success
Basic leadership practices; power sources
Real change leaders in organizations

TEAMS AND LEADERSHIP
Everyone feels leadership is lacking
Everyone thinks s/he is a leader
Results, not actions or intent
Workgroups, teams, and leaders
Situational leadership styles
Coaching and sports analogies to projects

INSPIRING AND MOTIVATING
Gaining commitment to project success
Communicating that influences others
Addressing negativism and groupthink
Conscious and unconscious messages
Greatest management principle
Hierarchy of needs effects on projects
Hygiene factors vs. motivators

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Helping project players get their rewards
Influencing up and down without authority
Inspiring the extra efforts projects need
Energizing the project team

SHARED VISIONS
Relating values and vision to projects
Getting others to embrace one's vision
Developing a motivating project vision

WHERE AND HOW LEADERS ARE MADE
Born or made? How do we know?
Habits of thought that affect project success
Overcoming self-limiting lifetime learning
Leader's critical success factors
Traditional education doesn't make leaders
Special way—personal development clinics

SETTING AND ACCOMPLISHING GOALS
S.M.A.R.T. goals for self and project
Action plans to achieve your goals
Visualizing and emotionalizing

DEFINING THE FOLLOW-ON PROGRAM
Clarifying project leadership objectives
Breaking into prioritized subgoals
Establishing rewarding daily achievements
Special techniques to change habits

CARRYING OUT THE MINI-CLINIC
Working with a follow-up support structure
Mapping results regularly to goals
Objectively recording leadership changes
Self-leadership through the process

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, Discovering REAL Business Requirements for Software Project Success, he regularly works with and trains business and systems professionals.

Decision (Run/Cancel) Date for this Courses is Friday, November 18, 2016

Payment received by November 11
IEEE Members $220
Non-members $245

Payment received after November 11
IEEE Members $245
Non-members $265

http://ieeeboston.org/making-leader-fast-track/

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Defining and Writing Business Requirements

Date & Time: **Monday & Tuesday, December 5 & 6; 8:30AM - 5:00PM**

Location: **Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA**

Speaker: **Robin Goldsmith, President, GoPro Management**

Discovering and documenting business requirements for projects always has been the weakest link in systems development. Up to 67 percent of maintenance and 40 percent of development is wasted rework and creep attributable to inadequately defined business requirements. Too often projects proceed based on something other than what the business people really need; and traditional methodologies commonly focus mainly on the format for writing requirements. This interactive workshop also emphasizes how to discover content, why to build it and what it must do to produce value for the customer/user. Using a real case, participants practice discovering, understanding, and writing clear and complete business/user requirements that can cut creep, speed project delivery, reduce maintenance, and delight customers

Participants will learn:
Avoiding creep--role and importance of defining business requirements accurately and completely.
Distinctions between the user's (business) requirements and the system's (design) requirements.
How to gather data, spot the important things, and interpret them meaningfully.
Using the Problem Pyramid™ tool to define clearly problems, causes, and real requirements.
Formats for analyzing, documenting, and communicating business requirements.
Techniques and automated tools to manage requirements changes and traceability.

WHO SHOULD ATTEND: This course has been designed for systems and business managers, project leaders, analysts, programmer analysts, quality/testing professionals, auditors, and others responsible for assuring business requirements are defined adequately.

REQUIREMENTS ROLE AND IMPORTANCE
Sources and economics of system errors
How requirements produce value
Business vs. system requirements
Survey on improving requirements quality
Software packages and outsourcing
How we do it now vs. what we should do

DISCOVERING "REAL" REQUIREMENTS
Do users really not know what they want?
How the "real" requirements may differ
Aligning strategy, management, operations
Technology requirements vs. design
Problem Pyramid™ tool to get on track
Understanding the business needs/purposes
Horizontal processes and vertical silos
Customer-focused business processes
Who should do it: business or systems?
Joint Application Development (JAD) limits
Management/supervisor vs. worker views

DATA GATHERING AND ANALYSIS
Surveys and questionnaires

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Research and existing documentation
Observing/participating in operations
Prototyping and proofs of concept
Planning an effective interview
Controlling with suitable questions
FORMATS TO AID UNDERSTANDING
Business rules, structured English
E-R, data flow,flow, organization diagrams
Data models, process maps
performance, volume, frequency statistics
Sample forms, reports, screens menus

DOCUMENTATION FORMATS
IEEE standard for software requirements
Use cases, strengths and warnings
7 guidelines for documenting requirements
Requirements vs. implementation scope
Iterating to avoid analysis paralysis
Conceptual system design solutions
Detailing for clarity, clarifying quality

GETTING MORE CLEAR AND COMPLETE
Stakeholders and Quality Dimensions
Addressing relevant quality factor levels
Standards, guidelines, and conventions
Detailing Engineered Deliverable Quality
Simulation and prototyping
Defining acceptance criteria

MANAGING THE REQUIREMENTS
Supporting, controlling, tracing changes
Automated requirements management tools
Measuring the “proof of the pudding”

Speaker’s Bio:
Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, Discovering REAL Business Requirements for Software Project Success, he regularly works with and trains business and systems professionals.

Decision (Run/Cancel) Date for this Courses is Friday, November 18, 2016

Payment received by November 11
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Payment received after November 11
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http://ieeeboston.org/defining-writing-business-requirements/

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Credibly Managing Agile and Other Projects

Skills, Approaches and Methods Needed to Make any Project Succeed!

Date & Time: **Monday & Tuesday, November 28 & 29; 8:30AM - 5:00PM**

Location: **Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA**

Speaker: **Robin Goldsmith, President, GoPro Management**

Despite claims to the contrary, even Agile projects need to be managed in order to succeed. That doesn't—and never did—mean the project manager dictates every little action; but every project must know what to do, how to do it, what it takes, and how to make sure it gets done well. Agile methods help but are not sufficient and can create challenges.

This intensive interactive seminar workshop shows how to manage projects to deliver the results their customers want, on time and in budget. This course helps improve project teams' credibility by better knowing what they're doing so they deliver as promised. Each section of the course shows how to make sure that an additional Critical Success Factor is present and addresses both Agile and other project formats. Case study exercises provide practice applying the techniques and learning how to avoid common pitfalls.

Participants who attend this course may also want to attend "Making You a Leader."

* How lack of credibility often unknowingly affects project success and ways to earn credibility.
* Recognizing and avoiding common, often overlooked pitfalls to on-time, in-budget, quality projects.
* Using Agile and other development life cycles to jumpstart projects confidently and quickly.
* Defining scope so it doesn't creep and building essential transitions to the workplan for achieving it.
* Methods for reliably estimating the time, effort, costs, and resources required.
* Controlling risks and balancing conflicts in the real world of both task and resource constraints.
* Tools and techniques to catch and correct problems early so project promises are kept.

WHO SHOULD ATTEND: This course has been designed for business and development specialists, product owners, scrum masters, managers, analysts, and other project participants.

CRITICAL PROJECT SUCCESS FACTORS
Importance of credibility to project success
Characteristics of successful projects
- Factors that really cause projects to fail
- Agile's view, why no project manager
- Superworker to supervisor to superfluous
- Establishing credibility, managing by facts
- Overcoming Parkinson's Law
- Projects succeed/fail in the first 15 minutes

PROJECT LIFE CYCLE
- Mapping project management/development
- Why we get impossible deadlines/budgets
- Traditional and iterative, Agile models
- Project management deliverables
- System development deliverables
- Proactive Testing□ developer's advantage

ANALYST/DESIGNER ROLE
- Establishing achievable project scope
- Internal & external customers/stakeholders
- Strategic and management alignment
- Identifying project risks
- Requirements, design, user stories, ATDD
- Make vs. buy
- JAD, facilitation, and customer partnering

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High-level conceptual design roadmap

ESTIMATING TIME, EFFORT, RESOURCES
- Understanding causes of poor estimates
- Applying multiple estimating strategies
- Work breakdown structure, controlling risk
- Measuring deliverables, function points
- User story sizing, backlog grooming
- PERT and weighted averages risk reduction
- Cost/benefit analysis and communication

SCHEDULING TO MEET DEADLINES
- Productive time scheduling practicalities
- Time management techniques
- Dependency networking and CPM
- Coordinating multiple projects/resources
- Sprints, releases, strengths and issues
- Managing resource-constrained projects
- Working within Brooks' Law
- Negotiating commitments and resources

CONTROLLING PROJECT COMPLETIONS
- Monitoring against budget and schedule
- Time boxing, burn down charts
- Earned value measure of completion
- Assuring quality and preventing errors
- Automated tools, Kanban boards
- Reporting to stakeholders, management
- Key to advancement

Speaker's Bio:

Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, Discovering REAL Business Requirements for Software Project Success, he regularly works with and trains business and systems pro-

Decision (Run/Cancel) Date for this Courses is Friday, November 18, 2016

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http://ieeeboston.org/managing-agile-projects-skills-approaches-methods/

IEEE Boston Section goes Online!!!'

The IEEE Boston Section is in the process of creating an comprehensive online course presence. We are working to populate our online course offerings with several courses. Our time line is to have the online curriculum operational by September 2017.

• Intro to Embedded Linux • Linux Optimization • Making you a Leader • DSP for Wireless Comm

• Forensics • S/W for Medical Devices • Verilog • Project Management • Linux Android

Please check our website, e-reflector and this Digital Reflector for details moving forward

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Introduction to Embedded Linux

Time & Date: 6 - 9PM; Thursdays, Nov. 10, 17, Wednesdays, Nov. 30, Dec. 7

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Overview - This 4 day course introduces the Linux Operating System and Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part of the course covers testing, booting and configuring of Embedded Linux systems including embedded cross-development and target board considerations.

Who Should Attend – The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives

• To provide a basic understanding of the Linux OS and the Eclipse IDE framework.
• To understand the complexities of Embedded Linux Distributions in embedded systems.
• To learn how to configure, boot and test Embedded Linux distributions and applications running on Embedded Linux target systems.
• To give students the confidence to apply these concepts to their next Embedded Linux project

Hardware and Software Requirements – The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ installation or prior knowledge of C-based Makefiles is useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials

• Linux Kernel Development by Robert Love
• Linux System Programming by Robert Love
• Embedded Linux Primer by Christopher Hallinan
• Pro Linux Embedded Systems by Gene Sally
• Embedded Linux Development Using Eclipse by Doug Abbott
• Linux Device Drivers by Jonathan Corbet et al
• Essential Linux Device Drivers by Sreekrishnan Venkateswaran

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at LynuxWorks, Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based development tools, training and consulting for the embedded systems market.

OUTLINE

Course Schedule Day 1

The Basics
Linux Terminology, History and Versioning

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The Linux Community: Desktop & Embedded
Linux and the GPL
Linux References (Books and Online)
Getting Started
Building the Kernel Source Code
Embedded Linux Kernels
Linux 2.6 and 3.x
Basic Kernel Capabilities
Process and Threads Management
Signals and System Calls
Synchronization, IPC and Error Handling
Timing and Timers
Memory Management and Paging
The I/O Subsystem: A Tale of Two Models
Modularization
Debugging
Process-Level and System-Level Debug
GDB, GDB Server and the GDB Server Debugger
Other Debug and Test Tools
An Eclipse Remote Debug Example
Advanced Debug with printk, syslogd and LTTng
System-Level Debug
System-Level Debug Tools
The /proc Filesystem
Advanced Logging Methods
KGDB and KDB
Crash and Core Dumps

Course Schedule Day 2
Process & Threads Management
What are Processes and Threads?
Virtual Memory Mapping
Creating and Managing Processes and Threads
Thread-Specific Data (TSD)
POSIX
The Native POSIX Threading Library (NPTL)
Kernel Threads
Signals
System Calls
Scheduling
Linux 2.4 and 2.6 Scheduling Models
The O(1) Scheduler
The Completely Fair Scheduler (CFS)
Synchronization
Via Global Data
Via Semaphores, Files and Signals
Condition and Completion Variables
Mutexes and Futexes
Inter-Process Communications (IPC)
Message Queues
Semaphores Revisited
Shared Memory
Pipes and FIFOs
Remote Procedure Calls
Networking

Course Schedule Day 3
Memory Management and Paging
Demand Paging and Virtual Memory
Allocating User and Kernel Memory
Mapping Device Memory
The Slab Allocator
The OOM Killer
Memory in Embedded Systems
Advanced Memory Operations
Linux and Memory
Managing Aligned Memory
Anonymous Memory Mappings
Debugging Memory Allocations
Locking and Reserving Memory
Error Handling
errno and perror
strerror and strerror_r
oops, panics and Segmentation Faults
Timing
How Linux Tells Time
Kernel, POSIX and Interval Timers
High-Resolution Timers (HRTs)
Modularization
Creating a Module and Module Loading
Dependency Issues
In Embedded Systems
Shared Libraries
A Shared Library Example
Static and Dynamic Libraries
The I/O Subsystem: A Tale of Two Models
The Original Device Driver Model
The Standard I/O Interface
Major and Minor Numbers
Configuring the Device Driver

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The Evolution of the New Device Driver Model
The Initial Object-Oriented Approach
Platform Devices, Busses, Adapters and Drivers
Comparing the Two Driver Models

Course Schedule Day 4
Advanced I/O Operations
Standard I/O Operations
Scatter-Gather and Asynchronous I/O
Poll, Select and Epoll
Memory-Mapped I/O
File Advice
I/O Schedulers
Interrupt and Exception Handling
Bottom Halves and Deferring Work
The Linux Boot Process
The Root Filesystem
Desktop Linux Boot
Bootloaders and U-Boot
Embedded Linux Boot Methods
Building and Booting from SD Cards
Managing Embedded Linux Builds
Configuring and menuconfig
Building Custom Linux Images
Target Image Builders
LTIB and Yocto
System Architecture Design Approaches
Deploying Embedded Linux
Choosing and Building the Root Filesystem
Useful Embedded Filesystems
Module Decisions
Final IT Work
Embedded Linux Trends
Some Final Recommendations

Decision (Run/Cancel) Date for this Courses is Monday, October 24, 2016

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IEEE Members $430
Non-members $455

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• Forensics • S/W for Medical Devices • Verilog • Project Management • Linux Android

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Revolutionary Developments in Phased Arrays

BOSTON 2016

18–21 October 2016

Westin Waltham Hotel, Greater Boston, Massachusetts, USA

www.array2016.org

About the Symposium

Phased array systems continue to be a rapidly evolving technology with steady advances motivated by the challenges presented to modern military and commercial applications. This symposium will present the most recent advances in phased array technology and provide a unique opportunity for members of the international community to interact with colleagues in the field of Phased Array Systems and Technology.

Plenary Session Speakers

- **William Delaney** – MIT Lincoln Laboratory
- **Troy Olsson** – DARPA
- **Israel Lupa** – IAI ELTA, Israel
- **Gordon Frazer** – DSTO Australia
- **Joseph Haimerl** – Lockheed Martin
- **Tony Fischetti** – Northrop Grumman Corp.

SESSIONS

Plenary
European Phased Array Systems and Technology*
Array Design I, II, III
T/R Modules
Radar I, II
Beamforming and Calibration I, II, III
Emerging Technologies for Wideband Arrays*
Communications Arrays
Array Measurements
Signal Processing and Architectures
Dual Polarization Weather Radar Arrays
Multifunction Arrays
Millimeter Wave and Terahertz Arrays*
Metamaterial Phased Arrays*
MIMO Arrays
Conformal Arrays
Poster Sessions I & II

*Special Session

Tutorials

- Phased Arrays for MIMO Radar
  Dr. Vito Mecca, MIT Lincoln Laboratory
- Smart Antennas
  Dr. Frank Gross, Boeing Technical Fellow, Georgia Southern University
- T/R Modules for Phased Arrays
  Dr. William H. Weedon, Applied Radar
- Phased Array Antenna Measurements
  Dr. Alan J. Fenn, MIT LL
- Advances in SiGe BiCMOS Technology with Chip Scale Phased Array Applications
  – Dr. Gabriel Rebeiz, UCSD
- Phased Arrays for Imaging Applications
  Dr. Carey Rappaport, Northeastern University
- Microwave Array Beamforming: Analog, Digital, and Photonic
  Dr. Jeffrey Herd, MIT Lincoln Laboratory
- Phased Arrays: Basics, Breakthroughs & Future Trends
  Dr. Eli Brookner, Raytheon (Retired)

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Advanced Embedded Linux Optimization

Time & Date: 6 - 9PM, Mondays, January 9, 16, 23, 30, 2017

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand methods for debugging, profiling and testing Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.
- To give students the confidence to apply these concepts to their next Embedded Linux project.

OUTLINE

Course Schedule Day 1

Getting Started with Embedded Linux
Linux and the GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs
Linux References (Books and Online)
Basic Debugging Review
Embedded Applications Debugging
GDB, GDB Server and the GDB Server Debugger
An Eclipse Remote Debug Example
Debugging with printk and LTTng
System Logs
Other Debuggers
System-Level Debug
System-Level Debug Tools
The /proc and /sys Filesystems
Basic Logging
KGDB and KDB
Crash Dumps and Post-Mortem Debugging
Debugging Embedded Linux Systems
Backend Debuggers
JTAG and In-Circuit Emulators
Hardware Simulators
Analyzers
Debugging Device Drivers
Kernel Probes
Kexec and Kdump
Kernel Profiling

Course Schedule Day 2

Testing
Design for Test
Agile Software Design
Unit-Level Testing
System-Level Testing
Code Coverage Tools
gcov
Automated Testing
DebugFS
Configuring DebugFS
DebugFS Capabilities
Advanced Logging
LogFS
Using Logwatch and Swatch
Using syslogd and syslog-ng

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Kernel Hacking
Configuring Kernel Hacking
Kernel Hacking Capabilities
Tracing
ptrace and strace
New Tracing Methods
SystemTap
Ftrace, Tracepoints and Event Tracing
Tracehooks and utrace

Course Schedule Day 3
Profiling
Basic Profiling
gprof and Oprofile
Performance Counters
LTTng
Another DDD Example
Manual Profiling
Instrumenting Code
Output Profiling
Timestamping
Measuring Embedded Linux Performance
Some Ideas on Performance Measurement
Common Considerations
Uncommon Considerations
Using JTAG Methods
BootLoader Optimizations
Boot Time Measurements
Effective Memory and Flash Usage
Filesystem Choices
Addressing Performance Problems
Types of Performance Problems
Using Performance Tools to Find Areas for Improvement
Application and System Optimization
Device Driver Optimization
CPU Usage Optimization
Memory Usage Optimization
Disk I/O and Filesystem Usage Optimization
The Perf Tool
Improving Boot Performance
Boot Time Optimization
The Linux Fastboot Capability
Building a Smaller Linux
Building a Smaller Application
Filesystem Tips and Tricks
Some Notes on Library Usage
Performance Tool Assistance
Recording Commands and Performance
System Error Messages and Event Logging
Dynamic Probes
User Mode Linux and Virtualization

Course Schedule Day 4
Improving CPU Performance
Run Queue Statistics
Context Switches and Interrupts
CPU Utilization
Linux Performance Tools for CPU
Process-Specific CPU Performance Tools
Stupid Cache Tricks
Improving System Memory Performance
Memory Performance Statistics
Linux Performance Tools for Memory
Process-Specific Memory Performance Tools
More Stupid Cache Tricks
Improving I/O and Device Driver Performance
Disk, Flash and General File I/O
Improving Overall Performance Using the Compiler
Basic Compiler Optimizations
Architecture-Dependent and Independent Optimization
Code Modification Optimizations
Feedback Based Optimization
Application Resource Optimization
The Hazard of Trust
An Iterative Process for Optimization
Improving Development Efficiency
The Future of Linux Performance Tools
Some Final Recommendations

Decision (Run/Cancel) Date for this Courses is Friday, December, 30, 2016

Payment received by December 27
IEEE Members $395
Non-members $415

Payment received after December 27
IEEE Members $415
Non-members $435

http://ieeeboston.org/advanced-embedded-linux-optimization/

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

Embedded Linux Board Support Packages and Device Drivers

Date & Time: 6 - 9PM; Mondays, Nov. 28, Dec. 5, 12, 19

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the development of Embedded Linux Board Support Packages (BSPs), Device Drivers and Distributions. The first part of the course focuses on BSP and Software Development Kit (SDK) development in an Embedded Linux context with a focus on application performance measurement and improvement. The latter part of the course covers Embedded Linux Device Driver development including key device driver decisions and deployment considerations for Embedded Linux BSPs.

Who Should Attend - The course is designed for real-time engineers who are developing Embedded Linux BSPs and Device Drivers for Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Linux BSP and Device Driver development.

Course Objectives

- To gain an understanding of the complexities of BSP and SDK development and their uses in Embedded Linux systems.
- To provide a basic understanding of the Linux I/O Subsystem and the Device Driver Models provided with Embedded Linux distributions.
- To gain an in-depth understanding of character-based device drivers in Embedded Linux
- To understand key device driver subsystems including relatively slow I/O interconnects such as I2C, SPI and USB as well as high-speed interfaces such as USB 3.0 and PCIe
- To give students the confidence to apply these concepts to their next Embedded Linux project.

Course Schedule Day 1

Getting Started with Embedded Linux
Linux and the GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs
Linux References (Books and Online)

Embedded Linux BSP Development Basics
BSP Requirements
U-Boot and Bootloader Development
Basic BSP Development
Files and Filesystem Support
The I/O Subsystem: Talking to Hardware
Memory Management and Paging
Error Handling in Embedded Linux BSPs
Timing and Timers
Interrupt Handling in BSPs
BSP Deployment Issues and Practices

Embedded Linux SDK Basics
The 3 Pieces of an SDK
Embedded Linux Distributions
The GNU Compiler Collection (GCC)
Other Embedded Linux Development Tools
Library Support
Glibc and Alternatives
SDK Deployment and Support
Debugging
GDB, GDB Server and the GDB Server Debugger
Other Debug Tools
An Abatron Board Bring-Up Example
An Eclipse Remote Debug Example
Advanced Debug with printk, syslogd and LTTng

System-Level Debug
System-Level Debug Tools
The /proc Filesystem
Advanced Logging Methods
KGDB and KDB
Crash Dumps

Course Schedule Day 2

Configuring Embedded Linux
Config Methods
Config Syntax
Adding Code to the Linux Kernel

Booting Embedded Linux
The Linux Boot Process

Please take this short survey, https://www.surveymonkey.com/r/B8R2DYL

NFS and RAMdisk Booting
Root and Flash File System Development
Building the RAMdisk
Busybox Development
Testing and Debug of Embedded Linux BSPs
Kernel Debug and Kernel Probes
Kexec and Kdump
The Linux Test Project (LTP)
Performance Tuning Embedded Linux BSPs
User Mode Linux and Virtualization
Measuring Embedded Linux BSP Performance
Common Considerations
Uncommon Considerations
BootLoader Optimizations
Boot Time Measurements
Effective Memory and Flash Usage
Filesystem Performance Issues
Some Ideas on Performance Measurement

Course Schedule Day 3
The Original Device Driver Model
The fops struct and Char Drivers
The inode and dentry structs
Major and Minor Numbers
Embedding Channel Information
Deferring Work
The /proc Filesystem

Configuring the Device Driver
Modularization Revisited
The New Device Driver Model
An Object-Oriented Approach
Platform Devices and Drivers
Subsystem Registration
The Probe and Init Functions
The Show and Store Functions
The /sys Filesystem
Configuring the New Device Driver
Comparing the Two Driver Models
The Flattened Device Tree (FDT)
openBoot and its Effect on Embedded Linux
The Device Tree Script (dts) File
The Device Tree Compiler (dtc)
The Device Tree Blob (dtb) File
Building a dtb File
Hybrid Device Drivers
Other fops Functions
The Need for Ioctl
A Simulated Char Device Driver
The SIM Device Driver
Initialization
Open and Close
Read and Write
The /proc Driver Interface
MMAP Support

Course Schedule Day 4
Linux Device Driver Subsystems
Serial Drivers
The RTC Subsystem
Watchdogs
I2C & SPI
Block Devices
PCI
USB
VME
Video
Sound
What's Missing?
Memory Technology Devices
What is an MTD?
NAND vs NOR Flash Interfaces
The Common Flash Interface (CFI)
Driver and User Modules
Flash Filesystems
Drivers in User Space
Accessing I/O Regions
Accessing Memory Regions
User Mode SCSI, USB and I2C
UIO
High-Speed Interconnects
PCIe
GigE
iSCSI
Infiniband
FibreChannel
Serial RapidIO
Debugging Device Drivers
kdb, kgdb and JTAG
Kernel Probes
Kexec and Kdump
Kernel Profiling
User Mode Linux and Kernel Hacking
Performance Tuning Device Drivers
Some Final Recommendations

Decision (Run/Cancel) Date for this Courses is Friday, November 18 2016

Payment received by November 15
IEEE Members $395
Non-members $415

Payment received after November 15
IEEE Members $415
Non-members $435

http://ieeeboston.org/embedded-linux-bsp-device-drivers/

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Attention: RF, Microwave, & High-Speed Digital Designers

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2016

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IEEE MIT Call for Submissions

Submission Deadline: September 3rd, 2016

Meet Innovation Technology

Sponsored by MIT IEEE Student Branch and IEEE Boston Section

MIT IEEE Student Branch believes a technical conference is needed for all the undergraduate students globally. They inaugurated the IEEE MIT Undergraduate Research Technology Conference last year, and will organize it again for this year. MIT will be the venue where the undergraduate students can meet to present, discuss, and develop solutions to advance technology for humanity. Participants can attend a rich program with renowned speakers, technical sessions, student design competition, exhibits, networking and social activities. It is a great opportunity for students to interact with the industry experts.

The conference theme is "Meet Innovation Technology (MIT)", and the four focus technical tracks are:

1. Big Data, Cloud Computing, Cybersecurity
2. Life Sciences, Biomedical Engineering and Technology
3. Robotics and Automation Technology
4. Communications for All Things
5. Wearable Technology
6. Innovative Technologies X-Track

Authors may submit content in the form of a technical paper, poster, or lightning talk.

All submissions must be written in English. Paper submissions must not be longer than 4 pages. Minimum font is 10 point, single-spaced, and submissions may include figures, illustrations, and graphs. Abstract submission for poster and lightning talk will be limited to 500 words.

All submissions will be peers reviewed. Notification of acceptance or rejection will be sent via email.

Submission will be online, and deadline is September 3rd, 2016. Notification of acceptance by September 24, 2016.

Please join the mailing list (MIT-Conference@ieee.org) for more information on the submission, technical program, registration, and accommodation.

Conference Proceeding of all the accepted papers that have been presented at the conference may be published, and included in the IEEE Xplore. Electronic media and online containing all accepted submissions will be distributed to the registered attendees.

For any inquiries, please email either the conference co-chair: - Alice Zhan (tzhan@mit.edu) or Helen Zhou (hlzhou@mit.edu).

http://ieee.scripts.mit.edu/conference

Massachusetts Institute of Technology

IEEE BOSTON SECTION

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Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is http://ieeeboston.org/course-proposals/ . Alternatively, you may contact the IEEE Boston Section office at sec.boston@ieee.org or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

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Note New Submission Schedule

Call for Papers, Posters & Tutorials

The 16th annual IEEE Symposium on Technologies for Homeland Security (HST '17), will be held 25-26 April 2017, in the Greater Boston, Massachusetts area. This symposium brings together innovators from leading academic, industry, business, Homeland Security Centers of Excellence, and government programs to provide a forum to discuss ideas, concepts, and experimental results.

Produced by IEEE with technical support from DHS S&T, IEEE, IEEE Boston Section, and IEEE-USA and organizational support from MIT Lincoln Laboratory, Raytheon, Battelle, and MITRE, this year's event will once again showcase selected technical paper and posters highlighting emerging technologies in the areas of:

- **Cyber Security**
- **Biometrics & Forensics**
- **Land and Maritime Border Security**
- **Disaster and Attack Preparedness, Mitigation, Recovery, and Response**

We are currently seeking technical paper, poster and tutorial session submissions in each of the areas noted above. Papers examining the feasibility of transition to practice will also be considered. Submissions should focus on technologies with applications available for implementation within about five years. All areas will cover the following common topics:

- Strategy and threat characterization, CONOPs, risk analysis,
- Modeling, simulation, experimentation, and exercises & training, and
- Testbeds, standards, performance and evaluations.

Contact Information

For more detailed information on the Call for Papers, Posters & Tutorials, as well as Sponsorship and Exhibit Opportunities, visit the website http://ieee-hst.org/ or email: information@ieee-hst.org. Submissions should be made at the following website: https://cmt3.research.microsoft.com/HST2017/

Important Dates

Paper Abstract Deadline:	October 17, 2016
Paper, Poster and Tutorial Acceptance Notification	December 1, 2016
Final Paper Submission Deadline:	March 1, 2017

All deadlines are by midnight Eastern Time.

Organizing Committee

General Chair:	James Flavin, MIT Lincoln Laboratory
Deputy Chair:	Fausto Molinet, Matrix Internationale
Technical Chair:	Gerald Larocque MIT Lincoln Laboratory
Tutorials Chair:	Anthony Serino, Raytheon
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2016 IEEE High Performance Extreme Computing Conference

(HPEC '16)

Twentieth Annual HPEC Conference

13 - 15 September 2016

Westin Hotel, Waltham, MA

www.ieee-hpec.org

IEEE Advancing Technology for Humanity

IEEE HPEC High Performance Extreme Computing

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About the Conference

HPEC is the largest computing conference in New England and is the premier conference in the world on the convergence of High Performance and Embedded Computing. We are passionate about performance. Our community is interested in computing hardware, software, systems and applications where performance matters. We welcome experts and people who are new to the field.

Keynote Speaker

- Mr. David Martinez (HPEC Founder; IEEE Fellow; MIT Lincoln Laboratory Associate Head Cyber Security & Information Sciences Division) - HPEC: The Past, Present and Future Outlook

Invited Speakers

- Prof. Gilbert Strang (National Academy of Sciences; SIAM Fellow; MIT Mathematics Department) - Finding the Important Part of a Matrix or Graph
- Mr. Trung Tran (DARPA MTO - Program Manager) - Machine Learning, Data Analytics, and Non-Conventional Computer Architecture
- Dr. Jennifer Roberts (DARPA I20 - Program Manager) - The Future of Scalable Analytics and Machine Learning
- Mr. Robert Bond (MIT Lincoln Laboratory Associate Head ISR Systems & Technology Division) - Future DoD Computing and the Emergence of Autonomous Systems
- Prof. Aleksander Madry (MIT Computer Science & AI Laboratory) - Linear-Algebraic Methods in Algorithmic Graph Theory
- Prof. Orran Krieger (Boston University Cloud Computing Initiative) - The Massachusetts Open Cloud: Vision and Early Experiences
- Prof. Martin Herbordt (Boston University Electrical & Computer Engineering Department) - TBD
- Prof. Viktor Prasanna (USC Charles Lee Powell Chair in Engineering) - TBD
- Prof. Nir Shavit (MIT Computer Science & AI Laboratory) - High Throughput Connectomics: The Building of a Brain-Scope
- Dr. Robert Cunningham (Chair IEEE Cybersecurity Initiative; MIT Lincoln Laboratory Group Leader Secure Resilient Systems & Technology) - End-to-End Security in the Cloud
- Dr. Igor Linkov (U.S. Army Corps of Engineers) - Cyber/Physical Resilience
- Mr. Clair Grant (Director of R&D VMS Software, Inc) - OpenVMS: 40 Years of Mission Critical Computing

Special Events

- BigDAWG Big Data Working Group; organizers: Dr. Tim Mattson (Principal Engineer - Intel) & Dr. Vijay Gadepally (MIT Lincoln Laboratory Supercomputing Center)
- GraphBLAS forum to define standard building blocks for graph algorithms; organizers: Prof. John Gilbert (SIAM Fellow; UC Santa Barbara) & Dr. Scott McMillan (CMU Software Engineering Institute)
- Massachusetts High Performance Computing; organizers: Dr. Chris Hill (Principal Research Engineer - MIT) & Prof. Patrick Dreher (North Carolina State)
- Vector, Signal, and Image Processing Libary (VSIPL) standard working group; organizer: Prof. Tony Skjellum (Director - Auburn University Cyber Research Center)
- Tools for Quantum Computing; organizers: Mr. Steve Reinhardt (D-Wave Systems) & Dr. John Cortese (MIT Lincoln Laboratory)
- Secure and Resilient Computing; organizers: Dr. Michael Vai (MIT Lincoln Laboratory Secure Resilient Systems & Technology) & Dr. George Kalb (JHU Information Security Institute)
- RISC-V; organizer: Mr. Kurt Keville (MIT ISN)

Tutorials

- Securing Your Embedded Systems for Cyberspace; instructors: Dr. Michael Vai, Dr. Roger Khazan & Mr. Benjamin Nahill (MIT Lincoln Laboratory Secure Resilient Systems & Technology)
- OpenMP programming; Dr. Tim Mattson (Principal Engineer - Intel)
- Mathematics of Big Data: Spreadsheets, Databases, Matrices, and Graphs; organizer: Dr. Jeremy Kepner (MIT Lincoln Laboratory Supercomputing Center)

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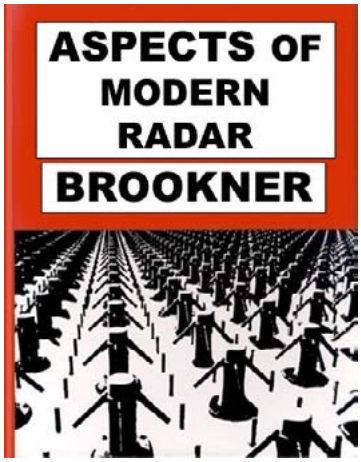
Radar Basics and Amazing Recent Advances

Time & Dates : **6:00 - 9:00 PM, Mondays, Oct. 24, 31, Nov. 7, 14, 21, 28, Dec. 5, 12, 19 2016, Jan. 9, 2017 (If needed, Snow/make up days Jan. 23, 30, Feb. 6)**

Location: **MITRE Corporation, 202 Bedford Rd., Burlington (tentative)**

Speaker: **Dr. Eli Brookner, Raytheon Company (Retired)**

The following book plus over ten paper reprints are provided FREE with your registration:



1. "Aspects of Modern Radar", Dr. Eli Brookner (Editor), Artech House, Hardcover, 432 pages, 1988, List price: $159. The 1st chapter gives the best easy to read introduction to radar. It covers all aspects of radar: transmitters, receiver, antennas, signal processing, tracking, clutter derivation of radar equation in easy terms and definition of dB. The 2nd chapter gives detailed descriptions of different radar systems like: Cobra Dane, Pave Paws, BMEWS, Series 320 3D radar, OTH radars and dome antenna. The book has a catalog giving the detailed parameters for over 200 radars from around the world. The remaining chapters cover AEGIS SPY-1, Hybrid and MMIC circuits, ultra low sidelobe antennas (ULSA), mmw, radar cross section and Doppler weather radars. The material in the book is easy to access and as a result the text serves as a handy reference book.

This course is an updated version of the Radar Technology course given previously. Those who have taken the Radar Technology previously should find it worthwhile taking this revised version. New material includes latest on solid state devices and transmitters including GaN, SiC, SiGe; Breakthroughs in Radar — $10 T/R module, Digital Beam Forming (DBF), Packaging, Disruptive Technology, Metamaterials, radar on a chip, 32 element phased array on a chip, Memristors, Graphene. Also covered are radar height-range coverage diagram using the powerful SPAWAR's AREPS program. AREPS provides coverage for arbitrary propagation conditions (ducts [evaporation, surface, or elevated], subrefraction and superrefraction) and terrain conditions based on DTED map data. AREPS now accounts for surface roughness scattering and evaluates sea and land clutter backscatter versus range. Attendees will be told how to obtain AREPS FREE. Valued at over $7,000. Also new is coverage of Anomalous Propagation and what to do about it. Finally also covered is the new Multiple-Input Multiple-Output (MIMO) explained in simple physical terms.

Updated course is framed around FREE book described above. Also given ot free are supplementary notes consisting of copies of >800 vugraphs plus over 15 paper reprints by Dr. Brookner.

For the beginner, basics such as the radar equation, MTI (Moving Target Indicator), pulse doppler processing, antenna-scanning techniques, pulse compression, CFAR, RAC and SAW devices, dome antenna, CCDs, BBDs, SAW, SAW monolithic convolvers, microstrip antennas, ultra-low antenna sidelobes (<-40 dB), stacked beam and phased array systems, (1-D, 2-D, Limited Field of

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View [LFOV]), Moving Target Detection (MTD) are all explained in simple terms. For both the novice and experienced covered are tracking, prediction and smoothing in simple terms (mystery taken out of GH, GHK and Kalman filters); the latest developments and future trend in solid state, tube and digital processing technologies; synthetic aperture radar (SAR); Displaced Phase Center Antenna (DPCA); Space-Time Adaptive Processing (STAP) ; digital beam forming (DBF); Adaptive-Adaptive Array Processing for jammer suppression with orders of magnitude reduction in computation; RECENT AMAZING RADAR BREAKTHROUGHS.

Lecture 1, Oct. 24

FUNDAMENTALS OF Radar: Part 1: Very brief history of radar, major achievements since WWII: PHASED ARRAYS: Principles explained with COBRA DANE used as example. Near and Far Field Defined, Phased Steering, Time Delay Steering,

(G.KLARI,, ET AL, "SINGLE CHIP MM RADAR", MICROWAVE J., 1-14-15;
R. J. Evans et al., "Consumer Radar," *Int. Radar Conf.*,Adelaide, 9/2013, pp. 21–26)

Subarraying, Array Weighting, Monopulse, Duplexing, Array Thinning, embedded element, COBRA DANE slide tour (6 stories building). Radar equation derived.

Lecture 2, Oct. 31

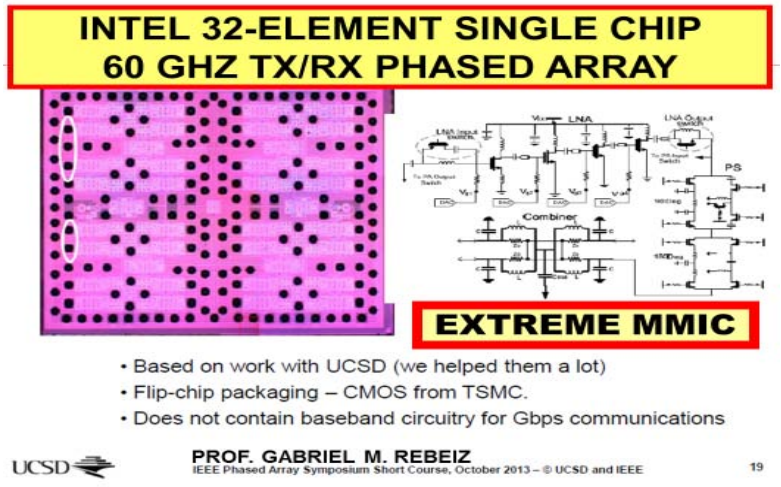
FUNDAMENTALS OF Radar: Part 2: FREQUENCY TRADEOFFS: Search vs Track, Range and Doppler Ambiguities, Detection in Clutter. Blind

http://spendergast.blogspot.com/2016/05/googles-project-soli-demos-mmw-micro.html
http://www.theverge.com/2016/5/20/11720876/google-soli-smart-watch-radar-atap-io-2016

Velocity region, range eclipsing, Environmental Factors, Dependence of clutter model on grazing angle and size radar resolution cell discussed, Weibull clutter: Polarization Choice, Detection of Low Flying Low Cross-Section Targets, Antenna Pattern Lobing in Elevation due to multipath, Ground Multipath Elevation Angle Error Problem and ways to cope with it, e.g., use of an even difference pattern Off-Axis Monopulse, Complex Monopulse,Two Frequency Radar Systems: Marconi L- and S-band S631, Signaal/Thales (Holland),Flycatcher X and Ka System; Tube and Solid State OTH. Radars

Lecture 3, Nov. 7

FUNDAMENTALS of Radar: Part 3: PROPAGATION: standard, superrefraction, subrefraction, sur-



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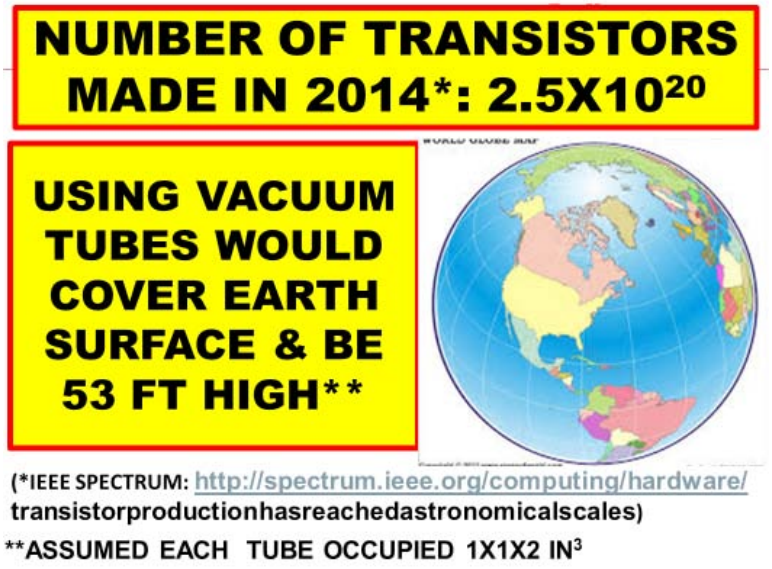
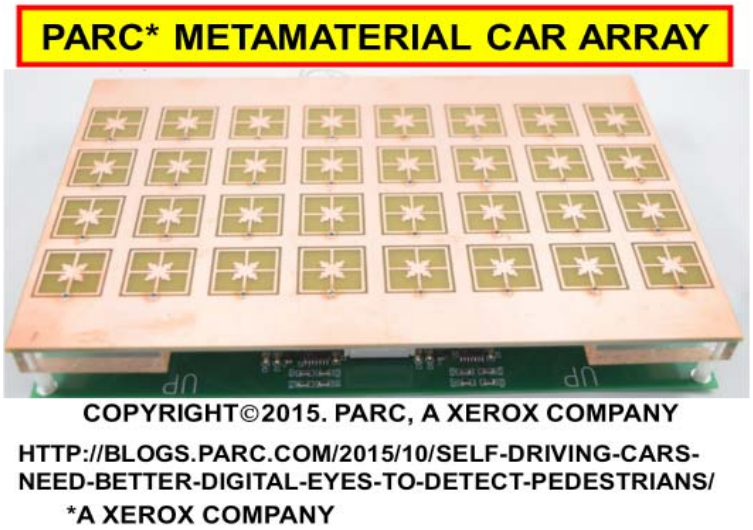
face-based ducts, evaporation ducts. Determination of radar coverage using new AREPS program. ANTENNA SCANNING SYSTEMS: Fixed Beam System: Wake Measurement Radar; 2-D Radars, 3-D Radars: Stacked Beam: Marconi Martello, Smart-L, SMARTELLO, ARSR-4; 1-D Frequency Scanning: ITT Series 320; 1-D Phased Scanning: TPS-59, GE-592, RAT-31DL; Phased-Frequency Scanners: Raytheon Fire Finder and Plessey AR320; Limited and Hemispherical Scanning (Dome Antenna) related and explained in simple terms.

Lecture 4, Nov. 14
FUNDAMENTALS of Radar: Part 4: ULTRA LOW ANTENNA SIDELOBES (40 dB down or more). MOVING TARGET INDICATORS (MTI): Two-Pulse Canceller, Pulse Doppler Processing; MOVING TARGET DETECTOR (MTD); Optimum Clutter Canceller, STAP, AMTI, DPCA.

Lecture 5, Nov. 21
SIGNAL PROCESSING: Part 1: What is PULSE COMPRESSION? Matched Filters; Chirp Waveform Defined; ANALOG PROCESSING: Surface Acoustic Wave (SAW) Devices: Reflective Array Compressor (RAC), Delay Lines, Bandpass Filters, Oscillators, Resonators; IMCON Devices; Analog Programmable Monolithic SAW Convolver; BBD/CCD. What are they?

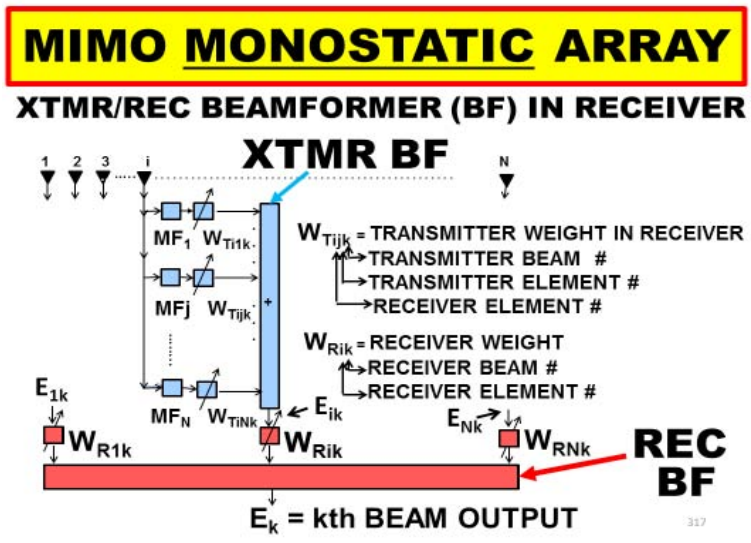


Lecture 6, Nov. 28
SIGNAL PROCESSING: Part 2: DIGITAL PROCESSING: Fast Fourier Transform (FFT); Butterfly, Pipeline and In-Place Computation explaine



in simple terms; Maximum Entropy Method (MEM) Spectral Estimate; State-of-the-art of A/Ds, FPGAs and Memory; Signal Processor Architectures: Pipeline FFT, Distributed, Systolic; Digital Beam Forming (DBF). Future Trends.

Lecture 7, Dec. 5
SYNTHETIC APERTURE RADAR (SAR): Strip and Spotlight SAR explained in simple terms. TUBES: Basics given of Magnetron, Cross Field



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Amplifiers, Klystrons, Traveling Wave Tubes, Gyro Tubes.
TREND TOWARD SOLID STATE PHASED-ARRAY TRANSMITTERS: Discrete All Solid State PAVE PAWS and BMEWS radars; advantages over tube radars; MMIC (Monolithic Microwave Integrated Circuitry; integrated circuitry applied to microwaves components): THAAD, SPY-3, IRIDIUM, XBR, JLENS. Solid State 'Bottle' Transmitters: ASR -11/DASR, ASR-23SS, ASDE-X. Extreme MMIC.

Lecture 8, Dec. 12
Breakthroughs and Trends in Phased-Arrays and Radars
Systems: 3, 4, 6 face "Aegis" systems developed by China, Japan, Australia, Netherlands, USA; Patriot now has GaN AESA providing 360o coverage without having to rotate; S/X-band AMDR provides 30 times the sensitivity and number of tracks as SPY-1D(V). Low Cost Packaging: Raytheon funding development of low cost flat panel X-band array using COTS type printed circuit boards (PCBs); Lincoln-Lab./MA-COM developing low cost S-band flat panel array using PCBs, overlapped subarrays and a T/R switch instead of a circulator; Extreme MMIC: 4 T/R modules on single chip at X-band costing ~$10 per T/R module ; full phased array on wafer at 110 GHz; on-chip built-in-self-test (BIST); Digital Beam Forming (DBF): Israel, Thales and Australia AESAs have an A/D for every element channel; Raytheon developing mixer-less direct RF A/D having >400 MHz instantaneous bandwidth, reconfigurable between S and X-band; Lincoln Lab increases spurious free dynamic range of receiver plus A/D by 40 dB; Radio Astronomers looking at using arrays with DBF. Materials: GaN can now put 5X to 10X the power of GaAs in same footprint, 38% less costly, 100 million hr MTBF; SiGe for backend, GaN for front end of T/R module. Metamaterials: Material custom man made (not found in nature): electronically steered antenna at 20 and 30 GHz demonstrated (with goal of $1K per antenna) remains to prove low cost and reliability); 2-20GHz stealthing by absorption simulated using <1 mm coating; target made invisible over 50% bandwidth at L-band; Focus 6X beyond diffraction limit at 0.38 μm; 40X diffraction limit, λ/80, at 375 MHz; In cell phones provides antennas 5X smaller (1/10th λ) having 700 MHz-2.7 GHz bandwidth; Provides isolation between antennas having 2.5 cm separation equivalent to 1m separation; used for phased array WAIM; n-doped graphene has negative index of refraction, first such material found in nature. Very Low Cost Systems: Valeo Raytheon (now Valeo Radar) developed low cost, $100s, car 25 GHz 7 beam phased array radar; about 2 million sold already, more than all the radars ever built up to a very few years ago; Commercial ultra low cost 77 GHz Roach radar on 72mm2 chip, uses >8 bits 1 GS/s A/D and 16 element array; Low cost 240GHz 4.2x3.2x0.15 cm3 5 gm radar for bird inspired robots and crawler robots, Frequency scans 2ox8o beam ±25o. SAR/ISAR: Principal Components of matrix formed from prominent scatterers track history used to determine target unknown motion and thus compensate for it to provide focused ISAR image. Technology and Algorithms: Lincoln Lab increases spurious free dynamic range of receiver plus A/D by 40 dB; MEMS: reliability reaches 300 billion cycles without failure; Has potential to reduce the T/R module count in an array by a factor of 2 to 4; Provides microwave filters like 200 MHz wide tuneable from 8-12 GHz; MEMS Piezoelec-

tric Material = piezoMEMS: Enables flying insect robots; Printed Electronics: Low cost printing of RF and digital circuits using metal-insulator-metal (MIM) diodes, 2D MoS2 ink and 1.6 diodes GHz (goal 2.4 GHz) made with Si and NbSi2 particles,; Electrical and Optical Signals on Same Chip: Electricity and light can be simultaneously transmitted over a silver nanowire combined with single layer 2D MoS2, could be a step towards transporting on computer chips digital information at the speed of light; COSMOS: DARPA revolutionary program: Allow integration of III-V, CMOS and opto-electronics on one chip without bonded wires leading to higher performance, lower power, smaller size, components; MIMO (Multiple Input Multiple Output): Where it makes sense; contrary to what is claimed MIMO array radars do not provide 1, 2 or 3 orders of magnitude better resolution and accuracy than conventional array radars; MIMO does not provide better barrage-noise-jammer, repeater-jammer or hot-clutter rejection than conventional array radars; should not be better for detecting low velocity targets in airborne STAP radar; Graphene and Carbon Nanotube (CNT): Potential for Terahertz transistor clock speeds, manufacture on CMOS demo'd, could allow Moore's law to march forward using present day manufacturing techniques; potential for non-volatile memory, flexible displays and camouflage clothing, self-cooling, IBM producing 200 mm wafers with RF devices; Electron spin: For memory; Atomic Memory: 12 iron atoms for 1 bit of memory; could provide hard drive with 100X density; Revolutionary 3-D Micromachining: integrated circuitry for microwave components, like 16 element Ka-band array with Butler beamformer on 13X2 cm2 chip; Superconductivity: We may still achieve superconductivity at room temperature; Superconductivity recently obtained for first time with iron compounds; DARPA UHPC (Ubiquitous High Performance Computing) Program): Goal: Reduce signal processing power consumption by factor of 75; Biodegradable Array of Transistors or LEDs: Imbedded for detecting cancer or low glucose; can then dispense chemotherapy or insulin; Quantum Radar: See stealth targets; New polarizations: OAMs, (Orbital Angular Momentum) unlimited data rate over finite band using new polarizati ons??

Lecture 9, Dec. 19

TRACKING, PREDICTION AND SMOOTHING: Simple Algebra and Physical explanation. Mystery taken out of αβ (GH) Filter; Errors of; Fading Memory; Benedict-Bordner; Example Designs; Stability; Tracking Initiation; αβγ (GHK) Filter; Kalman Filter Explained in simple physical terms; Why Kalman Filter?; Relationship to GH and GHK Filters; Matrix Notation; Simple Derivation.

Lecture 10, Jan. 9

HOW TO LOOK LIKE A GENIUS IN DETECTION WITHOUT REALLY TRYING: Simple procedure for determining detection using Meyer Plots, MATLAB, Excel and MATHCAD is presented. No detailed mathematics used, emphasis on physical understanding of target models (non-fluctuating, Marcum, Swerling, Weinstock, Chi-Square, Rayleigh, Lognormal, Rice and YGIAGAM) and performance results. Also covered are beam shape, CFAR, mismatch losses.

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