BOSTON

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IEEE Boston Section Online Courses:

Verilog101:Verilog Foundations CLASS DESCRIPTION: Verilog is IEEE standard 1364. It is a Hardware Description Language that is the corner stone of much of the simulation world. Verilog Foundations is a comprehensive introduction to the IEEE 1364 (Verilog). The Verilog Foundations class has a slightly different approach to learning Verilog than other methods. There is a lecture section for each main topic. This presents a basic foundation for the language. What makes Verilog Foundations exciting is the emphasis on labs/examples. There are nearly 100 labs/examples giving comprehensive "how to" examples of most Verilog language constructs. There are working solutions for each lab and the students can use the lab database for developing their own models later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace.
(Register at http://www.ieeeboston.org) and click on course title

System Verilog 101: Design Constructs CLASS DESCRIPTION: SytemVerilog is an extensive set of language constructs to the IEEE 1364-2001 standard. It's meant to aid in the creation and verification of models. There are two parts to the language extension. The first part covered by this class, is new design constructs. The second part of SystemVerilog is verification constructs, covered by SystemVerilog102. There are over 100 labs/examples giving comprehensive "how to" examples of most SystemVerilog language constructs. There are working solutions for each lab and the students can use the lab database for developing their own models later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace. There are self-grading quizzes for each chapter that allow the student to see if he/she is learning the material. The goals of this course are to make you familiar with the new part of the language. Students taking SystremVerilog101 will have a 90-day access to it. The lab database you will be able to download and is yours to keep. **(Register at http://www.ieeeboston.org) and click on course title**

System Verilog 102: Verification Constructs CLASS DESCRIPTION:SytemVerilog is an extensive set of language constructs to the IEEE 1364-2001 standard. It's meant to aid in the creation and verification of models. There are two parts to the language extension. The first part covered by SV101, is new design constructs. SV102, this class, covers verification constructs. SystemVerilog102, like all CBE classes, is lab based. There are over 30 verification labs/examples giving comprehensive "how to" examples of most SystemVerilog verification language constructs. There are working solutions for each lab and the students can use the lab database for developing their own assertions later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace. **(Register at http://www.ieeeboston.org) and click on course title**

Introduction to Embedded Linux Part I CLASS DESCRIPTION: This first of a 2-part series introduces the Linux Operating System and the use of Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part covers the methods for booting Embedded Linux distributions including embedded cross-development and target board considerations.

High Performance Project Managment CLASS DESCRIPTION: This12 hour course(broken into short 10 to 20 minute independent modules) provides the project methodology, concepts, and techniques that ensure successful completion (on time, on budget, with the quality required) of projects, large and small. Participants learn the steps to take before, during, and at the end of a project to hone planning and execution to a strategically built process that delivers project success when used. Additionally, the course provides the interpersonal and leadership techniques to ensure everyone involved with the project whether a team member, organization member, or outside of the organization commits to the success of the project—voluntarily—and provides the support and assistance to ensure its success. In addition to learning how to master the technical skills that have evolved over thousands of years of project implementation and practice, the course provides the advanced team building, leadership, and interpersonal skills that ensure the technical skills can be used, they way they are designed to be used, resulting in a process that delivers the on time, on or under budget, with the quality required completed project consistently.

Who wants to be an Engineer?

Karen Panetta, Reflector Editor

I met with my department chair for a cup of coffee to talk. He needed to discuss something with me and promised we wouldn't be discussing anything bad. When we met, he asked me to teach the circuit theory course. My response was, "I thought you said we wouldn't be talking about anything bad?"

In case you didn't know, circuit theory is the number one reason students leave, actually run, from the electrical engineering major. It is considered the plague for most U.S. engineering institutions.

Upon informing my husband that I would be teaching this course, I returned home to find he bought me a beautiful shirt embossed with a sequined lighting bolt with the word "BOOM" written below it. This is what I call a sympathy gift, with a sense of humor.

I received many other condolences from friends and colleagues when they heard my news. They shared their circuit theory memories, or should I say horror stories. They even cited that it was a good thing computer science programs did not exist when they were in school, or they too would have fled electrical engineering and changed majors.

I decided to investigate why this course is considered the scourge of the earth for engineers. Moreover, why did all of us stay in Electrical Engineering, if we were tortured so badly by this course?

Students say, "I don't want to solder for the rest of my life", or "I don't care about how to turn on a light bulb." Obviously, their view is very limited, but whose fault is it if this is the way they think after taking a circuit theory course?

I try to explain to them that they are learning fundamentals and that I don't know a single engineer that solders all day. They nod in agreement and then continue to hand me a form requiring my signature allowing them to drop the course, despite my best reassurances.

I could tell them they would be millionaires if they would stay in Electrical Engineering, but not even money sways them. My dad used this line on me to make me go into Electrical Engineering, but today's kids are much smarter than when I was in school. Back then, we thought our parents knew more than we did, and we actually listened to their advice.

My colleagues also condemned to teach this course, try to ease my pain by offering me their notes and labs. It is a nice gesture, but turning on light bulbs doesn't turn me on either. I am with the students on this one. I have to bite the bullet and tame this beast myself.

Now, if we are talking about controlling airport runway lighting during all weather conditions, I am more interested. If we are talking about using sound

signals to diagnose oncoming mechanical failures in helicopter gearboxes or to do audio forensics, I am all ears.

Ah ha! The light bulb is going on now. Students hate circuit theory because they don't see how any of it is useful or where it is used.

I told this to one of my seasoned colleagues.
His response was, "Who said Electrical Engineering had to be easy, fun or enjoyable?" I interpreted this to be the equivalent of saying, "let them eat cake."

Telling students to wait a few years to see how it all comes together in their academic career is like telling your kid, "some day you will thank me for punishing you." It just doesn't sell.

Our nation suffers from a horrendous shortage of young people pursuing engineering. If we don't change our recruitment efforts and public awareness to show the impact engineers have on humanity, then we will never overcome this sad reality.

One of the most successful ways to do this is to have role models. We need role models who show us the "big picture", lead by example and the best part is that to be a role model doesn't mean the person has to be dead!

IEEE Boston is very proud that we have many wonderful role models among us.

There are many more of you out there that are great role models and we need you! With your help, those of us in the trenches of education may be able to find more exciting ways to make topics like voltage division cool.

As always, the views expressed in our editorials are those of the author and not necessarily those of the IEEE Boston Section

Letters to the editor can be sent to, ieeebostonsection@gmail.com

Communications Society – 7:00PM, Thursday, 2 February

Fixed Wireless for Broadband Access

Fred Goldstein, Interisle Consulting Group

While mobile radio technology and short-range WLANs and PANs get most of the attention, the fixed wireless industry has seen very rapid evolution recently, going through several generations over the past 15 years. Broadband wireless access systems operate on several bands, primarily unlicensed, between 470 MHz and 64 GHz, and typically allow point-to-multipoint access at subscriber speeds in the 10 to 25 Mbps range. Advancements in MIMO and beam-steering technology promise greater spectrum efficiency, while costs continue to decline, making this a more economical choice than fiber optics for a growing share of the market, largely rural but increasingly urban.

Fred Goldstein is a Principal of the Interisle Consulting Group, where he advises public and private sector entities on technical, regulatory and business issues related to the telecommunications, cable, wireless and Internet industries, especially in areas where they overlap. He has provided regulators with expertise on technical convergence issues, such as non-video services provided across cable, and serves as FCC Consultant to the Wireless ISP Association. He has helped numerous CLECs navigate the startup process, helping them deal simultaneously with technical, regulatory and business issues. He assists service providers in network design, business modeling, planning, and technical architecture. He has frequently been an expert witness in regulatory matters, and in intercarrier compensation and network interconnection cases. He has worked with enterprise networks on a wide range of matters such as backbone network design, voice systems planning, and traffic engineering.

Please circulate to interested parties.

Venue Note: This is our venue at the new Verizon Technology Center Campus in Waltham.

The meeting begins at 7 PM at the new meeting auditorium at the Verizon Technology Center. The address is 60 Sylvan Road, Waltham, MA 02451. The entrance is by the far corner – with the picnic tables out front – and not the tower or the new building. It is most easily reached by the West Street entrance. ***Important Note:*** *Verizon Technology Center requests the names of the meeting attendees* ***in advance of the meeting****. If you plan to attend, please send a note via e-mail with your name to John Nitzke at RF@ieee.org by Wednesday, February 1st*

The meeting is preceded by dinner at Bertucci's, 475 Winter St, Waltham at 5:30 PM. The speaker will be joining us at dinner.

Directions to Bertucci's restaurant in Waltham: Take Exit 27B on I95/128, heading west on Winter Street. After exiting, stay all the way to the right and take the first right turn into the shopping plaza. Please let Bob Malupin know if you plan to attend the dinner at Bertucci's. Bob can be contacted at Robert.Malupin@VerizonWireless.com .

Directions to Verizon Technology Center (old Verizon Labs location), 60 Sylvan Rd. campus, Waltham, MA 02451: Take Exit 27B on I95/128, heading west on Winter Street. Stay all the way to the right. Verizon Technology Center is 1/2 mile ahead. At the second traffic light, turn left onto WEST ST. and then take the first right (at the Verizon sign) which leads into the Verizon campus. Take the first left. The building and entrance for the meeting are on your right. Note that the entrance to the auditorium area is by the far corner – with the picnic tables out front – and not the tower or the new building.

To assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

Entrepreneurs' Network Boston Meeting - 6:30PM, Tuesday, 7 February

Winning Investors With Your Pitch Deck And Presentation

Meeting location – Constant Contact, 1601 Trapelo Rd., 3rd Floor Great Room, Waltham, MA (Exit 28, I-95/Route 128)

PRE-MEETING DINNER at 5:15 PM (sharp) at Bertucci's, Waltham, MA (Exit 27, I-95/Route 128) . One of the most obvious and challenging key requirements for the success of an early stage entrepreneurial company is securing funding. Our Boston ENET June 7th meeting is focused on learning how to win potential investors with the right pitch deck and presentation. It will also focus on how companies can build a value proposition which will enable an entrepreneur to raise value, a critical step prior to raising money.

The Panel is composed of several venture capitalists, some who have been in successful startups prior to their investment careers and a CEO who has led several successful start-ups, is an author, currently works with early stage companies as an adviser and who has developed webinars and a work shop to guide early stage company executives to success.

Join us for an exciting and informative evening of informative presentations and networking.

Speaker: Barbara Finer, CEO, TechSandBox, has founded several technology companies. She has served on the Board of MIT Enterprise Forum, WPI Venture Forum, and Choices Wellness Center and has judged and/or mentored at Ignite/CTO, FIRST, and MassChallenge. Her professional areas of expertise include Marketing, Business Development, Entrepreneurship and Leadership. Barbara can be found teaching Marketing, Business and Entrepreneurship at local colleges. She holds a BS from Northeastern University and a MSA in Management of Innovation and Technology from Boston University.
See https://www.linkedin.com/in/barbfiner and http://www.techsandbox.org/ .

Speaker: Brad Kayton is a serial entrepreneur, with 8 startups, and an emerging fund manager. He is President of Studio Ventures, and General Partner and Screening Committee Member of Investors Collaborative, a new type of equity fund, part angel capital part hedge fund, and an original member of FP Angels in New York City. He is also COO and GM of 1World Online, which creates highly engaging polls, quizzes and surveys, on the mission to become the central resource on the Internet to find out what people really think on a variety of topics.
See https://www.linkedin.com/in/bradkayton and http://www.investorscollaborative.com/

Speaker and Co-Organizer: Johnny Monsarrat was founder and CEO of Turbine, which raised non-dilutive capital by getting a $3 million cash advance against royalties from Microsoft to publish their first game. The company was bought by Warner Brother for $160 million. He is now the CEO of Monsarrat, Inc., which is following Pokemon Go into the augmented reality mobile game market with a new twist. He is an Ivy League award-winning public speaker.

See http://linkedin.com/in/monsarrat and http://monsarrat.com/.

Moderator: Larry Grumer, Co-founder/CEO Energy Harvesters LLC, is developing a wearable device so users can charge their mobile device batteries anytime, anywhere – just by walking. He has partnered to launch 6 companies and a 30-person engineering consultancy. He has 25 years of P&L leadership with Textron, Arthur D. Little, Foster-Miller and start-ups. Larry was Chairman, Boston Entrepreneurs' Network, I-cubator Director, Northeastern University, a founding Board member North Shore Technology Council and created the EntreTech Forum. He has a BSME and MBA from Northeastern University. See http://www.energyharvesters.com/ and https://www.linkedin.com/in/lawrence-grumer-95125

Meeting Location: Constant Contact, 1601 Trapelo Rd., 1st Floor Great Room, Waltham, MA (Exit 28, I-95/Route 128).

Check for Updates: Boston Entrepreneurs' Network Website at (http://www.boston-enet.org)

Refreshments: Light refreshments, cookies, chips, cheese and soft drinks will be provided at the meeting.

PRE-MEETING DINNER at 5:15 PM (sharp) at Bertucci's, Waltham, MA (Exit 27, I-95/Route 128) . Pay as you go – separate checks.

Reservations: ENET meetings in Waltham are free to ENET members and $20 for non-members. To expedite sign-in for the meeting, we ask that everyone -- members as well as non-members -- pre-register for the meeting online. Pre-registration is available until midnight the day before the meeting. If you cannot pre-register, you are welcome to register at the door

Reliability Society and co-sponsored by NE-ESDA – 5:30PM, Wednesday, 8 February

ESD Concerns with Energetics & Explosives

Jay Skolnik, Certified ESD Program Manager

This presentation will be on ESD control for explosives and other energetic materials, introducing the attendees to the differences of ESD damage of electronics versus energetics. It will discuss the various energy levels and types of discharges which can cause catastrophic or latent failures. Enlightening demonstrations and case histories will be included to illustrate practical, real-life situations of past ESD-induced failures of energetic components and methods to prevent them, as well as explanations of the use of ESD mitigation in the work environment. The prevention of ESD failures be examined, as well as methods to safely work with explosive products while ensuring human safety, preventing catastrophic health hazards, injuries, and severe damages.

Jay Skolnik, PE, CPI, CPM, a Licensed Professional Electrical Engineer, is the co-founder and Lead Engineer / Consultant of Skolnik Technical Training in Albuquerque, NM. With over thirty years of experi-

ence in the electronics industry, Jay has developed a multitude of products utilized in different industries, including military, defense, avionics, aerospace, commercial, industrial, medical, automotive, and sports entertainment. As an ESDA Certified Program Manager, Jay teaches ESD mitigation and control for the electronics & energetics specialties. He performs ESD audits to ensure factories and laboratories are following safe ESD control guidelines and procedures. He is also certified by iNARTE and is a Certified Professional Instructor of National Instruments (NI). He received his Electrical Engineering degree from the University of Missouri-Rolla.

Email: engr@skolnik-tech.com

This meeting will be held on Wednesday, February 8, 2017 at 3 Forbes Road, Lexington, MA.

5:30-6:00 Sign In, Networking, Light Dinner & Refreshments

6:00-6:10 Chapter Chair Greetings & Announcements

6:10-7:30 Jay Skolnik, Certified ESD Program Manager

7:30-7:45 Q&A Session, Meeting Adjourns

To assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

Life Members – 4:00PM, Wednesday, 8 February

Little Issues with Big Data

Speaker: Jim Isaak, Past President IEEE Computer Society, 2016 VP IEEE Society on the Social Implications of Technology, 2003-4 IEEE Board of Directors, and retired from the Industry.

Big Data is one of the areas in computing that is just, well, getting bigger. However it exposes a number of issues that folks doing “Data Engineering” need to consider - from bit rot to legal issues like ownership, privacy, disclosure and liability. Presidential elections since 1960 have triggered big data driven investments. Consumer behavior is now tracked at the individual level, and tracking many more “data points” than you might anticipate. But Big Data is also a path towards environmental protection, detecting emergence of disease, and validating medical research.

Jim will provide some historical context that shines a light on recent, current and future issues facing corporations, software developers, but also managers, lawyers and the public in general.\

Jim is currently Blog mister for SSIT, Chair NH Life Member group, policy gadfly, and prescient skeptic. For additional background, visit www.JimIsaak.com.

The meeting will be held at the Lincoln Lab Auditorium, 244 Wood Street., Lexington, MA at 4:00 PM. Refreshments will be served at 3:30 PM. Registration is in the main lobby. Foreign national visitors to Lincoln Lab require visit requests. **Please pre-register by e-mail to reception@ll.mit.edu and indicate your citizenship.** Please use the Wood Street Gate. For directions go to http://www.ll.mit.edu/; for other information, contact Steve Teahan, Chairman, at (978)763-5136, or Steve.F.Teahan@raytheon.com

Meeting Location: Lincoln Lab Auditorium, 244 Wood Street, Lexington, MA 02421, USA

To assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

Photonics Society – 6:30PM, Thursday, 9 February

Nonlinearity-Tolerant Modulation Formats for Coherent Optical Fiber Communications

Dr. Keisuke Kojima, Mitsubishi Electric Research Laboratories (MERL), Cambridge, MA

Fiber nonlinearity is often the limiting factor in long distance optical fiber communications. Four-dimensional constant modulus modulation (i.e., the sum of x- and y-polarization power is constant) reduces the fiber nonlinearity effects significantly. In addition, high-dimensional modulation (>=4D) typically improves the signal to noise ratio characteristics. In this talk, we review our newly proposed 4D-2A8PSK format family which covers the range of 5-7 bits/symbol spectral efficiency and fills the gap of dual polarization (DP)-QPSK (4 bits/symbol) and DP-16QAM (8 bits/symbol) through sets of optical transmission simulations. We also show time-domain hybrid modulation using these 4D-2A8PSK formats to cover the whole 4-8 bits/symbol range. Discussions on practical implementations, as well as experimental results will be also presented.

Keisuke Kojima received the B.S., M.S., and Ph.D. degrees in electrical engineering all from the University of Tokyo, Tokyo, Japan. He also received the M.S. degree from the University of California, Berkeley. He worked for eight years at Mitsubishi Electric Corp., Japan, from 1983 on the research of narrow linewidth DFB lasers and grating-coupled surface-emitting DFB/DBR lasers. He spent nine years at AT&T/Lucent Bell Laboratories on the R&D of uncooled Fabry-Perot and DFB lasers, vertical-cavity surface-emitting lasers, and passive optical network systems.

He also worked at Agere Systems, Denselight Semiconductors, and TriQuint Semiconductors on optical devices and modules designs. He has been with Mitsubishi Electric Research Laboratories, Cambridge, MA, since 2005, where he is currently working on the research of coherent optical systems and photonic-integrated circuits as a Senior Principal Research Scientist. He has more than 170 publications in journals and conference proceedings. He is a Fellow of the Optical Society of America.

This meeting begins at 6:30 PM Thursday, February 9th, 2017 and will be located 3 Forbes Road (an MIT Lincoln Laboratory facility), Lexington, MA, 02420. The meeting is free and open to the public. All are welcome. Prior to the seminar there will be social time and networking from 6:30 – 7:00PM. Dinner will also be provided. The seminar will begin at 7:00PM. For more information contact Ajay Garg, Boston IEEE Photonics Society Chapter chair at ajay.garg@ll.mit.edu, or visit the Boston IEEE Photonics Society website at www.bostonphotonics.org.

Directions to Forbes Rd Lincoln Laboratory: (from interstate I-95/Route 128)

- Take Exit 30B onto Marrett Rd in Lexington – Merge into left lane
- Make the first Left onto Forbes Rd.
- Proceed straight through the small rotary and enter the parking lot.
- The entrance is on your right, by the flags.

To assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

Solid State Circuits Society – 12:00PM, Friday, 10 February

Approximate Hierarchical Sensing and Computing Towards Always-On Context-Awareness

Future mobile electronic devices will be equipped with more and more sensors that require always-on operation, to bring continuous context-awareness to the mobile device. Enabling this at near-zero-power budgets requires the device to exploit this context-information to at run-time tune its own performance and hardware configuration. Energy can dynamically be saved by continuously adapting sensing and processing circuitry to the observed operating context. This hardware context-awareness will be crucial in achieving the necessary 10x energy improvement for further miniaturization of wearables and mobiles.

Enabling such context-scalability at the hardware level requires combining research on always-on context sensing, embedded machine learning, and reconfigurable computing. This talk will zoom in on two important building blocks of the context-scalable system: 1.) Context-aware sensing through self-adaptive sensor interfaces. 2.) Context-aware computing through dynamically-scalable approximate computing.

Marian Verhelst (S'01-M'09-SM'14) is an assistant professor at the MICAS laboratories (MICroelectronics And Sensors) of the Electrical Engineering Department of KU Leuven as of 2012. Her research focuses on self-adaptive circuits and systems, embedded machine learning, and low-power sensing and processing for the internet-of-things. Before that, she received a PhD from KU Leuven cum ultima laude in 2008, was a visiting scholar at the Berkeley Wireless Research Center (BWRC) of UC Berkeley in the summer of 2005, and worked in the Radio Integration Research Lab of Intel Labs, Hillsboro OR from 2008 to 2011. Marian is a member of the Young Academy of Belgium, and has published over 100 papers in conferences and journals. She is a member of both the ISSCC and DATE TPCs and of the ISSCC and DATE executive committees. Marian was associate editor for TCAS-II and currently is for JSSC.

Meeting hosts: **Hosts:** Bruce Hecht, ADI, Rabia Tugce Yazicigil, MIT, Professor Anantha P. Chandrakasan, MIT

Meeting Location: 34-401 Grier Room, MIT, Cambridge. The program is free, but please register in advance by using the link below. **CLICK HERE TO REGISTER**

To assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

Entrepreneurs' Network – 6:00PM, Tuesday, 21, February

Licensing and Technology Transfer for Life Science and Tech Companies

Meeting Location – Pivotal Labs, 145 Broadway, 3rd Floor, Cambridge, MA

Are you an inventor or entrepreneur seeking to license technology from a university or a research establishment?

Are you a technology owner seeking to license it out to existing companies to gain revenue? Or to develop, commercialize and market your products and create a new start-up company?

On **21 Feb 2017**, the IEEE Boston Entrepreneurs' Network panel will address "Licensing and Technology Transfer for Life Science and Tech companies" from both sides.

Our speakers will offer both perspectives discussing licensing technology from Institutions and research establishments. What are typical and atypical terms? What and how to negotiate? At what stage of development can we attract seed investment? How do we assess the commercialization and marketability? What unmet needs are met and how bad is the "pain", i.e. maket size or a unique strategy? How to transition from the lab into viable and profitable products, i.e. "mind-to market" strategy? Typical terms and payment structures the entrepreneur or the Angel/Angel group, VC will seek in licensing will be discussed. What is royalty, fees and dividends? What are the license fees and milestones? What is the equity for the licensor? What are terms on sublicensing and royalty stacking?

Our speakers will also discuss licensing technology to a newly formed start-ups and early stage companies. They will also discuss licensing terms and offer insights – dos and don'ts – for entrepreneurs and start-up companies to successfully license technology from Institutions.

In addition, our speakers will also speak as a licensor, discussing how their institution/research establishment licenses out technology. Others discussions items will involve terms that a small or mid-size high tech company seek, as it licenses out its technology to generate revenue, as it acquires technology through cross-licensing, as it secures sources of supply, as it maximizes incentives to gain sales and market traction, and the implications of licensing on mergers and acquisitions.
Whether you are or want to be a technology licensor or licensee, there is much to learn from the experience of our speakers.

Brian J. Wainger, MD, PhD
Dr. Wainger is Assistant Professor in Anesthesiology and Neurology at Harvard Medical School and an attending physician at Massachusetts General Hospital. He studied molecular biology as an undergraduate at Princeton University and ion channel physiology in the MD/PhD program at Columbia University. He then completed medical residency in the Partners Neurology Program followed by a clinical fellowship in Pain Medicine at MGH, research fellowship with Clifford Woolf at Boston Children's Hospital and clinical investigator training through the Harvard Master's Program in Clinical and Translational Investigation. His clinical expertise spans the intersection of neurology and pain medicine.

Lori Pressman
Lori Pressman has been an independent deal maker,

license negotiator, business development and technology transfer strategic advisor since 2000. Recent assignments include licensing biotech and oncology inventions for academic medical centers, and securing IP licenses for small companies in energy and instrumentation . She was a Director at Harris & Harris (NASDAQ:TINY) from 2002-2012, an advisor for Axsun Technologies prior to its acquisition by Volcano, and Assistant Director with signatory authority of the MIT Technology Licensing Office.

She is a member of the grant review committee at the MIT Deshpande Center for Technological Innovation and frequent coach of entrepreneurs and students studying entrepreneurship and business development. She is a reasonable royalty damages expert, a metrics guru for AUTM and BIO, and a member of the AUTM Public Policy Committee. She is an inventor on a half dozen medical device patents and earned the SB, Physics from MIT and the MSEE from the Columbia School of Engineering. Earlier in her career, she was a practicing engineer, working on optoelectronic materials and devices at Bell Laboratories and Lasertron, an MIT Lincoln Laboratory start-up.

Abi Barrow - Director
abarrow@umassp.edu
Dr. Abigail Barrow is the Interim Executive Director, Office of Technology Commercialization and Ventures (OTCV) at the University of Massachusetts. She joined the UMass President's Office in 2004 as the Founding Director of the Massachusetts Technology Transfer Center (MTTC) which is housed in OTCV. At OTCV she supports the campus technology transfer programs as well as assisting with start-up formation and other system wide entrepreneurship activities at UMass. She is also responsible for the overall management of the MTTC and the development of its programs. Prior to joining UMass, Dr. Barrow served as managing director of William J. von Liebig Center at the University of California San Diego (UCSD). The von Liebig Center was created in 2001 to support the commercialization of research being performed in the UCSD Jacobs School of Engineering.

Dr. Barrow worked in a variety of roles at UCSD CONNECT from 1990 to 2001. At CONNECT, she developed and expanded many of its programs to support early-stage company formation and technology commercialization. The CONNECT program is internationally recognized and has been successfully replicated in many other regions around the world.

Dr. Barrow is on the board and is Chair of Venture Well (formerly the National Collegiate Inventors and Innovators Alliance). Dr. Barrow received her Ph.D. from the Science Studies Unit and a B.Sc. in Mechanical Engineering from the University of Edinburgh.

Moderator: Dr. Nathalie Goletiani, MD, Founder & CEO, POWERFEM Therapeutics
Dr. Goletiani is the Founder and Chief Executive Officer of POWERFEM Therapeutics, a company devoted to novel, networked treatment methods for the care of those suffering from substance abuse and mental illness. Her extensive clinical research into the hormonal effects of nicotine, opioid and cocaine use lead her to new concepts and mechanisms in understanding and treating psychiatric disorders, in particular, disorders experienced by underserved female populations. At Harvard's McLean Hospital, she was charged with rebuilding and responsible for all the operations of Clinical Research Program, including simultaneously running multiple clinical trials. Based on her patented work, she founded POWERFEM Therapeutics, an independent company devoted to creating new treatments and healthcare solutions. POWERFEM incorporates novel disease concepts and treatments

to design cost-effective, integrated mental and substance abuse care solutions across multiple provider networks.

Dr. Goletiani has received numerous national and international awards including most recently the Harvard Livingston Award for the investigation of complex underlying mechanisms in the neurobiology of women. She also received a Harvard University Zinberg Fellowship specifically to support her research on alcohol and drug use disorders. Her research provides a valuable basis for psychotherapeutic public policy decision making on issues of substance abuse and the integrated treatment of mental illness. She has extensively published the results of her research in peer reviewed journals.
Nathalie completed basic and clinic fellowships at the Harvard School of Public Health and at Harvard Medical School. In addition, she has been trained at and conducted medical research at Tbilisi State Medical University, University of Amsterdam and King's College in London.

Meeting Location: Pivotal Labs, 145 Broadway, 3rd Floor, Cambridge, MA

Check for Updates: Boston Entrepreneurs' Network Website at (http://www.boston-enet.org)

Reservations: ENET Constant Contact meetings are free to ENET members and $**10** for non-members. No reservations are needed for the dinner. To expedite sign-in for the meeting, we ask that everyone -- members as well as non-members -- pre-register for the meeting online. Pre-registration is available until midnight the day before the meeting. If you cannot pre-register, you are welcome to register at the door.

IEEE Boston Section Social Media Links:

Twitter: https://twitter.com/ieeeboston

Facebook: https://www.facebook.com/IEEEBoston

YouTube: https://www.youtube.com/user/IEEEBostonSection

Google+: https://plus.google.com/107894868975229024384/

LinkedIn: https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about

Locally held IEEE Conferences

2017 IEEE International Symposium on Technolgies for Homeland Security
April 25 - 26, 2017
www.ieee-hst.org

(The technical program, conference registration are now online)

2017 IEEE International Midwest Symposium on Circuits and Systems
August 6 - 9, 2017
www.MWSCAS2017.org
(Call for Papers Deadline, March 10, 2017)

2017 IEEE High Performance Extreme Computing Conference HPEC '17
September 12 - 14, 2017
www.ieee-hpec.org
Submission deadline is May 19, 2017

Microwave Theory and Techniques, and Aerospace and Electronics Systems Societies - 6:00PM, Wednesday, 22 February

Photonics for Microwave Phased Arrays

Dr. Paul Juodawlkis, MIT Lincoln Laboratory

Fiber-optic communications technology serves as the primary backbone of the information age due to the ultra-wide bandwidth (> 50 THz) and low loss (< 0.5 dB/km) of modern optical fibers. Fiber-optic systems are used to transfer voice and data around the world, stream high-definition movies to the home, and provide backhaul connectivity for cellular phone networks. While the majority of these optical interconnects are used to transfer digital signals, similar photonic components (e.g., lasers, optical modulators, photodetectors) can be used to generate, process, and transfer analog signals. This talk will explore the application of both analog and digital photonic technologies to microwave phased-arrays. We will motivate the potential impact of photonics on microwave phased-arrays, provide an overview of the differences between analog and digital photonic components and performance metrics, describe the fundamentals and state-of-the-art for analog or microwave photonic links, and discuss the analog and digital functions in phased-array systems that can be augmented or replaced using photonic technologies.

Dr. Paul Juodawlkis is Assistant Leader of the Quantum Information and Integrated Nanosystems Group at MIT Lincoln Laboratory where he is working to develop photonic integrated circuit (PIC) technology for application to quantum information systems, optical communications, laser radar, inertial navigation, and microwave sensing. Over the past decade, he led the team that developed the semiconductor slab-coupled optical waveguide amplifier (SCOWA) and used it to realize Watt-class power amplifiers, mode-locked lasers, and low-noise single-frequency lasers having record performance. In earlier work, he made key contributions to the development of optical sampling techniques for microwave frequency translation and photonic analog-to-digital conversion. Dr. Juodawlkis has authored or coauthored over 130 peer-reviewed journal and conference publications, and has participated on a number of technical program committees, including serving as Program Co-Chair (2010) and General Co-Chair (2012) of the Conference on Lasers and Electro-Optics (CLEO). He was an elected member of the IEEE Photonics Society Board of Governors (2011-2013), served as Vice President of Membership for the Society (2014-2016), and is presently Secretary-Treasurer for the Society. Dr. Juodawlkis is a Fellow of both the IEEE and the Optical Society (OSA). He holds a BS degree from Michigan Technological University, a MS degree from Purdue University, and a PhD degree from the Georgia Institute of Technology, all in electrical engineering.

Meeting Location: 3 Forbes Road, Lexington, MA (Refreshments: 5:30PM)

To assist us in planning this meeting, please pre-register at *http://www.ieeeboston.org/Register/*.

Consultants Network - 6:30PM, Tuesday, 28 February

Is Networking & Speaking Bringing You Lots of New Business? If Not, Stop Leaving $$$ on the Table!

Networking and public speaking have long been the lifeblood of management consultants seeking new business. When done right, new contacts or a well-presented speaking engagement can yield a veritable gold mine of future projects. If that's not happening for you, this program will change your business life.

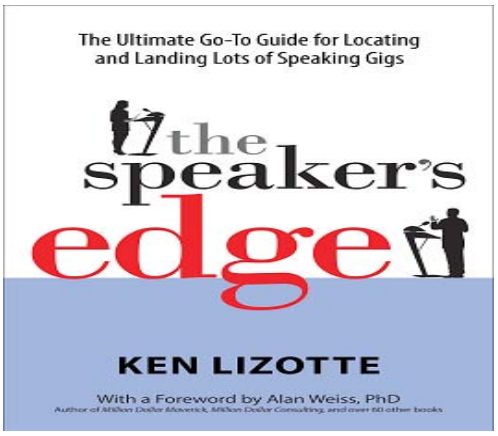
Alan Weiss has coined the phrase, "Make them come to you!" By practicing techniques in this session, and by rewiring your mindset, you'll soon be ensuring that Alan's catch phrase is your slogan too. Doing it "right" ensures that qualified prospects and repeat customers seek *you* out rather than the other way around. .

In this session, we'll discuss mistakes and limiting assumptions of networking & speaking as well as innovative best practices that really work. Topics will include:

- Why making "great connections" isn't enough
- Why delivering a terrific presentation isn't enough
- What most speakers don't bother doing to leverage their speaking gigs
- What most consultants don't bother doing to leverage their networking
- Why you should publish a book or articles
- Replace your elevator pitch with something amazing!
- Social media helps … but only a little
- How to follow up in a way that enhances your value
- Short tips from Ken's survey of successful networkers and speakers

By the end of this session, you'll have acquired immediately actionable steps that will transform your networking and public speaking efforts forever. Before long, your results will markedly improve as you will stop leaving good money on the table!

Ken Lizotte CMC is Chief Imaginative Officer (CIO) and founder of Emerson Consulting Group Inc., a consulting firm that transforms individual management consultants and management consulting firms into "thoughtleaders"



A thoughtleader in his own right having been interviewed by The Wall Street Journal, Fortune Magazine, Newsweek, Financial Times, Investors' Business Daily, National Public Radio, CBS-TV and Writer's Digest Magazine, among others.

Ken is the author of seven books including, *The Expert's Edge: Become the Go-To Authority that People Turn to Every Time* (McGraw-Hill). *His newest book is The Speaker's Edge: The Ultimate Go-To Guide for Locating and Landing Lots of Speaking Gigs, with a foreword by Alan Weiss PhD* (Maven House Press)

PLEASE NOTE: The meeting is open to the public. No charge for Consultants Network members or employees of Constant Contact; $5 entrance fee for all others. Casual dress. Registration (no registration required).

The Consultants Network meeting starts at 6:30 PM. The meeting will take place at Constant Contact, Reservoir Place - 1601 Trapelo Road, Waltham, MA 02451.

A nohost, PRE-MEETING DINNER will take place at 5:15 PM (sharp) at Bertucci's, 475 Winter Street, Waltham, MA 02451 (exit 27B, Rte 128).

Driving Directions
To Bertucci's:
Follow I-95/route 128 to Winter St in Waltham. Take exit 27B from I-95/Route 128. Turn left on Wyman S, then left on Winter St. Bertucci's is the 1st right after crossing the bridge over I95/Route128.

To Constant Contact:
Follow I-95/route 128 to Trapelo Rd in North Waltham, Waltham. Take exit 28 from I95/route 128. Constant Contact is the 1st right after crossing the bridge over I95/Route128.

Consultants Network meetings generally take place on the fourth Tuesday of each month, but are not held during the summer months. Check the Consultants Network website for meeting details and last-minute information.

For more information, e-mail chairman@bostonconsult.com
To assist us in planning this meeting, please pre-register at *http://www.ieeeboston.org/Register/*.

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YouTube: https://www.youtube.com/user/IEEEBostonSection

Google+: https://plus.google.com/107894868975229024384/

LinkedIn: https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about

60th IEEE International Midwest Symposium on Circuits and Systems

Boston, MA, USA | August 6th-9th, 2017
www.mwscas2017.org

Tufts University · DRAPER · IEEE · CAS

CALL FOR PAPERS IEEE INTERNATIONAL MWSCAS 2017

The IEEE International Midwest Symposium on Circuits and Systems is the oldest Circuits and Systems Symposium sponsored by IEEE. The 60th edition will be held on the campus of Tufts University, Boston, MA, USA, August 6 - 9, 2017. MWSCAS 2017 will include oral and poster sessions, student paper contest, tutorials given by experts in circuits and systems topics, and special sessions. Topics include, but are not limited to:

Track 1. Analog Circuits and Systems I
- 1.1 Analog Circuits
- 1.2 Analog Systems
- 1.3 Biomedical Electronics
- 1.4 Bioengineering Systems and Bio Chips
- 1.5 Other Analog Circuits and Systems

Track 2. Analog Circuits and Systems II
- 2.1 Linear Analog Systems
- 2.2 Non-linear Analog Systems
- 2.3 System Architectures
- 2.4 Neuromorphic Systems

Track 3. Digital Circuits and Systems I
- 3.1 Digital Integrated Circuits
- 3.2 System On a Chip (SOC) and Network on a Chip (NOC)

Track 4. Digital Circuits and Systems II
- 4.1 Digital Filters
- 4.2 Hardware-Software Co-Design
- 4.3 Other Digital Circuits and Systems

Track 5. Communications Circuits and Systems
- 5.1 Communications Circuits, Computers and Applications
- 5.2 Communications Systems and Control
- 5.3 Information Theory, Coding and Security
- 5.4 Communications Theory
- 5.5 Other Communications Circuits and Systems

Track 6. RF and Wireless Circuits and Systems
- 6.1 RF Front-End Circuits
- 6.2 Mixed-Signal RF and Analog and Baseline Circuits
- 6.3 Wireless Mobile Circuits and Systems and Connectivity
- 6.4 VCO's and Frequency Multipliers, PLL's and Synthesizers
- 6.5 Other RR and Wireless Circuits and Systems

Track 7. Sensor Circuits and Systems
- 7.1 Technologies for Smart Sensors
- 7.2 Sensor Fusion
- 7.3 Control Systems
- 7.4 Mechatronics and Robotics
- 7.5 Other Sensor Circuits and Systems

Track 8. Converter Circuits and Systems
- 8.1 Analog to Digital Converters
- 8.2 Digital to Analog Converters
- 8.3 DC-DC Converters
- 8.4 Other Converter Circuits and Systems

Track 9. Signal and Image Processing
- 9.1 Analog and Mixed Signal Processing
- 9.2 Digital Signal Processing
- 9.3 Signal Processing Theory and Methods
- 9.4 Image, Video and Multi-Dimensional Signal Processing
- 9.5 Other Signal and Image Processing

Track 10. Hardware Design
- 10.1 Processor and Memory Design
- 10.2 MEMS/NEMS
- 10.3 Nano-Electronics and Technology
- 10.4 Optics and Photonics
- 10.5 Power Management, Power Harvesting and Power Electronics
- 10.6 Photovoltaic Devices/Panels and Energy Harvesting

Track 11. Hardware Security
- 11.1 Hardware Authentication and Physically Unclonable Functions (PUFs)
- 11.2 Trusted Microelectronics
- 11.3 Hardware Anti-Tamper
- 11.4 Architectural System Security
- 11.5 Other Hardware Security

Prospective authors are invited to submit a full paper (4 pages) describing original work. Only electronic submissions will be accepted. Papers should include title, abstract, and topic category from the list above in standard IEEE two-column format for consideration as lecture or poster. Both formats have the same value, and presentation method will be chosen for suitability. All submissions should be made electronically through the MWSCAS 2017 web site (http://www.mwscas2017.org). Students are encouraged to participate in the best student paper award contest. Accepted papers will be published in the conference proceedings subject to advance registration of at least one of the authors.

IMPORTANT DATES

March 18: Tutorial and Special Session proposals deadline
March 18: Regular and Student paper submission deadline
April 1: Special session and invited paper submission deadline
April 29: Notice of acceptance
May 20: Final camera-ready paper deadline

www.mwscas2017.org

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CALL FOR PAPERS

www.ieee-hpec.org

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The IEEE High Performance Extreme Computing Conference (HPEC '17) will be held in the Greater Boston Area, Massachusetts, USA on 12 – 14 September 2017. The HPEC charter is to be the premier conference in the world on the confluence of HPC and Embedded Computing.

The technical committee seeks new presentations that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- Advanced Multicore Software Technologies
- Case Studies and Benchmarking of Applications
- Automated Design Tools
- Mapping and Scheduling of Parallel and Real-Time Applications
- Computing Technologies for Challenging Form Factors
- ASIC and FPGA Advances
- Open System Architectures
- Data Intensive Computing
- Big Data and Distributed Computing
- Interactive and Real-Time Supercomputing
- Graph Analytics and Network Science
- Fault-Tolerant Computing
- Embedded Cloud Computing
- Digital Front Ends
- General Purpose GPU Computing
- Advanced Processor Architectures
- Secure Computing & Anti-Tamper Technologies
- New Application Frontiers
- High Performance Data Analysis
- Cloud HPEC
- Big Data Meets Big Compute

HPEC accepts two types of submissions:

1. Full papers (up to 6 pages, references not included), and
2. Extended abstract (up to 2 pages, references included).

IMPORTANT DATES:

Submission Deadline: **May 19, 2017**
Notification of Acceptance: **June 16, 2017**

Preference will be given to papers with strong, quantitative results, demonstrating novel approaches or describing high quality prototypes. Authors of full papers can mark their preference for a poster display or an oral presentation. Presenters who wish to have hardware demonstrations are encouraged to mark their preference for a poster display. Accepted extended abstracts will be displayed as posters. All paper and extended abstract submissions must use the approved IEEE templates. Full paper submissions with the highest peer review ratings will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions and extended abstracts are published on ieee-hpec.org. Vendors are encouraged to sign up for vendor booths. This will allow vendors to present their HPEC technologies in an interactive atmosphere suitable for product demonstration and promotion.

We welcome input (hpec@ieee-hpec.org) on tutorials, invited talks, special sessions, peer reviewed presentations, and vendor demos. Instructions for submitting will be posted on the conference web site shortly.

Practical Antenna Design for Wireless Products

An intensive Two-day Workshop

Time & Date: 9AM - 4:30PM, Thursday & Friday, June 1 & 2

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speakers: Henry Lau, Lexiwave Technology

INTRODUCTION

To stay competitive in today's fast evolving business environment, faster time to market is necessary for wireless communication products. Playing a critical role in determining the communication range of products, RF design, particularly the antenna design, becomes crucial to the success of the introduction of new wireless products. Competence in advanced antenna designs can definitely strengthen the competitive edge of RF product design or manufacturing companies.

COURSE OBJECTIVES

This 2-day course aims to provide participants with technical insights on the vital aspects of antenna design from a practical and industrial perspective. It covers the fundamental antenna concepts and definitions, specifications and performance of different types of commonly-used and advanced antennas in RF products. Simulation tools will be introduced and discussed. Practical implementation strategies in RF products for optimum antenna performance will also be presented.

WHO SHOULD ATTEND

Antenna designers, RF designers, wireless product designers, field application engineers, business development engineers and managers, design managers, and related professionals.

OUTLINE

Day 1 (1 June)
Fundamental Concepts
1. Antenna Fundamental
* Basic types of Antenna
* Dipole, Monopole, helical, loop, printed PCB
* Radiation Mechanism
* Source of radiation
* Characteristics of radiation

2. Specification and Performance
* Radiation pattern
* Antenna efficiency, aperture
* Impedance and circuit matching
* Directivity, gain
* Friis Transmission Equation

3. Antenna Elements
* Dipole antenna
* Monopole antenna
* Multi-band antenna
* Miniature chip type antenna
* Loop antenna

Day 2 (2 June)
Advanced Antenna Elements
4. Miniature antenna for portable electronics
* Patch, inverted-L, inverted-F
* Meandered line, multi-band
5. CAD Design and Simulation
* CAD tools

* Design strategies
* Limitations
* Case studies

Practical implementation strategies

6. How to design good antennas

* Understand the requirements
* Selection of antenna type, size and geometry
* Location and placement

7. Team work with product designers, electronic engineers and mechanical engineers

* Why it matters
* Case studies on designing good antennas

EXPERTISE

Henry Lau received his M.Sc. and MBA degrees from UK and USA respectively. He has more than 26 years of experience in designing RF systems, products and RFICs in both Hong Kong and US. He worked for Motorola and Conexant in US as Principal Engineer on developing RFICs for cellular phone and silicon tuner applications. Mr Lau holds five patents all in RF designs. He is currently running Lexiwave Technology, a fables semiconductor company in Hong Kong and US designing and selling RFICs, RF modules and RF solutions. He has also been teaching numerous RF-related courses internationally.

Decision (Run/Cancel) Date for this Course is Monday, May 22, 2017

Payment received by May 17
IEEE Members $405
Non-members $435

Payment received after May 17
IEEE Members $435
Non-members $455

http://ieeeboston.org/practical-antenna-design-wireless-products/

Simulink Model based FPGA Digital Design and Digital Signal Processing

Time & Date: Course postponed until fall 2017

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speakers: Cherif Chibane, Rick Rosson; MIT Lincoln Laboratory

Description:

Over the last 30 years, applications for Field Programmable Gate Array (FPGA) designs have increased exponentially. FPGA's have moved from just digital designs to other areas such as embedded controllers, Digital Signal Processing, communication systems, and configurable computing. This has made exposure to and mastery of FPGA design crucially important for many people in industry and academia.

This course provides a detailed overview of FPGA technologies, a top-down design workflow, modeling and simulation, standard design tools, and applications. Using a mixture of theory and hands-on laboratories, the course provides students what they need to know in modeling, simulation, design, verification, and implementation of multi-disciplinary applications targeting FPGA's. This course provides plenty of hands-on lab exercises to reinforce the key concepts. While the material covered in this class targets Xilinx devices, it can be easily used for others devices such as ALTERA and other FPGA devices.

Presenters:

This course will be jointly presented by Cherif Chibane and Rick Rosson of MIL Lincoln laboratory. Their combined and complementary expertise will greatly benefit attendees from industry and academia.

Cherif Chibane is currently with MIT Lincoln laboratory as a research staff. He was one of the early adopters of FPGA's for configurable computing. Prior to MIT-LL, he was part of the BAE Systems team that pioneered the use FPGA's for Software Denied Radio (SDR). He has more than 25 years in the design of advanced configurable computing using FPGA's for DSP, digital logic, and embedded designs.

Rick Rosson is a senior modeling and simulation engineer at MIT Lincoln Laboratory. Prior to joining MIT-LL, Rick served as a senior applications engineer at MathWorks for 9 years, with a focus on digital signal processing, statistical signal processing, embedded systems design, modeling and simulation, and data analysis and visualization. Rick holds a Master of Science in Electrical Engineering from Boston University and a Master of Science in Management from the MIT Sloan School of Management.

Agenda

Session #1

- Course Overview
- Model based benefits in today's FPGA designs.
- Simulink/Matlab Overview
- Simulink Examples

Session #2
• FPGA Technologies Overview
• Xilinx ISE Overview
• Fixed point Vs floating point overview
• HDL/FPGA Examples

Session #3
• Preparing Simulink models for HDL code generation
• Generating HDL code from Simulink
• Verifying the generated code
• Code Generation Examples

Session #4
• Modeling Signal Processing and Communications Systems in Simulink®
• Signal Processing Examples
• Implementing Signal Processing Systems on FPGA's

Session #5
• Advanced Topics using FPGA's
• End-To-End Design and Verification
• End-To-End Design Example
• Course Summary

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gamil.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

SAVE THE DATE! PLAN TO ATTEND!

2017 IEEE International Symposium on Technologies for Homeland Security

IEEE Advancing Technology for Humanity

25 – 26 April Westin Hotel, Waltham, MA

http://ieee-hst.org/

PLENARY SPEAKER: Kay C. Goss, CEM President, World Disaster Management, LLC

Internationally recognized expert, lecturer, author on Emergency Management and General Resiliency

The 16th annual IEEE Symposium on Technologies for Homeland Security (HST '17), will be held 25-26 April 2017 **must attend event**, in the Greater Boston, Massachusetts area. This symposium brings together innovators from leading academic, industry, business, Homeland Security Centers of Excellence, and government programs to provide a forum to discuss ideas, concepts, and experimental results.

Produced by IEEE with technical support from DHS S&T, IEEE, IEEE Boston Section, and IEEE-USA and organizational support from MIT Lincoln Laboratory, Raytheon, Battelle, and MITRE, this year's event will once again showcase selected technical paper and posters highlighting emerging technologies in the areas of:

- **Cyber Security**
- **Biometrics & Forensics**
- **Land and Maritime Border Security**
- **Disaster and Attack Preparedness, Mitigation, Recovery, and Response**

There are over 110 paper and posters to be presented at the symposium with focus on technologies with applications available for implementation within about five years. All areas will cover the following common topics:

- Strategy and threat characterization, CONOPs, risk analysis,
- Modeling, simulation, experimentation, and exercises & training, and
  - Testbeds, standards, performance and evaluations.

In addition there will be plenary sessions as well as ample networking activities to interact and exchange ideas with speakers and other symposium attendees.

Contact Information

For more detailed information on sponsorship and Exhibit Opportunities, visit the website http://ieee-hst.org/ or email: information@ieee-hst.org.

The symposium technical program as well as the conference registration and hotel reservation pages are now online (www.ieee-hst.org)

Technical Sessions

Cyber Security Track:
#1: Cyber-Physical Systems
#2: Authentication
#3: Intrusion Detection
#4: Approaches in Cybersecurity Modeling
#5: Secure Systems
#6: Analytics
#7: Testbeds and Training Environments
#8: Privacy
#9: Classification and Scoring Algorithms in Cybersecurity

Attack/Disaster Track:
#1: Critical Infrastructure
#2: Cyber Risk Management and Intelligence Analysis
#3: Resilience
#4: Disaster Preparedness and Response
#5: Network Vulnerability
#6: Situational Awareness
#7: Machine Learning and UAV
#8: Terrorism and Disaster Preparedness

Plus 20 Poster Presentations during our Welcome/networking Reception

Border Security Track:
#1: Airborne Sensing
#2: Enhancing Data Exploitation 1
#3: Enhancing Data Exploitation 2
#4: Ground-based Hardware for Border and Customs Enforcement
#5: Counter-UAS and Small Aircraft Detection
#6: Underwater Imaging
#7: Human- and Cargo-Borne Concealed Threat
#8: Radiological and Nuclear Detection

Biometrics & Forensics Track
#1: Facial Recognition
#2: Finger and Palm Prints
#3: Video Analytics
#4: Ocular Biometrics and Other Modes

Software Development for Medical Device Manufacturers

An intensive Two-day Workshop

Time & Date: 8:30AM - 4:30PM, Wednesday & Thursday, April 5 & 6, 2017

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speakers: Steve Rakitin, President, Software Quality Consulting, Inc.

OVERVIEW:

Developing software in compliance with FDA, EU regulations and international standards is challenging. This two-day intensive course provides practical guidance and suggestions for developing software that complies with applicable FDA and EU regulations, guidance documents and international standards such as IEC 62304 and ISO 14971. The focus of this course is interpreting Design Controls for software. Each section of the Design Controls regulation (820.30) is discussed from the software perspective. Corresponding requirements from IEC 62304 are woven into the flow.

In-depth discussion of critical topics such as Requirements, Software Verification & Validation, Risk Management and Fault Tree Analysis are included. In addition, techniques for validating software development tools and software used in Manufacturing and Quality Systems are also discussed. Interactive group exercises are included to facilitate discussion and learning.

WHO SHOULD ATTEND

Software and firmware engineers, software managers, RA/QA staff, validation engineers, and project managers. Anyone interested in learning how to develop medical device software in compliance with regulations, standards and guidance documents.

COURSE OUTLINE

- **Introduction**
  - Medical Device Definitions – FDA and EU
  - Regulatory Roadmap and FDA/EU Device Classification Schemes
  - FDA Regulations and Guidance Documents for Software
  - Standards – ISO 13485, IEC 62304, ISO 14971, EN-14971, IEC 60601, and IEC 62366-1
  - All Software is Defective

- **Interpreting Design Controls for Software**
  - Software Development Models
  - Design and Development Planning
  - Design Inputs
    - **About Requirements…**
    - **Requirements Exercise**
  - Design Outputs
  - Design Reviews
  - Design Verification
    - Software Verification Techniques
  - Design Validation
    - Software Validation Process
  - Design Transfer
  - Design Changes
  - Design History File

- **Validation of…**
  - Software Tools used to develop Medical Device Software
  - Software used in Manufacturing
  - Software used in Quality Systems

- **Risk Management**
  - Standards and Regulations
  - Terms and Concepts
  - Risk Management Process
  - Risk Management Tools and Techniques
    - **Fault Tree Exercise**
  - Data Collection and Analysis
  - Documentation Requirements

- **Summary**

- **Comprehensive reference materials included**

Speaker Bio:

Steven R. Rakitin has over 40 years experience as a software engineer including 25 years of experience in the medical device industry. He has worked with over 85 medical device manufacturers worldwide, from startups to Fortune 100 corporations. He has written several papers on medical device software risk management as well as a book titled: Software Verification & Validation for Practitioners and Managers.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE and a member of MassMEDIC. He is on the Editorial Review Board for the ASQ Journal Software Quality Professional.

As President of Software Quality Consulting Inc., he helps medical device companies comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

Decision (Run/Cancel) Date for this Course is Friday, March 24, 2017

Payment received by March 20
IEEE Members $465
Non-members $495

Payment received after March 20
IEEE Members $495
Non-members $545

http://ieeeboston.org/software-development-medical-device-manufacturers-intensive-two-day-workshop/

More Digital Signal Processing (DSP) for Wireless Communications

Time and Dates: 6 - 9PM, Wednesdays, March 22, 29, April 5, 12, 26

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Dan Boschen, Microsemi

Course Summary

This course is a continuation of the IEEE course "DSP for Wireless Communications" also taught by Dan Boschen, detailing digital signal processing most applicable to practical real world problems and applications in radio communication systems. Students need not have taken the Part I course if they are familiar with basic DSP concepts.

This course brings together core DSP concepts to address signal processing challenges encountered in radios and modems for modern wireless communications. Specific areas covered include carrier and timing recovery, equalization, automatic gain control, and considerations to mitigate the effects of RF and channel distortions such as multipath, phase noise and amplitude/phase offsets.

Dan builds an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real world applications for mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges, rather than a tutorial on implementations with DSP processors.

Target Audience:

All engineers involved in or interested in signal processing for wireless communications. Students should have either taken the first part of this course "DSP for Wireless Communications" or have been sufficiently exposed to basic signal processing concepts such as Fourier, Laplace, and Z-transforms, Digital filter (FIR/IIR) structures, and representation of complex digital and analog signals in the time and frequency domains. Please contact Dan at boschen@loglin.com if you are uncertain about your background or if you would like more information on the course.

Benefits of Attending/ Goals of Course:

Attendees will gain a strong intuitive understanding of the practical and common signal processing implementations found in modern radio and modem architectures and be able to apply these concepts directly to communications system design.

Topics / Schedule:

Class 1:
DSP Review, Radio Architectures, Transforms, Mapping to Digital, Pulse Shaping, Eye Diagrams

Class 2:
ADC Receiver, CORDIC Rotator, Digital Down Converters, Numerically Controlled Oscillators

Class 3:
Digital Control Loops; Output Power Control, Automatic Gain Control

Class 4:
Digital Control Loops; Carrier and Timing Recovery, Sigma Delta Converters

Class 5:
RF Signal Impairments, Equalization and Compensation, Linear Feedback Shift Registers

Speaker's Bio:
Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 20 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems. Dan is currently at Microsemi (formerly Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page at:
http://www.linkedin.com/in/danboschen

Decision (Run/Cancel) Date for this Course is Monday, March 13, 2017

Payment received by March 9
IEEE Members $325
Non-members $360

Payment received after March 9
IEEE Members $360
Non-members $425

http://ieeeboston.org/digital-signal-processing-dsp-wireless-communications-2/

Locally held IEEE Conferences

2017 IEEE International Symposium on Technolgies for Homeland Security
April 25 - 26, 2017
www.ieee-hst.org
(The technical program , conference registration is now online)

2017 IEEE International Midwest Symposium on Circuits and Systems
August6 - 9, 2017
www.MWSCAS2017.org
(Call for Papers Deadline, March 10, 2017)

2017 IEEE High Performance Extreme Computing Conference HPEC '17
September 12 - 14, 2017
www.ieee-hpec.org
Submission deadline is May 19, 2017

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Last Notice Before Course Begins, Please Register now and Save $$$!!!

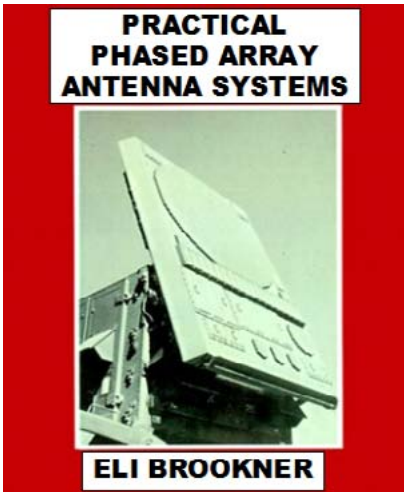
Phased-Array and Adaptive-Array Fundamentals and Their Recent Advances

Time & Date: 6 - 9PM, Mondays, Feb. 27, March 6,13, 20, 27, April 3, 10, 24, May 1, 15 (Snow/make-up days May 22, June 5, 12)

Location: MITRE Corp., 202 Burlington Rd., Bedford, MA (tentative)

Speaker: Dr. Eli Brookner, Raytheon, (Retired)

Text: Practical Phased Array Antenna Systems", Dr. Eli Brookner (included with registration)



"Practical Phased Array Antenna Systems", Dr. Eli Brookner, Editor, Artech House, 1991, Hardcover, 258 pages, List Price $179, Hardcover, 258 pages. Covers array fundamentals: phase and time-delay steering; grating lobes for 1- and 2-dimensional arrays; effects of errors and failures on gain, sidelobes and angle accuracy; array weighting, thinning, blindness, mutual coupling, elements, phase-shifters and feeds; limited field of view (LFOV) arrays; SPY-1; example design.

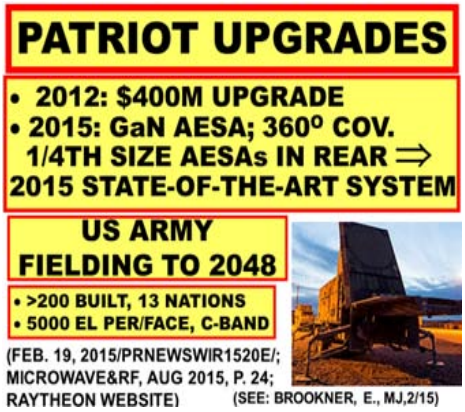
This course is based on the book entitled Practical Phased Array Antenna Systems by Dr. Eli Brookner. The book covers array basics and fundamentals which do not change with time. The course, the book and the notes will provide an ideal introduction to the principles of phased array antenna design and adaptive arrays. The course material and notes cover in addition recent developments in phased arrays updated to 2017.

With the explicitly tutorial approach the course and book offers a concise, introductory-level survey of the fundamentals without dwelling on extensive mathematical derivations or abstruse theory. Instead a physical feel will be given. The book provides extensive curves, tables and illustrative examples. Covered in easy terms will be sidelobe cancellation, full adaptive array processing without suffering its computation complexity (through the use of adaptive-adaptive array processing also called beam-space processing and eigenbeam processing). Finally, Space-Time Adaptive Array (STAP) for airborne platforms will be explained and related to the displaced phase center antenna (DPCA).

All Attendees of the class will receive trial trial license of MATLAB and Phased Array System Toolbox from MathWorks in addition to a set of examples which help demonstrate key array concepts covered in the course.

This course is intended for the engineer or scientist not familiar with phased-array antennas as well as the antenna specialist who wants to learn about other aspects of phased-array antenna systems as well as get the latest developments in array systems, such as: MIMO, metamaterial arrays, Extreme MMIC arrays, stealthing and cloaking. The major emphasis will be on the system aspects of phased-arrays.

Lecture #1. Monday February 27; Phased Array Fundamentals: Electronically Scanned Array (ESA) explained with tube COBRA DANE used as example. Covered will be: Near and Far Field Definitions, Phased Steering, Switched-Line Phase Steering; Time Delay Steering, Subarraying, Array Weighting, Monopulse, Duplexing, Array Thinning, Embedded Element, dual polarized circular waveguide element, advantage of triangular lattice over square lattice, Tour of COBRA DANE (6 stories high) via color slides.



Lecture #2. Monday March 6; Linear Array Fundamentals: Conditions for no grating lobes; beamwidth vs scan angle; sine space; Array Factor; sidelobe level vs antenna beamwidth; directivity; antenna efficiency factors; array weightings; array frequency scanning; array bandwith.

Lecture #3. Monday March 13; Planar Arrays: Array Factor; array separability; sine-space (sinα-sinß space, T- space); grating lobes location for triangular and rectangular lattice; directivity; very useful bell curve approximation; array thinning system issues.

Lecture #4. Monday March 20; Array Errors: Effects of element phase and amplitude element errors and element failures; simple physical derivation of error effects; paired echo theory; subarray errors; quantization errors; examples.

Lecture #5. Monday March 27; Radiating Elements: Waveguide; dipole; slotted waveguide; microstrip patch; stacked patch; notch (wideband); spiral; matching (wide-angle); waveguide simulator; practical limitations, mutual coupling and array blindness; scattering matrix; design procedure; polarization missmatch loss.

Lecture #6. Monday April 3; Active Phased Arrays: 2nd generation solid state hybrid active electronically scanned array (AESAs) covered using PAVE PAWS as example, T/R Module Introduced, Cross Bent Dipole Element, Mutual Coupling, Array Blindness, Tour of PAVE PAWS (6 stories) via color slides. 3rd Generation AESAs: THAAD (TPY-2), SPY-3, IRIDIUM, F-15 APQ-63(V)2, APG-79, XBR, AMDR and upgraded Patriot; GaAs and GaN microwave integrated circuits (Monolithic Microwave Integrated Circuit, MMIC).

Lecture #7. Monday April 10; Array Feeds: Corporate and space fed; Reactive (lossless) and matched (Wilkinson); even/odd node analysis. Se-

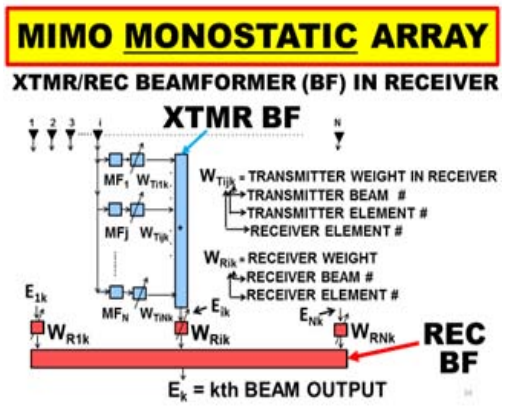
rial; Ladder; Lopez; Blass; Radial, Butler matrix; microstrip/stripline; Rotman Lens; SLQ-32; PATRIOT space-fed array; reflectarray.

a.) LOCKHEAD MARTIN (LM) SPACE FENCE RADAR SITE, b.) CUTAWAY OF TRANSMIT ARRAY, c.) CROSS-SECTION OF RADAR-ON-A-BOARD TRANSMIT LRUs (MICROWAVE J. SEPT-2016: HTTP://WWW.MICROWAVEJOURNAL.COM/ARTICLES/26872V

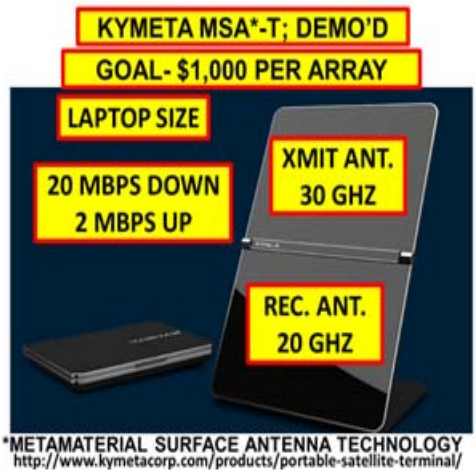
System Considerations: sequential detection, beam shape loss; receiver and A/D dynamic range; polarization miss-match loss; AESA noise figure and system temperature taking into account array mismatch.

Phase Shifters: Diode switched-line, hybrid-coupled, loaded-line; ferrite phase-shifters: non-reciprocal latching; diode vs ferrite; MEMS (Micro-Electro-Mechanical Systems) and its potential for a low cost ESA.

Lecture #8. Monday April 24; Limited Scan (Limited Field of View [LFOV]) Arrays: Explained using simple high school optics for TPS-25, 1st Electronically Scanned Array (ESA) put in production. Fundamental Theorem specifying minimum number of phase shifters needed for a specified scan angle. Method for realizing this minimum using overlapped array antenna elements as with HIPSAF lens array system and Microwave Landing System (MLS); reflector; randomized oversized elements; LFOV using sum and difference patterns; use of spatial filters to reduce grating lobes and sidelobes. Hemispherical Coverage Dome Antenna.

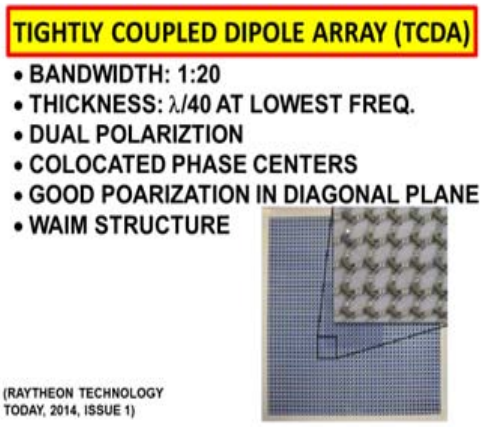


Lecture #9. Monday May 1; Phased Array Amazing Advances and Breakthroughs --



Part 1: SYSTEMS: Patriot now has GaN active electronically scanned array (AESA) providing 360o coverage, now a 2015 state-of-the-art AESA radar system; S-band AMDR provides 30 times the sensitivity and number of tracks as SPY-1D(V); 3, 4, 6 faced "Aegis" radar systems developed by China, Japan, Australia, Netherlands, USA;

EXTREME MMIC: can now put on single chip 256-Element 60 GHz Transmit Phased Array, such arrays may be used for the internet-of-things and in cell phones which by 2020 is expected to number 50 billion, expect such single chip arrays to cost only few dollars in future; All the RF circuitry for mm-wave automobile radars being put on a chip, in future such radars could be produced for just a few dollars; Valeo Raytheon (now Valeo Radar) developed low cost, $100s, car 25 GHz 7 beam phased array radar; ~2 million sold.

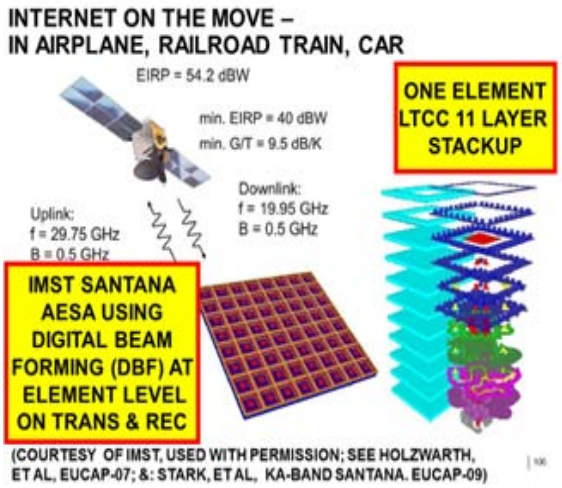


LOW COST PACKAGING: Raytheon, Rockwell Collins, Lincoln-Lab./MA-COM and South Korea developing low cost flat panel S and X-band AESAs using commercial components, practices and printed circuit boards (PCBs);

DIGITAL BEAM FORMING (DBF): Israel, Thales, Australia and Lockheed Martin(LM) have under

development array with an A/D for every element channel (LM array has 172,000 channels and A/Ds); Raytheon developing mixer-less direct RF A/D having >400 MHz instantaneous bandwidth, reconfigurable between S and X-band.

MOORE'S LAW: Not dead yet; Slowed down but has much more to go; potential advance via: graphene, spintronics, memristors, synaptic transistors and quantum computing.

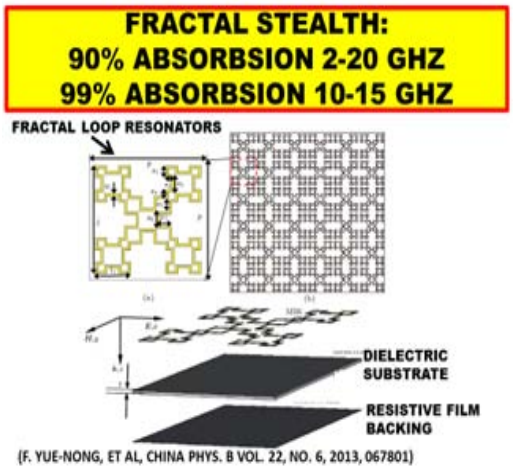


MATERIALS: GaN can now put 5X to 10X the power of GaAs in same footprint, 38% less costly, 100 million hr MTBF, Raytheon invested $200 million to develop GaN.

METAMATERIALS: Material custom made (not found in nature): 20 and 30 GHz metamaterial electronically steered antennas demonstrated December 2013 transmission to satellites and back, goal is $1K per antenna, how this antenna works explained for first time; 2-20GHz stealthing by absorption simulated using <1 mm coating; target made invisible over 50% bandwidth at L-band using fractals; Focus 6X beyond diffraction limit at 0.38 μm; 40X diffraction limit, λ/80, at 375 MHz; In cell phones provides antennas 5X smaller (1/10th λ) having 700 MHz-2.7 GHz bandwidth; The Army Research Laboratory in Adelphi MD has funded the development of a low profile metamaterial 250-505 MHZ antenna having a □/20 thickness; Provides isolation between antennas with 2.5 cm separation equivalent to 1 m separation; used for phased array WAIM.

Sidelobe Cancellers (SLC): The simple single-loop, feed-forward canceller is introduced in easy physical terms. This is followed by a discussion of the simple single-loop feedback canceller with and without hard limiting. The normalized feedback SLC will also be covered. Next the multiple-loop SLC (MSLC) will be covered. Applied to the MSLC will be the Gram-Schmidt, Givens and Householder orthonormal transformation methods. Systolic array implementations will be given.

Lecture #10. Monday May 15; Fully Adaptive Arrays: The optimum weight for a fully adaptive array is developed using a very simple derivation. Methods for calculating this optimum weight are given using the Sample Matrix Inversion (SMI) algorithm, the Applebaum-Howells adaptive feedback loop method, a recursive method, and Gram-Schmidt, Givens and Householder orthonormal transformations developed for the tracking problem and for the MSLC. The use of eigenvector beams and a whitening filter will also be developed. It will be shown how the latter reduces the transient response. Methods for obtaining the benefits of a fully adaptive array without its high computation and large transient time disadvantages are given. These are the adaptive-adaptive array processing procedures, the use of eigenbeam space, and the method of finding the largest eigenvectors and in turn their eigenbeams. The STAP algorithm covered.



Phased Array Amazing Advances and Breakthroughs --

Part 2: NEW MIMO (MULTIPLE INPUT MULTIPLE OUTPUT) ARRAYS: Explained in simple physical terms rather than with heavy math. Gives attendees an understanding of where it makes sense to

use. Contrary to what is claimed MIMO array radars do not provide 1, 2 or 3 orders of magnitude better resolution and accuracy than conventional array radars; also contrary to claims made MIMO should not provide better minimum detectable velocity for airborne radars.

MIMO and JAMMING: MIMO does not provide better barrage-noise-jammer, repeater-jammer or hot-clutter rejection than conventional array radars. SAR/ISAR: Principal Components of matrix formed from prominent scatterers track history used to determine target unknown motion and thus compensate for it to provide focused ISAR image. Technology and Algorithms: A dual polarized, low profile, (□/40), wideband (1:20) antenna can be built using tightly coupled dipole antennas (TCDA); Lincoln Lab increases spurious free dynamic range of receiver plus A/D by 40 dB; MEMS: Has potential to reduce the T/R module count in an array by a factor of 2 to 4; Can provide microwave filters tunable from 8-12 GHz that are 200 MHz wide;

LOW COST PRINTED ELECTRONICS: 1.6 GHz printed diodes achieved (goal 2.4 GHz).

ELECTRICAL AND OPTICAL SIGNALS ON SAME CHIP: Will allow data transfer at the speed of light; IR transparent in silicon.

BIODEGRADABLE ARRAYS OF TRANSISTORS OR LEDS: Imbedded under skin for detecting cancer or low glucose.

QUANTUM RADAR: Has potential to defeat stealth targets.

NEW POLARIZATIONS: OAMS, (ORBITAL ANGULAR MOMENTUM) unlimited data rate over finite band using new polarizations??

Your Registration Includes: 1 textbook; 15 Reprints; over 800 Vugraphs; trial license of MATLAB and Phased Array System Toolbox from MathWorks with examples demonstrating key array concepts covered in the course.

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- **1 textbook**
- **15 Reprints**
- **over 800 Vugraphs**
- **trial license of MATLAB and Phased Array System Toolbox from MathWorks with examples demonstrating key array concepts covered in the course.**

Decision (Run/Cancel) Date for this Course is Monday, February 20, 2017

Payment received by February 15
IEEE Members $300
Non-members $340

Payment received after February 15
IEEE Members $340
Non-members $370

http://ieeeboston.org/phased-array-adaptive-array-fundamentals-recent-advances/

Locally held IEEE Conferences

2017 IEEE International Symposium on Technologies for Homeland Security
April 25 - 26, 2017
www.ieee-hst.org
(The technical program, conference registration is now online)

2017 IEEE International Midwest Symposium on Circuits and Systems
August 6 - 9, 2017
www.MWSCAS2017.org
(Call for Papers Deadline, March 10, 2017)

2017 IEEE High Performance Extreme Computing Conference HPEC '17
September 12 - 14, 2017
www.ieee-hpec.org
Submission deadline is May 19, 2017

QA and Testing in DevOps Automation

Time & Date: 8AM - 5PM, Thursday, April 20 (Please note new date!!!)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Rajkumar Joghee Bhojan, Wipro Technologies

Introduction: In most of the IT organizations, there are hundreds of applications are getting deployed per release. Currently, Agile projects release cycle duration is reduced dramatically. In this "Fail Fast" environment, choosing right test automation tool and its framework becomes imperative for delivering quality software. This day-long course (lecture/lab) will address the following questions: How to create new ways of adopting QA and testing in their core software? Are we able to deliver better product using existing testing methodologies?

Format: lecture/lab

Topics

- Comprehend the need of automated testing.
- Employ TestNG and Eclipse to execute and write tests.
- Develop a group of test classes with the use of WebDriver.
- Building POM framework
- Running Tests in Parallel
- Understanding how to use Jenkins and GitHub for Selenium Tests
- Design tests to minimize code using inheritance

Target Audience: IT Professionals, Students both UG and PG with Computer Knowledge and Researchers

Benefits of Attending the Course:

- Learning recent technologies in Test Automation space.
- Will get knowledge of Selenium and its techniques in trending technologies

*** Gain Hands-on experience in Selenium WD.**

- Latest technologies used in Software Testing
- Participants can directly implement the taught methodologies in their software projects

Speaker Bio: Rajkumar J.Bhojan is a Test Architect (TA), Wipro Technologies, Quincy, MA, USA. He has over two decades of professional experience in both IT and Academics. He holds M.Sc., (Phy), MCA, and M.Phil (CS). He has executed IT projects in diverse geographies including India, Australia & USA. He has worked as a QA Manager, Scrum Master, Corporate Trainer and Principal Consultant in reputed organizations. He has presented many technical papers at International conferences, Journals, IEEE forums and Google Tech Talks. He is a Certified Scrum Master and has rich experience in Agile/scrum Methodologies. He is a member in IEEE and ACM.
http://sites.ieee.org/sem/files/2013/07/May_2014-WL_Rev1.pdf
http://www.atagg.agiletestingalliance.org/speakers.html. http://princetonacm.acm.org/tcfpro/
He also spoke at Google Tech Talks (GTAC-2016).
https://www.youtube.com/watch?v=RfQi5PNO4L8.

Course Materials, PPT - deck, Working notes and Sample Scripts.

Decision (Run/Cancel) Date for this Course is Wednesday, April 12, 2017

Payment received by April 10
IEEE Members $230
Non-members $255

Payment received after April 10
IEEE Members $255
Non-members $275

http://ieeeboston.org/qa-testing-devops-automation/

Call for Articles

Now that the Reflector is all electronic, we are expanding the content the publication. One of the new features we will be adding are technical and professional development articles of interest to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional articles will be reviewed by the publications committee for suitability.The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to; ieeebostonsection@gmail.com

Advanced Embedded Linux Optimization

Time & Date: 6 - 9PM, Wednesdays, May 10, 17, 24, 31

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand debugging, profiling and testing high performance Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.
- To give students the confidence to apply these concepts to their next Embedded Linux project.

Course Schedule Day 1

Getting Started with Embedded Linux

Embedded Linux Training Overview
Terminology
Linux Versioning
The GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs
Linux References (Books and Online)
A Development Cycle Focused on Performance
A Basic Optimization Process

Basic Debugging Review

Embedded Applications Debug
GDB, GDB Server and the GDB Server Debugger
Other Debuggers
An Eclipse Remote Debug Example
Debugging with printk, syslog, syslogd and LTTng

System-Level Debug

System-Level Debug Tools
The /proc and /sys Filesystems
Basic Logging
KDB and KGDB
Crash Dumps and Post-Mortem Debugging

Debugging Embedded Linux Systems

Backend Debuggers
In-Circuit Emulators
Hardware Simulators
Analyzers

Course Schedule Day 2

Requirements Development

Performance Requirements
Derived Requirements

Testability and Traceability
Reviewing Requirements
Designing for Performance
Design for Test (DFT)
Agile Software Design
Software and Linux Decomposition
Memory Management
CPU and OS Partitioning
Design Reviews
Coding for Performance
Coding Standards and Consistency
Languages, Libraries and Open Source Components
Learning Magic Numbers
Letting Compilers Work For You
Global, Static and Local Variables
Code Reviews

Software Testing
Unit-Level Testing
System-Level Testing
Code Coverage Tools
gcov
Automated Testing
Some Embedded Linux Test Recommendations
DebugFS
Configuring DebugFS
DebugFS Capabilities
Advanced Logging
LogFS
Using Logwatch and Swatch
Using syslogd and syslog-ng
Tracing
ptrace and strace
New Tracing Methods
SystemTap
Ftrace, Tracepoints and Event Tracing
Tracehooks and utrace
Profiling
Basic Profiling
gprof and Oprofile
Performance Counters
LTTng
Another DDD Example
Manual Profiling
Instrumenting Code
Output Profiling
Timestamping

Course Schedule Day 3

Addressing Performance Problems
Types of Performance Problems
Using Performance Tools to Find Areas for Improvement
Application and System Optimization
CPU Usage Optimization
Memory Usage Optimization
Disk I/O and Filesystem Usage Optimization
Measuring Embedded Linux Performance
Some Ideas on Performance Measurement
Common Considerations
Uncommon Considerations
Using JTAG Methods
BootLoader Measurements
Boot Time Measurements
The Perf Tool
Origins of Perf
The Perf Framework
Perf Commands and Using Perf
Listing Events
Counting Events
Profiling with Perf
Static Tracing with Perf
Dynamic Tracing with Perf
Perf Reporting
Performance Tool Assistance
Recording Commands and Performance
System Error Messages and Event Logging
Dynamic Probes
Jprobes and Return Probes
Kernel Probes
Kexec and Kdump
Improving Boot Performance
Boot Time Optimization
The Linux Fastboot Capability
Building a Smaller Linux
Building a Smaller Application
Filesystem Tips and Tricks
Some Notes on Library Usage

Course Schedule Day 4

Improving Kernel Performance
Kernel Hacking
CONFIG_EMBEDDED
Configuring printk
Test Code
Configuring Kernel and IO Scheduling

Improving CPU Performance
Run Queue Statistics
Context Switches and Interrupts
CPU Utilization
Linux Performance Tools for CPU
Process-Specific CPU Performance Tools
Stupid Cache Tricks

Improving System Memory Performance
Memory Performance Statistics
Linux Performance Tools for Memory
Process-Specific Memory Performance Tools
More Stupid Cache Tricks

Improving I/O and Device Driver Performance
Disk, Flash and General File I/O

Improving Overall Performance Using the Compiler
Basic Compiler Optimizations
Architecture-Dependent and Independent Optimization
Code Modification Optimizations
Feedback Based Optimization
Application Resource Optimization
The Hazard of Trust
An Iterative Process for Optimization
Improving Development Efficiency
The Future of Linux Performance Tools

Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

Decision (Run/Cancel) Date for this Courses is Monday, May 1, 2017

Payment received by April 28
IEEE Members $395
Non-members $415

Payment received after April 28
IEEE Members $415
Non-members $435

http://ieeeboston.org/embedded-linux-optimization/

Introduction to Embedded Linux

Time & Date: 6 - 9PM, Mondays, March 20, 27, April 3, 10

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4 day course introduces the Linux Operating System and Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part of the course covers testing, booting and configuring of Embedded Linux systems including embedded cross-development and target board considerations.

Who Should Attend - The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives

• To provide a basic understanding of the Linux OS and the Eclipse IDE framework.
• To understand the complexities of Embedded Linux Distributions in embedded systems.
• To learn how to configure, boot and test Embedded Linux distributions and applications running on Embedded Linux target systems.
• To give students the confidence to apply these concepts to their next Embedded Linux project

Hardware and Software Requirements - The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ installation or prior knowledge of C-based Makefiles is useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials

• Linux Kernel Development by Robert Love
• Linux System Programming by Robert Love
• Embedded Linux Primer by Christopher Hallinan
• Pro Linux Embedded Systems by Gene Sally
• Embedded Linux Development Using Eclipse by Doug Abbott
• Linux Device Drivers by Jonathan Corbet et al
• Essential Linux Device Drivers by Sreekrishnan Venkateswaran

Course Schedule Day 1

Embedded Development Basics

Embedded Systems Characteristics
Embedded Real-Time Systems
Embedded Linux Systems and the Internet of Things (IOT)

Embedded Linux Basics

Embedded Linux Training Overview
Linux Terminology, History and Versioning

The Linux Community: Desktop & Embedded
Linux and the GPL
Linux References (Books and Online)

Getting Started in Embedded Linux

Kernel Source Code
Building the Kernel
Embedded Linux Kernels
Linux 2.6, 3.x and 4.x

Embedded Linux Kernel Overview

Process and Threads Management
Signals and System Calls
Synchronization, IPC and Error Handling
Timing and Timers
Memory Management and Paging
The I/O Subsystem: A Tale of Two Models
Modularization

Debugging

Process-Level and System-Level Debug
GDB, GDB Server and the GDB Server Debugger
Other Debug and Test Tools
An Eclipse Remote Debug Example
Advanced Debug with printk, syslogd and LTTng

System-Level Debug

System-Level Debug Tools
The /proc Filesystem
Advanced Logging Methods
KGDB and KDB
Crash and Core Dumps

Course Schedule Day 2

Process & Threads Management

What are Processes and Threads?
Virtual Memory Mapping
Creating and Managing Processes and Threads
Thread-Specific Data (TSD)
POSIX
The Native POSIX Threading Library (NPTL)
Kernel Threads

Signals in Embedded Linux

System Calls in Embedded Linux

Scheduling

Linux 2.4 and 2.6 Scheduling Models
The O(1) Scheduler
The Completely Fair Scheduler (CFS)

Synchronization

Via Global Data
Via Semaphores, Files and Signals
Condition and Completion Variables
Mutexes and Futexes

Inter-Process Communications (IPC)

Message Queues
Semaphores Revisited
Shared Memory
Pipes and FIFOs
Remote Procedure Calls
Networking

Course Schedule Day 3

Memory Management and Paging

Linux, Demand Paging and Virtual Memory
Allocating User and Kernel Memory
Mapping Device Memory
The Slab Allocator
The OOM Killer
Managing Aligned Memory
Anonymous Memory Mappings
Debugging Memory Allocations
Locking and Reserving Memory
Huge Pages
Memory in Embedded Systems

Error Handling

errno and perror
strerror and strerror_r
oops, panics and Segmentation Faults

Timing

How Linux Tells Time
Kernel, POSIX and Interval Timers
High-Resolution Timers (HRTs)

Sleeping

Sleep Waiting and Spinlocks
Using Timers
Embedded Recommendations for Timing

Modularization

Creating and Building a Module
A Simple Kernel Module
Module Loading

Module Dependencies
Module Licensing

Shared Libraries

A Shared Library Example
Static and Dynamic Libraries

Interrupt and Exception Handling

Bottom Halves and Deferring Work

Course Schedule Day 4

The I/O Subsystem: A Tale of Two Models

The UNIX Device Driver Model
The Standard I/O Interface
Major and Minor Numbers
Configuring the Device Driver

The Evolution of the New Device Driver Model

The Initial Object-Oriented Approach
Platform Devices, Busses, Adapters and Drivers
A Generic Subsystem Model

The Generic Subsystem Model in Detail

Subsystem Registration
The Probe and Init Functions
The Show and Store Functions
User Access via the /sys Filesystem
Configuring the New Device Driver
The udev Linux Application

Comparing the Two Driver Models

Advanced I/O Operations

Standard UNIX I/O Operations
Scatter-Gather and Asynchronous I/O
Poll/Select and Epoll
Memory-Mapped I/O
File Advice
I/O Schedulers and inotify

The Linux Boot Process

The Root Filesystem
Desktop Linux Boot
Bootloaders and U-Boot
Embedded Linux Boot Methods
Building and Booting from SD Cards

Managing Embedded Linux Builds

Configuring and menuconfig
Oldconfig, menuconfig, xconfig and gconfig
Building Custom Linux Images
Target Image Builders
The Open Embedded Project and the Yocto Project

System Architecture Design Approaches

Deploying Embedded Linux

Choosing and Building the Root Filesystem
Module Decisions
Final IT Work

Embedded Linux Trends

Development Trends
Monitoring Trends
Testing Trends

Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

Decision (Run/Cancel) Date for this Courses is Friday, March 10, 2017

Payment received by March 8
IEEE Members $400
Non-members $430

Payment received after March 8
IEEE Members $430
Non-members $455

http://ieeeboston.org/introduction-embedded-linux-2/

Embedded Linux BSPs and Device Drivers

Time & Date: 6 - 9PM, Wednesdays, April 12, 19, 26, May 3

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the development of Embedded Linux Board Support Packages (BSPs), Device Drivers and Distributions. The first part of the course focuses on BSP and Software Development Kit (SDK) development in an Embedded Linux context with a focus on application performance measurement and improvement. The latter part of the course covers Embedded Linux Device Driver development including key device driver decisions and deployment considerations for Embedded Linux BSPs.

Who Should Attend - The course is designed for real-time engineers who are developing Embedded Linux BSPs and Device Drivers for Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Linux BSP and Device Driver development.

Course Objectives

• To gain an understanding of the complexities of BSP and SDK development and their uses in Embedded Linux systems.
• To provide a basic understanding of the Linux I/O Subsystem and the Device Driver Models provided with Embedded Linux distributions.
• To gain an in-depth understanding of character-based device drivers in Embedded Linux
• To understand key device driver subsystems including relatively slow I/O interconnects such as I2C, SPI and USB as well as high-speed interfaces such as USB 3.0 and PCIe
• To give students the confidence to apply these concepts to their next Embedded Linux project.

Course Schedule Day 1

Getting Started with Embedded Linux
Linux and the GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs
Linux References (Books and Online)

Embedded Linux BSP Development Basics
BSP Requirements
U-Boot and Bootloader Development
Basic BSP Development
Files and Filesystem Support
The I/O Subsystem: Talking to Hardware
Memory Management and Paging
Error Handling in Embedded Linux BSPs
Timing and Timers
Interrupt Handling in BSPs
BSP Deployment Issues and Practices

Embedded Linux SDK Basics
The 3 Pieces of an SDK
Embedded Linux Distributions
The GNU Compiler Collection (GCC)
Other Embedded Linux Development Tools
Library Support
Glibc and Alternatives
SDK Deployment and Support

Debugging
GDB, GDB Server and the GDB Server Debugger

Other Debug Tools
An Abatron Board Bring-Up Example
An Eclipse Remote Debug Example
Advanced Debug with printk, syslogd and LTTng
System-Level Debug
System-Level Debug Tools
The /proc Filesystem
Advanced Logging Methods
KGDB and KDB
Crash Dumps

Course Schedule Day 2

Configuring Embedded Linux
Config Methods
Config Syntax
Adding Code to the Linux Kernel
Booting Embedded Linux
The Linux Boot Process
NFS and RAMdisk Booting
Root and Flash File System Development
Building the RAMdisk
Busybox Development
Testing and Debug of Embedded Linux BSPs
Kernel Debug and Kernel Probes
Kexec and Kdump
The Linux Test Project (LTP)
Performance Tuning Embedded Linux BSPs
User Mode Linux and Virtualization
Measuring Embedded Linux BSP Performance
Common Considerations
Uncommon Considerations
BootLoader Optimizations
Boot Time Measurements
Effective Memory and Flash Usage
Filesystem Performance Issues
Some Ideas on Performance Measurement

Course Schedule Day 3

The Original Device Driver Model
The fops struct and Char Drivers
The inode and dentry structs
Major and Minor Numbers
Embedding Channel Information
Deferring Work
The /proc Filesystem
Configuring the Device Driver
Modularization Revisited
The New Device Driver Model
An Object-Oriented Approach
Platform Devices and Drivers
Subsystem Registration
The Probe and Init Functions
The Show and Store Functions
The /sys Filesystem
Configuring the New Device Driver

Comparing the Two Driver Models

The Flattened Device Tree (FDT)
openBoot and its Effect on Embedded Linux
The Device Tree Script (dts) File
The Device Tree Compiler (dtc)
The Device Tree Blob (dtb) File
Building a dtb File
Hybrid Device Drivers
Other fops Functions
The Need for Ioctl
A Simulated Char Device Driver
The SIM Device Driver
Initialization
Open and Close
Read and Write
The /proc Driver Interface
MMAP Support

Course Schedule Day 4

Linux Device Driver Subsystems
Serial Drivers
The RTC Subsystem
Watchdogs
I2C & SPI
Block Devices
PCI
USB
VME
Video
Sound
What's Missing?
Memory Technology Devices

What is an MTD?
NAND vs NOR Flash Interfaces
The Common Flash Interface (CFI)
Driver and User Modules
Flash Filesystems
Drivers in User Space
Accessing I/O Regions
Accessing Memory Regions
User Mode SCSI, USB and I2C
UIO
High-Speed Interconnects
PCIe
GigE
iSCSI
Infiniband
FibreChannel
Serial RapidIO
Debugging Device Drivers
kdb, kgdb and JTAG
Kernel Probes
Kexec and Kdump
Kernel Profiling
User Mode Linux and Kernel Hacking
Performance Tuning Device Drivers
Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at LynuxWorks, Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based software development tools, training and consulting services for the embedded systems market.

Decision (Run/Cancel) Date for this Courses is Monday, April 3, 2017

Payment received by March 31
IEEE Members $395
Non-members $415

Payment received after March 31
IEEE Members $415
Non-members $435

http://ieeeboston.org/embedded-linux-bsps-device-drivers/

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YouTube: https://www.youtube.com/user/IEEEBostonSection

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