

THE REFLECTOR

ISSUE #12 DECEMBER 2017

NEW ONLINE COURSE - EMBEDDED LINUX BSP AND DEVICE DRIVERS

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INDUSTRY
APPLICATIONS
SOCIETY CHAPTER
MEETING

P.4

YOU ARE INVITED TO SUBMIT AN ARTICLE P.5

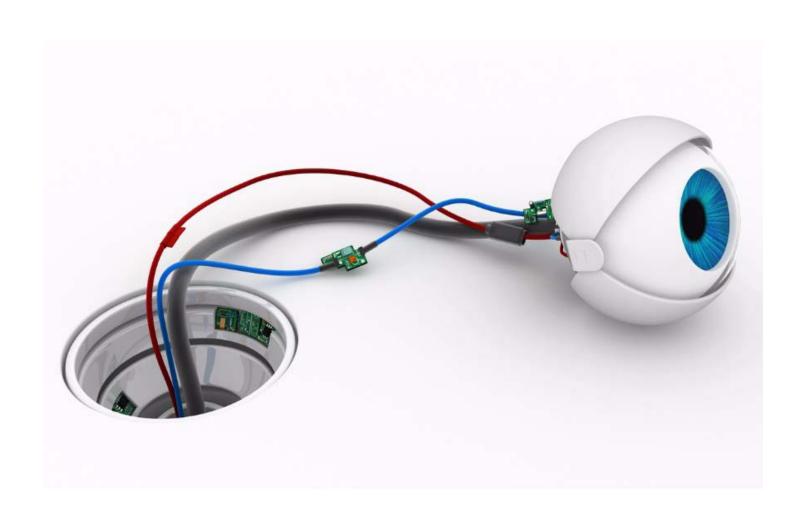




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Happy New Year!

Greg Walson, 2018 IEEE Boston Section Chair

Each year the incoming Chair uses this Editorial space to reflect on the year before and set their goals for the new year. In spite of having served on the Executive Committee in one function or another for almost 10 years, I have had a hard time finding something inspiring to say that hasn't been said before. My wife often asks me why I continue to volunteer for the Boston Section, and I'm sometimes at a loss to explain it to her.

Having reflected on the matter, I think it comes down to community. For me the IEEE represents a set of communities. We have online communities that discuss current technology. We have communities of people who regularly attend the same Technical Society meetings. And we have the many communities of volunteers that give of their time to keep the Section and its various Societies operating.

For those of us with a technical bent, the IEEE is often the only community outside work where we can be assured of interacting with others like us. In

this era where facts are disregarded if they aren't convenient to an argument, having a community of people who discover and use facts for their living is more important than ever.

It has been said before, but it bears repeating: the IEEE is what you make of it. If you simply use a corporate membership to access technical standards, then you will not feel a sense of community attached to the IEEE. Attending Society meetings and conferences produces a greater level of connection to the community. But volunteering provides the greatest connection.

We all make time for the things that are important to us. I hope that the IEEE and the Boston Section are important to you. If they aren't, then please tell us what we can do to improve. Or better yet, come lend a hand, and help us make the Section better.

Happy New Year!

IEEE Boston Section Social Media Links:

Twitter: https://twitter.com/ieeeboston

Facebook: https://www.facebook.com/IEEEBoston

YouTube: https://www.youtube.com/user/IEEEBostonSection

Google+: https://plus.google.com/107894868975229024384/

LinkedIn: https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about

Education, and Signal Processing Societies- 11:30AM, Monday, 4 December

Current Research Opportunities

WHEN: Monday, December 4th from 11:30 am to 1:00 pm – Lunch provided

WHERE: Science and Engineering Complex, Main Atrium, 200 College Avenue, Medford, MA 02155

REGISTER: https://tufts.qualtrics.com/jfe/form/SV_aasNfC6BRe4Gvdj (space is limited)

The School of Engineering invites IEEE members to meet representatives from MITRE on Monday, December 4th from 11:30 am to 1:00 pm. Dr. Karen Panetta, Dean of Graduate Education for the School of Engineering, will be hosting a lunch with leaders from MITRE to discuss research and other opportunities. Following presentations from MITRE employ-

ees, participants will have the opportunity to speak one-on-one with company representatives and exchange information.

We encourage students to bring copies of their resumes and be prepared to discuss their research interests.

MITRE is a not-for-profit company that operates multiple federally funded research and development centers. MITRE provides innovative, practical solutions for some of our nation's most critical challenges in defense and intelligence, aviation, civil systems, homeland security, the judiciary, healthcare, and cybersecurity. MITRE has two principal locations in Bedford, Massachusetts and McLean, Virginia.

Industry Applications Society - 6:00PM, Tuesday, 5 December

Applying Probabilistic Risk Assessment to Mission Critical Power System Design

Speaker: Neal Dowling Senior Engineer, MTechnology Inc.



I will begin by examining the definition of "risk": the "risk" associated with an event is a function of the likelihood and the consequences of that event. After a brief discussion of "consequences", I will dive into how to assess "likelihood". There will be a brief discussion of IEEE Standards that are useful in risk assessment. I

will work through a simple but meaningful real-world example. To conclude, I will provide links to some resources for further study, and answer questions about risk assessment.

Neal Dowling is Senior Engineer at MTechnology, Inc. MTechnology has performed PRA studies for clients worldwide, including data center designers, electric utilities, financial services firms, hospitals, medical facilities, owner/operators of mission critical facilities, and manufacturers serving the 7x24 uptime industry. Neal is a Senior Member of the IEEE and Vice Chair of the IEEE 3006 Working Group. A graduate of the Massachusetts Institute of Technology (SB 1974, SM 1979), he also has an extensive background in medical device development

Location: Bertucci's Kitchen & Bar, Medford 4054 Mystic Valley Parkway, Medford, MA 02155. Refreshments start at 6:00PM . Talk commences at 6:30PM

Free and Open to the Public. RSVP is appreciated. If you have any questions, please contact Ozgur Cosar (765-543-9172)

Call for Articles

Now that the Reflector is all electronic, we are expanding the content the publication. One of the new features we will be adding are technical and professional development articles of interest to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional articles will be reviewed by the publications committee for suitability. The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to; ieeebostonsection@gmail.com

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Comprised of Engineers, scientists and professionals in the electrical and computer sciences and engineering industry

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Entrepreneurs' Network - 6:30PM, Tuesday, 5 December

IP Protection and Legal Issues for Early Stage Companies

Meeting Location – Microsoft Technology Center, 5 Wayside Road, Burlington, MA

This meeting is co-sponsored by IEEE Technology and Engineering Management Society, Boston Chapter.

PRE-MEETING DINNER at 5:15 PM (sharp) at Bertucci's, Waltham.

The legal environment is constantly changing because of new laws and evolving interpretations of existing laws and regulations. Founders and executives of early stage companies have to address numerous legal questions in this changing environment; for instance:

- How to use provisional, utility, and design patents, trademarks, and other IP protections
- How copyrights, and trade secrets can be used to protect intellectual property and build value for investors and employees
- Where to incorporate, how to apportion founders equity and granting employee stock options, restricted stock and other equities
- How employer/employee agreements can benefit both investors, founders, and employees. Employee agreements may include terms of employment, compensation including benefits and independent contractor agreements.

Our panel of legal experts will address these fundamental issues that early stage companies must consider during their earliest days in order to lay a strong legal foundation for success.

Agenda:

- 6:30 7:30 PM Registration & networking
- 7:30 7:40 PM ENET Chairman's announcements
- 7:40 7:55 PM E Minute Up to 3 Startup companies' presentations
- 7:55 8:45 PM 3 expert speakers on the night's topic
- 8:45 9:00 PM Audience / Speakers Q & A
- 9:00 9:30 PM Final networking includes meeting presenting speakers

A question and answer session follows the presentation, and panelists will be available afterwards for responses to individual questions.

Speakers:



Jeremy Cohen, Gesmer Updegrove Jeremy Cohen is an attorney at Gesmer Updegrove, LLP, a firm specialized in the representation of emerging technology companies. His focus is on business creation, development, transactions, financings, and assisting with any other advice you need to help your business grow. Jeremy's experiences and back-

ground have helped him develop a practice that is broad as well as deep, including: Business formation and organization: advising start-ups on how to best begin their business while looking to future growth. Mergers & Acquisitions: from spin-outs and carve-outs to complex transaction structures or outright sales of companies, Jeremy has experience in a variety of transaction structures and can bring insight and know-how to any situation. Financings: Whether the funding is coming from a bank, a professional investor or a relative, Jeremy can help guide the process to a successful financing.



Mike Attisha, Associate, Wolf Greenfield & Sacks

Mike Attisha is an attorney at Wolf Greenfield, a boutique law firm that is focused entirely on intellectual property. Mike counsels clients on their patent portfolio in a wide range of technology areas, including electronics, additive fabrication (3D printing), display technologies (LCD, OLED, electrophoretic), software, semicon-

ductors, optics, medical devices, electronic music, automated hardware testing, and signal processing. He has an extremely broad technical knowledge drawn

largely from his experience working in experimental physics and as a software consultant. Prior to joining Wolf Greenfield, Mike worked at Ab Initio Software assisting clients with their enterprise data processing applications. During his graduate studies at Brown University, Mike worked on the Cryogenic Dark Matter Search (CDMS) experiment located a half mile underground in northern Minnesota.



Moderator and Co-Organizer: Bob Weber, Managing Director, Patent Kinetics, LLC

Robert Weber is a successful intellectual property professional, inventor, serial entrepreneur, management consultant, and senior executive. Presently, he is Managing Director, Patent Kinetics, LLC, a company that helps entrepreneurs and patent owners build and monetize valuable patent portfolios.

Weber is an inventor with 28 issued US patents and a number of foreign counterparts assigned to Intertrust Technologies, where he served as SVP Business and Technology Strategy, 1996-1999. The Intertrust portfolio was characterized in the Wall Street Journal as a once in a generation billion dollar licensing opportunity. (Intertrust is presently a joint venture of Sony and Philips.) Weber has also been a Principal Consultant at Northeast Consulting Resources, Inc. At NCRI, his consulting practice focused on the intersection of business and technology. Weber divides his time between Boston and Silicon Valley. He is a former Vice Chair, Programs, of the Boston Entrepreneurs Network and is a member of the Silicon Valley Chapter of the Licensing Executives Society.

Co-Organizer: William R. Byrnes

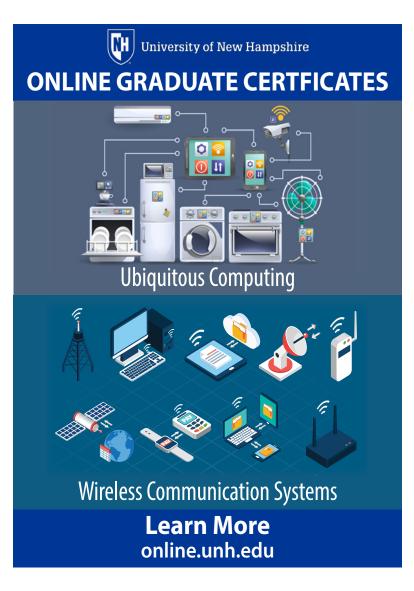
Bill's legal practice assists entrepreneurial companies with the legal issues they face with a focus on day-to-day commercial issues involving customers, vendors, and other third party relationships. Bill received his undergraduate degree in English Literature and Creative Writing from Boston University, a J.D. from Suffolk University Law School, and a L.L.M. degree in Taxation from Boston University Law School, Graduate Tax Program. He is also a Boston Entrepreneurs' Network board member.

E-Minute Presentations will be given at the start of the meeting. These very short presentations enable young startup entrepreneurs to gain experience in presenting their summary business plans to expert panels and audiences.

Directions: Constant Contact is adjacent to RT 128 / 95 at Exit 28B.

See: http://www.constantcontact.com/about-constant-contact/office-location-waltham.jsp

Reservations: ENET Constant Contact meetings are free to ENET members and \$20 for non-members. No reservations are needed for the premeeting dinner. To expedite sign-in for the meeting, we ask that everyone -- members as well as non-members -- pre-register for the meeting online. Pre-registration is available until midnight the day before the meeting. If you cannot pre-register, you are welcome to register at the door.



IEEE Boston Section Online Courses:

(Students have 90 day access to all online, self-paced courses)

Verilog101:Verilog Foundations

Full course description and registration at , http://ieeeboston.org/verilog-101-verilog-foundations-online-course/

System Verilog 101: Design Constructs

Full course description and registration at , http://ieeeboston.org/systemverilog-101-sv101-design-constructs-online-course/

System Verilog 102: Verification Constructs

Full course description and registration at , http://ieeeboston.org/systemverilog-102-sv102-verification-constructs-online-course/

High Performance Project Management

Full course description and registration at , http://ieeeboston.org/high-performance-project-management-online-course/

Introduction to Embedded Linux Part I

Full course description and registration at , http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/

Embedded Linux Optimization - Tools and Techniques

Full course description and registration at , http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/



Embedded Linux Board Support Packages and Device Drivers

Full course description and registration at , http://ieeeboston.org/embedded-linux-bsps-device-drivers-line-course/

Software Development for Medical Device Manufacturers

Full course description and registration at , http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/

Fundamental Mathematics Concepts Relating to Electromagnetics

Full course description and registration at , http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/

Reliability Engineering for the Business World

Full course description and registration at , http://ieeeboston.org/reliability-engineering-business-world-line-course/

Computer and Geoscience & Remote Sensing Societies and GBC/ACM – 7:00PM, Thursday, 7 December

Probabilistic Programming

Theo Giannakopoulos, BAE Systems



In this talk I will present a rapidly maturing approach to machine learning and data science called probabilistic programming. Probabilistic programming languages enable the use of machine learning by programmers and domain specialists without experience in the creation of specialized machine learning algorithms. However, the

combination of probability and program semantics makes reasoning about probabilistic programs challenging, even for probabilistic programming language implementers. I will outline an approach to reasoning about probabilistic programs using techniques from traditional programming language theory.

Theo Giannakopoulos is a Principal Research Engineer at BAE Systems. He led the development of the Tempest programming language for BAE's SAFE project on the DARPA CRASH program and was the Principal Investigator for BAE's Open Probabilistic Programming

Platform project for the DARPA PPAML program. Prior to joining BAE Systems, he developed secure back-of-fice systems for financial and e-commerce companies. He received his Master's degree in Computer Science at Worcester Polytechnic Institute (WPI) as part of the Applied Logic and Security group under the supervision of Prof. Daniel Dougherty, researching languages for the formal specification of security policies and policy combinators.

This joint meeting of the Boston Chapters of the IEEE Computer and GRSS Societies and GBC/ACM will be held in MIT Room 32-G449 (the Kiva conference room on the 4th floor of the Stata Center, building 32 on MIT maps). You can see it on this map of the MIT campus.

Up-to-date information about this and other talks is available online at http://ewh.ieee.org/r1/boston/computer/. You can sign up to receive updated status information about this talk and informational emails about future talks at http://mailman.mit.edu/mailman/listinfo/ieee-cs, our self-administered mailing list.

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Nuclear and Plasma Science Society and Boston University IEEE HKN- 5:00PM, Thursday, 7 December

Parallel Processing of Compressed Graphs with Ligra+

Speaker: Katie Lewis, MIT

Graph algorithms span many applications from biological network to social network analysis. With the continuous growth in data, compression has become increasingly important for reducing the space and cost of large-scale graph analytics. In this talk, I will give an overview of several integer compression techniques, such as StreamVbyte, currently used in the literature. I will also discuss how to apply these techniques towards compressing graphs and speeding up algorithms in the graph processing framework, Ligra+.

Katie Lewis is a graduate student conducting research in Computer Science and Artificial Intelligence Laboratory (CSAIL) at MIT. Her research

with Professor Julian Shun focuses on the theory and implementation of parallel graph processing frameworks and algorithms. In particular, her current work incorporates integer compression techniques into the graph processing framework Ligra+to reduce the space and computation requirements of large-scale graph processing. When Katie Lewis studied at Boston University for a BS in Computer Engineering, she served as President of BU IEEE/IEEE-HKN. She is elected as a student governor to the board of IEEE HKN for 2018."

Meeting Location: 5:00 - 6:30 PM. Boston University, Room EPC 207, 750 Commonwealth Avenue, Boston, MA 02215.

Women in Engineering – 1:00PM, Saturday, 16 December

Holiday Lunch

Women in Engineering will have its annual Holiday Lunch on Saturday, December 16. Meeting Location: Bertucci's, 5 Cambridge Park Drive, Cambridge, MA 02140.

Reliability Society – 5:30PM, Wednesday, 13 December

Trends and Prospective in Risk and Reliability Engineering Research

Mohammad Pourgol-Mohammad, Ph.D.



This is the IEEE Boston Reliability chapter December Annual Past Chairs Dinner Meeting. IEEE members & non-members are welcome, and the meeting and food are free of charge, but registration is required in advance, so we can finalize food and drink arrangements.

This meeting is limited to 40 members and guests. You MUST be registered to attend. Please Register by COB Thursday, December 7th so we can finalize the arrangements!

This talk will highlight current and promising directions in the fields of Reliability Engineering and Risk Assessment. Leading topics such as research on the fundamental sciences that underpin risk and reliability technologies, challenges in reliability of ultra-complex systems of interacting hardware and software, utilization and processing of large data and machine learning algorithms, advances in system-level prognostics and health monitoring, and new approaches to integrate physics of failure and traditional reliability assessment methods.

Mohammad Pourgol-Mohammad, Ph.D. of ASQ RRD

Dr. Mohammad Pourgol-Mohammad is a safety/reliability analyst in multidisciplinary systems analysis and an Associate Professor of Reliability Engineering with Sahand University of Technology (SUT), Tabriz-Iran. He received his Ph.D in Reliability Engineering from University of Maryland (UMD), and holds one M.Sc

degree in Nuclear Engineering and another in Reliability Engineering from UMD. His undergraduate degree was in Electrical Engineering. Dr Pourgol-Mohammad has more than 15 year of work experience including research and teaching in safety applications and reliability engineering at various institutions including FM Global, Goodman Manufacturing, UMD, Massachusetts Institute of Technology (MIT), International Atomic Energy Agency (IAEA), University of Zagreb-Croatia, USNRC and INEL. He is a senior member of ASQ, ASME, IEEE (2008-2010) and ANS and member of several technical committees and a registered Professional Engineer (PE) in Nuclear Engineering in States of Maryland and Massachusetts. He is a certified reliability engineer (ASQ CRE). He has authored more than 80 papers and reports on his research. His efforts have been appreciated with several awards and recognition.

Email: mpourgol@gmail.com

This meeting will be held on Wednesday, November 8, 2017 at 3 Forbes Road, Lexington, MA.

5:30-6:00: Sign In & Personal Networking

6:00-6:45: Catered dinner, refreshments, dessert

6:45-7:00: Greetings, Election Results, Year in review

Guest Presenter Introduction

7:00-8:00 Dr. Mohammad Pourgol-Mohammad - Associate Professor of Reliability Engineering SUT, Tabriz-Iran

8:00-8:15 Q&A session, meeting adjourns

Meeting Location: 3 Forbes Rd, Lexington, Massachusetts

Photonics Society and co-sponsoring Nuclear & Plasma Science Society –6:30PM, Thursday, 14 December

High-Resolution Retinal Imaging – Visualizing Cellular Structures In The Living Eye

Dr. Mircea Mujat, Physical Sciences Inc., Andover, MA



Scanning laser ophthalmoscopy (SLO) and optical coherence tomography (OCT) provide information on cellular and sub-cellular structures in the living eye when enhanced with adaptive optics (AO) capabilities. AO enhances transverse resolution and confocal sectioning capabilities by detecting and correcting ocular aberrations in real-time and has become a valuable tool for vision re-

searchers to explore the structural and functional aspects of vision and its disruption by disease. While AO has yet to fully transition from research lab to clinic, OCT is now a standard diagnostic procedure for glaucoma, macular holes, macula edema, retinal detachments, and other retinal pathologies. Simultaneous use of the two complementary imaging modalities provides a powerful comprehensive modality to investigate the eye.

AO systems use a wave-front sensor to sense ocular aberrations that arise primarily from the cornea, crystalline lens, and tear film, and correct them using a deformable mirror in a closed-loop manner. AO has recently achieved success in a range of applications in ophthalmology in which the building blocks of retinal microstructures such as cone photoreceptors, rods, RPE cells, blood cells, and microvasculature need to be identified, counted, and mapped properly. In this presentation we will review the state-of-the-art capabilities in high-resolution retinal imaging. PSI designed, developed, and tested a number of compact platforms combining the power of AO with SLO or line-scanning technology (LSO), and OCT for human and animal eye imaging. Our compact, simplified research instruments can be used by ophthalmologists, optometrists, and vision scientists and will facilitate the introduction of this technology and the development of new techniques to detect and treat retinal diseases.

Although AO-enhanced confocal SLO enables high-resolution imaging of the eye fundus, the capillaries are essentially transparent and, in standard, bright-field AO imaging can be difficult to visualize, except for the specular glint from blood cells coursing through them or the shadow they cast on deeper layers. Recently, it was shown that by using a larger, offset pinhole in the AO detection unit, images

that capture multiply scattered light (as opposed to direct backscatter) can reveal the tiny retinal vasculature network of the human retina with unprecedented clarity. Offset aperture/split detector/quad simultaneous imaging modalities will also be presented as the most recent developments in high-resolution retinal imaging.

Mircea Mujat obtained his Ph.D. in Optics in 2004 under the supervision of Prof. Aristide Dogariu at the School of Optics/CREOL, University of Central Florida. As a graduate student, he developed theoretical models and experimental techniques for polarimet¬ric characterization of random electromagnetic fields, and for analyzing the signature of various random media. Between 2004 and 2007 Mircea joined Harvard Medical School and Wellman Center for Photomedicine - MGH as a Research Fellow, working with Prof. Johannes de Boer on ophthalmic investigations using OCT. He then joined the Biomedical Optics Group at PSI. His research interests at PSI are in ophthalmic imaging, medical instrumentation, adaptive optics, optical coherence tomography, and polarization imaging. Mircea is a member of the OSA, SPIE and ARVO.

This meeting begins at 6:30 PM Thursday, December 14th, 2017 and will be located 3 Forbes Road, Lexington, MA, 02420. Note this is a satellite location ~1.5mi away from MIT Lincoln Laboratory. The meeting is free and open to the public. All are welcome. Prior to the seminar there will be social time and networking from 6:30 – 7:00PM. Dinner will also be provided. The seminar will begin at 7:00PM. For more information contact Ajay Garg, IEEE Photonics Society Boston Chapter chair at

ajay.sinclair.garg@ieee.org, or visit the IEEE Photonics Society Boston Chapter website at www.bostonphotonics.org.

Directions to Forbes Rd Lincoln Laboratory: (from interstate I-95/Route 128)

- Take Exit 30B onto Marrett Rd in Lexington Merge into left lane
- Make the first Left onto Forbes Rd.
- Proceed straight through the small rotary and enter the parking lot.
- The entrance is by the flags.

Life Members Affinity Group - 4:00PM, Wednesday, 13 December

A Little Bit More About Big Data

Jim Issak

Big Data just keeps getting bigger, and it may be that we have gone past a tipping point on applications.

What if you could cross connect thousands of data points on every person in the U.S.?

What f you could run human medical/psychological tests on thousands or millions of volunteers without any "human subject review committee?".

What if you could target custom ads at each individual, knowing their preferences, purchasing history, and personality traits?

What if examining a few pictures of a persons face you would have a high probability of accurately associating them with a capital offense?

What if connecting the gun purchasing database into other data stores could identify highly likely suicide or violent offenders?

All but the last one of these potential applications is "so last year." It is time to be aware of the uses, and potential abuses of big data, and consider what it means for our future.

Jim Isaak is past president of the IEEE Computer Society and past Vice President of the IEEE Society on Social Implications of Technology. Jim also is the primary@ blogger for

"SocietyAndTechnolgy.org" (aka IEEESSIT.org). Jim has been contemplating data since it was little, and last year's take on these issues does not reflect what the bouncing baby is now doing.

The meeting will be held at the Lincoln Lab Main Cafeteria, 244 Wood Street, Lexington, MA at 4:00 PM. Please use the Wood Street Gate. For directions go to http://www.ll.mit.edu/

Refreshments will be served at 3:30 PM, and a video on Big Data will be shown starting at 3:50.

For other information, contact Lori Jeromin 781-981-4152.

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Last Notice Before Course Begins, Please Register Now!!!)

Determining and Communicating Project Value Return on Investment (ROI)

ROI Value Modeling ™ for Decision Making

Communicate Right, Reliable, and Responsible REAL ROI Business Cases

Date & Time: Wednesday, December 12; 8:30AM - 5:00PM (7.5 hours of instruction!)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

Companies are demanding reliable financial measures of proposed projects' value. Yet, project managers often don't know how to identify, calculate, or communicate a project's REAL ROI™ (Return on Investment). Traditional ROI calculations increasingly are being criticized for telling only part of the necessary story. The difficulty afflicts all types of projects but often is greatest in areas like IT, where benefits may seem intangible and frequent overruns impact estimates' credibility. This interactive workshop reveals 22 pitfalls that render common ROI determinations meaningless and shows instead how to identify full-story key effects on revenue and expense variables, reliably quantify tangible and intangible costs and benefits, and convincingly communicate the business value of project investments. Exercises enhance learning by allowing participants to practice applying practical techniques to a real case.

PARTICIPANTS WILL LEARN:

- * The financial information that business decision makers need and demand.
- * ROI and related calculations, strengths, weaknesses, and common pitfalls.

- * Using ROI Value Modeling™ and Problem Pyramid™ to fully identify relevant costs and benefits.
- * Quantifying intangibles, risk, flexibility, and opportunity.
- * Professionally presenting credible business value measurements so people pay attention.

WHO SHOULD ATTEND: This course has been designed for business, systems, and project managers as well as analysts, implementers, users, and others who must know the return on project investments.

OUTLINE

WHAT MONEY HAS TO DO WITH IT

Project Manager role with regard to ROI Situations demanding ROI, their issues Difficulty of making convincing arguments Linking ROI to the business case Value Modeling™ Relationship Diagram Investment vs. expense Justification vs. objective analysis Meanings of "It costs too much" Total Cost of Ownership (TCO) Factors other than cost to be considered

Costs and benefits, revenues vs. expenses Return on Investment (ROI) calculations Net present value, discounted cash flow Payback period, annualized return Internal rate of return (IRR), hurdle rate 'Telling the story' not just ROI calculations Failing to quantify 'intangibles' and risk Scenario approach to showing benefits Mistakenly thinking ROI does not apply

DETERMINING MEANINGFUL BENEFITS

Why it's important to find the benefits first Treacy's model of 5 revenue categories Problem Pyramid™ to find requirements Decision variable clarification chain Putting a dollar value on intangibles Opportunity, innovation, and flexibility Mandates, project with no apparent benefits

ESTIMATING CREDIBLE COSTS

Problem Pyramid™ ties costs to value
Basing costs on implementation of design
Business case framework
Basic formula for estimating costs
Main causes of poor estimates
Top-down vs. bottom-up techniques
Risks that afflict ROI calculations
Three measurable ways to address risks
Best-, worst-, most-likely-case scenarios
Sources of parameter sizing assumptions
Defining a reasonable scenario for success
Getting reliable cost and revenue amounts

REPORTING AND MONITORING

Single vs. multiple scenario presentation Applying apples vs. apples, when you can't Scenario assumptions and parameters No change vs. proposed scenarios' ROIs Measuring intangibles' monetary effects
Continual, step-wise, and one-time changes
Percentage-likelihood impact adjustments
Presenting with spreadsheets
ROI Value Dashboard™ modeling tool
Caution about commercial ROI calculators
Using value modeling to improve decisions
Dashboard and scorecard-type notification
Capturing, calibrating with project actuals
Adjusting appropriately during project

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, Discovering REAL Business Requirements for Software Project Success, he regularly works with and trains business and systems professionals.

Decision (Run/Cancel) Date for this Courses is Wednesday, December 6, 2017

Payment received by Nov. 29

IEEE Members \$220 Non-members \$245

Payment received after Nov. 29

IEEE Members \$245 Non-members \$265 Last Notice Before Course Begins, Please Register Now!!!)

Making You a Leader - Fast Track

Become the Leader You Want and Need

Date & Time: Monday, December 11; 8:30AM - 5:00PM (7.5 hours of instruction!)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

We do projects to make change. Yet, change will not occur without leadership, and leaders are rare. Leaders make others want to do what the leader wants done. Leaders cause ordinary people to achieve extraordinary things. Managing is not the same as leading, and titles do not make leaders. Seminars can teach you to manage, but they cannot teach you to be a leader. Rather, making a leader takes special techniques—such as our personal development clinics—that can change deepseated behaviors learned over a lifetime.

However, since clinics usually last about ten weeks, this mini-clinic was devised as a more convenient alternative. This format places responsibility upon the participant to carry out an extended informal follow-on program after completion of the formal seminar workshop session.

During the follow-on period, the participant uses time-condensed methods that simulate the lifetime learning which makes a leader. Therefore, commitment to carrying out these exercises is essential for successful transformation.

PARTICIPANTS WILL LEARN:

- Leadership characteristics and practices that are essential for project and personal success.
- Differences between management and leadership, how they conflict, and why leaders are so rare.

- Behaviors leaders use to influence others, up and down, to want to do what the leader wants them to do
- Special techniques personal development clinics use to change lifetime learning and make leaders.
- How to employ those special techniques in a follow-on mini-clinic to develop the leadership skills they need to make their projects successful.

WHO SHOULD ATTEND: This course has been designed for business and systems professionals who want to improve their ability to lead and influence other people.

LEADERSHIP CHARACTERISTICS & ROLE

How leadership looks and feels
Management vs. leadership
Leadership components of project success
Basic leadership practices; power sources
Real change leaders in organizations

TEAMS AND LEADERSHIP

Everyone feels leadership is lacking
Everyone thinks s/he is a leader
Results, not actions or intent
Workgroups, teams, and leaders
Situational leadership styles
Coaching and sports analogies to projects

Hierarchy of needs effects on projects
Hygiene factors vs. motivators
Helping project players get their rewards
Influencing up and down without authority
Inspiring the extra efforts projects need
Energizing the project team

SHARED VISIONS

Relating values and vision to projects Getting others to embrace one's vision Developing a motivating project vision

WHERE AND HOW LEADERS ARE MADE

Born or made? How do we know?
Habits of thought that affect project success
Overcoming self-limiting lifetime learning
Leader's critical success factors
Traditional education doesn't make leaders
Special way—personal development clinics

SETTING AND ACCOMPLISHING GOALS

S.M.A.R.T. goals for self and project Action plans to achieve your goals Visualizing and emotionalizing

DEFINING THE FOLLOW-ON PROGRAM

Clarifying project leadership objectives
Breaking into prioritized subgoals
Establishing rewarding daily achievements
Special techniques to change habits

CARRYING OUT THE MINI-CLINIC

Working with a follow-up support structure Mapping results regularly to goals Objectively recording leadership changes Self-leadership through the process

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, Discovering REAL Business Requirements for Software Project Success, he regularly works with and trains business and systems professionals.

Decision (Run/Cancel) Date for this Courses is Monday, December 4, 2017

Payment received by Nov. 27

IEEE Members \$220 Non-members \$245

Payment received after Nov. 27

IEEE Members \$245 Non-members \$265

http://ieeeboston.org/making-leader-fast-track-become-leader-want-need/



Embedded Linux Board Support Packages and Device Drivers (Online Edition)



Students have access to this self-paced course for 90 days!!

Registration Fee: 350

Course Summary - This video course provides advanced training in the development of Embedded Linux Board Support Packages (BSPs) and Device Drivers. The first part of the course focuses on BSP and Software Development Kit (SDK) development in an Embedded Linux context with a focus on application performance measurement and improvement. The latter part of the course covers Embedded Linux Device Driver development including key device driver decisions and deployment considerations for Embedded Linux BSPs.

Who Should Attend - The course is designed for real-time engineers who are developing Embedded Linux BSPs and Device Drivers for Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Linux BSP and Device Driver development.

Course Objectives

- To gain an understanding of the complexities of BSP and SDK development and their uses in Embedded Linux systems.
- To provide a basic understanding of the Linux I/O Subsystem and the Device Driver Models provided with Embedded Linux distributions.
- To gain an in-depth understanding of character-based device drivers in Embedded Linux
- To understand key device driver subsystems including relatively slow I/O interconnects such as I2C, SPI and USB as well as high-speed interfaces such as Ethernet, USB 3.0 and PCIe

 To give students the confidence to apply these concepts to their next Embedded Linux project.

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at LynuxWorks, Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based software development tools, training and consulting services for the embedded systems market.

Course Schedule

Getting Started with Embedded Linux

Embedded Linux Training Overview Linux Terminology, History and the GPL Building the Kernel Source Code Embedded Linux Kernels BSPs and SDKs

Linux References (Books and Online)

BSP Requirements

U-Boot and Bootloader Development Embedded Linux BSP Development Basics

Basic BSP Development

Files and Filesystem Support

The I/O Subsystem: Talking to Hardware

Memory Management and Paging

Error Handling in Embedded Linux BSPs

Timing and Timers

Interrupt and Exception Handling in BSPs

BSP Deployment Issues and Practices

Embedded Linux SDK Basics

The 3 Pieces of an SDK

Embedded Linux Distributions and the GNU Compiler

Collection (GCC)

Other Embedded Linux Development Tools

Library Support, Glibc and Alternatives

SDK Deployment and Support

Debugging

GDB, GDB Server and the GDB Server Debugger

Other Debug and Test Tools

An Eclipse Remote Debug Example

Advanced Debug with printk and syslogd

System-Level Debug

System-Level Debug Tools

The /proc and sys Filesystems

Advanced Logging Methods

KGDB and KDB

Crash Dumps

Debugging Embedded Linux Systems

Configuring Embedded Linux

Config Methods

Config Syntax

Adding Code to the Linux Kernel

Booting Embedded Linux

Processor Startup

Initial Functions The initcalls

Using init Functions

NFS Booting

Root File Systems

RAMdisk Booting with initrd

RAMdisk Booting with initramfs

initrd vs initramfs

Root File System Development

Busybox Development

Building a RAMdisk for an initrd

Building a RAMdisk for an initramfs

Flash File System Development

Testing and Debug of Embedded Linux BSPs

Kernel Debug and Kernel Probes

Kexec and Kdump

The Linux Test Project (LTP)

Performance Tuning Embedded Linux BSPs

Virtualization

Measuring Embedded Linux BSP Performance

Common Considerations

Uncommon Considerations

BootLoader Optimizations

Boot Time Measurements

Effective Memory and Flash Usage

Filesystem Performance Measurement

Some Ideas on Performance Measurement

The Original UNIX Device Driver Model

The fops and file structs

The inode and dentry structs

Major and Minor Numbers

Embedding Channel Information

Deferring Work

The /proc Filesystem

Configuring the Device Driver

A Simulated Device Driver

Modularization Revisited

The Evolution of a New Driver Model

The Initial Object-Oriented Approach

Platform Devices and Drivers

A Generic Subsystem Model

The Generic Subsystem Model in Detail

Subsystem Registration

The Probe and Init Functions

The Show and Store Functions

User Access via the /sys Filesystem

Configuring the New Device Driver

The udev Linux Application

Comparing the Two Driver Models

The Flattened Device Tree (FDT)

openBoot and its Effect on Embedded Linux

The Device Tree Script (dts) File

The Device Tree Compiler (dtc)

The Device Tree Blob (dtb) File

Building a dtb File

Hybrid Device Drivers

Other fops Functions

The Need for loctl

Linux Device Driver Subsystems

Direct Connect Device Drivers

Serial/Console Drivers, I2C & SPI

Real-Time Clocks and Watchdogs

GPIO and the Pinmux

Flash MTDs and Direct Memory Access

USB, Power and CPU Management

Video and Audio

PCI and VME

Block Devices

RAMdisk and Flash Filesystems

MMCs and SD Cards

Network Device Drivers

MAC and PHY Device Drivers

net device and net device stats

Network Device Initialization

Device Discovery and Dynamic Initialization

Network Interface Registration

Network Interface Service Functions

Receiving and Transmitting Packets

Notifier Chains and Device Status Notification

Unwired Device Drivers

Wireless Device Drivers (WiFi, WLAN)

Bluetooth and BlueZ Infrared and IrDA

Cellular from 2G to 5G

Drivers in User Space

Accessing I/O and Memory Regions

User Mode SCSI, USB and I2C

UIO

High-Speed Interconnects

PCle

iSCSI

Infiniband

FibreChannel

Debugging Device Drivers

kdb, kgdb and JTAG

Kernel Probes

Kexec and Kdump

Kernel Profiling

User Mode Linux

Performance Tuning Device Drivers

Some Final Recommendations

http://ieeeboston.org/embedded-linux-bsps-device-drivers-line-course/

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Embedded Linux Optimization - Tools and Techniques (Online Edition)



Students have access to this self-paced course for 90 days!!

Registration fee: \$250

Summary - This video course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand debugging, profiling and testing high performance Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.

 To give students the confidence to apply these concepts to their next Embedded Linux project.

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

Getting Started with Embedded Linux
Embedded Linux Training Overview
Terminology
Linux Versioning
The GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs
Linux References (Books and Online)
A Development Cycle Focused on Performance
A Basic Optimization Process

Basic Debugging Review
Embedded Applications Debug
GDB, GDB Server and the GDB Server Debugger
Other Debuggers
An Eclipse Remote Debug Example
Debugging with printk, syslog, syslogd and LTTng
System-Level Debug

System-Level Debug Tools
The /proc and /sys Filesystems

Basic Logging	New Tracing Methods
KDB and KGDB	SystemTap
Crash Dumps and Post-Mortem Debugging	Ftrace, Tracepoints and Event Tracing
Debugging Embedded Linux Systems	Tracehooks and utrace
Backend Debuggers	Profiling
In-Circuit Emulators	Basic Profiling
Hardware Simulators	gprof and Oprofile
Analyzers	Performance Counters
Requirements Development	LTTng
Performance Requirements	Another DDD Example
Derived Requirements	Manual Profiling
Testability and Traceability	Instrumenting Code
Reviewing Requirements	Output Profiling
Designing for Performance	Timestamping
Design for Test (DFT)	Addressing Performance Problems
Agile Software Design	Types of Performance Problems
Software and Linux Decomposition	Using Performance Tools to Find Areas for
Memory Management	Improvement
CPU and OS Partitioning	Application and System Optimization
Design Reviews	CPU Usage Optimization
Coding for Performance	Memory Usage Optimization
Coding Standards and Consistency	Disk I/O and Filesystem Usage Optimization
Languages, Libraries and Open Source Compo-	Measuring Embedded Linux Performance
nents	Some Ideas on Performance Measurement
Learning Magic Numbers	Common Considerations
Letting Compilers Work For You	Uncommon Considerations
Global, Static and Local Variables	Using JTAG Methods
Code Reviews	BootLoader Measurements
	Boot Time Measurements
Software Testing	The Perf Tool
Unit-Level Testing	Origins of Perf
System-Level Testing	The Perf Framework
Code Coverage Tools	Perf Commands and Using Perf
gcov	Listing Events
Automated Testing	Counting Events
Some Embedded Linux Test Recommendations	Profiling with Perf
DebugFS	Static Tracing with Perf
Configuring DebugFS	Dynamic Tracing with Perf
DebugFS Capabilities	Perf Reporting
Advanced Logging	Performance Tool Assistance
LogFS	Recording Commands and Performance
Using Logwatch and Swatch	System Error Messages and Event Logging
Using syslogd and syslog-ng	Dynamic Probes
Tracing	Jprobes and Return Probes
ptrace and strace	Kernel Probes

Kexec and Kdump

Improving Boot Performance

Boot Time Optimization

The Linux Fastboot Capability

Building a Smaller Linux

Building a Smaller Application

Filesystem Tips and Tricks

Some Notes on Library Usage

Improving Kernel Performance

Kernel Hacking

CONFIG EMBEDDED

Configuring printk

Test Code

Configuring Kernel and IO Scheduling

Improving CPU Performance

Run Queue Statistics

Context Switches and Interrupts

CPU Utilization

Linux Performance Tools for CPU

Process-Specific CPU Performance Tools

Stupid Cache Tricks

Improving System Memory Performance

Memory Performance Statistics

Linux Performance Tools for Memory

Process-Specific Memory Performance Tools

More Stupid Cache Tricks

Improving I/O and Device Driver Perfor-

mance

Disk. Flash and General File I/O

Improving Overall Performance Using the

Compiler

Basic Compiler Optimizations

Architecture-Dependent and Independent

Optimization

Code Modification Optimizations

Feedback Based Optimization

Application Resource Optimization

The Hazard of Trust

An Iterative Process for Optimization

Improving Development Efficiency

The Future of Linux Performance Tools

Some Final Recommendations

http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/

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Software Development for Medical Device Manufacturers (Online Edition)

Students have access to this self-paced course for 90 days!! Registration Fee: \$125

Course Description This course provides an introduction to the development of medical device software. The course is comprised of 4 modules that range from 30-45 minutes in duration. The focus is on complying with FDA Design Controls and IEC 62304 requirements.

This course is intended for software developers who are actively involved in developing medical device software.

Module 1

- Medical Device Definitions: FDA and European Union (EU)
- Regulatory Roadmap
- FDA/EU Device Classifications
- FDA QSR Regulation
- FDA Guidance Documents that pertain to medical device software

Module 2

- International Standards that pertain to medical device software
- Types of Software Regulated by FDA
- Quality System basics: Procedures, Work Instructions and Records
- ALL Software is Defective...

Module 3:

- Design Control Overview
- General Requirements
- Design and Development Planning
- Software Development Models
- Design Input
- About Requirements...
- Design Output

Design Reviews

Module 4:

- Design Control (continued)
- Design Verification
- Software Verification Process
- Testing Overview
- Design Validation
- Software Validation Process
- Design Changes
- Design Transfer
- Design History File
- Course Summary

Speaker Bio:

Steven R. Rakitin has over 40 years experience as a software engineer including 25 years of experience in the medical device industry. He has worked with over 85 medical device manufacturers worldwide, from startups to Fortune 100 corporations. He has written several papers on medical device software risk management as well as a book titled: Software Verification & Validation for Practitioners and Managers.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE and a member of MassMEDIC. He is on the Editorial Review Board for the ASQ Journal Software Quality Professional.

As President of Software Quality Consulting Inc., he helps medical device companies comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

Fundamental Mathematics Concepts Relating to Electromagnetics (Online Edition)

Students have access to this self-paced course for 90 days!!

Registration Fee: 150

Course Summary This course is designed for people wishing to refresh or to learn the fundamental mathematical concepts that are used to describe electromagnetic wave behavior. The modules address all of the basic math concepts covered in a traditional undergraduate electromagnetics course in an ECE curriculum. These concepts include Vector Basics, Integral Vector Calculus, Differential Vector Calculus, Fundamental Coordinate Systems and Complex Numbers. After completing these modules, a person should have sufficient math skills to pursue graduate studies in electromagnetics and/or be able to decipher the math presented in an upper-level text on the subject.

Target audience: This course is designed for people wishing to refresh or to learn the fundamental mathematical concepts that are used to describe electromagnetic wave behavior.

Course chapters

- 1. Vector Basics
- 2. Dot Product

- 3. Cross Product
- 4. Contour Integration
- 5. Vector Algebra
- 6. Surface Integration
- 7. Metric Coefficients
- 8. Coordinate Systems
- 9. Vector Coordinate Conversion
- 10. Del Operator and the Gradient
- 11. The Curl
- 12. Divergence
- 13. Stokes Theorem
- 14. Divergence Theorem
- 15. Laplacian
- 16. Complex Numbers

Instructor's Bio:

Dr. Kent Chamberlin is the Chair and a Professor in the Department of Electrical and Computer Engineering. In his more than thirty-five years in academia, he has performed research for more than twenty sponsors, including the National Science Foundation. He has received two Fulbright awards, including the prestigious Fulbright Distinguished Chair, which he served in Aveiro, Portugal. He has also served as an Associate Editor for the Institute for Electrical and Electronics Engineers, and he continues to be active in performing and publishing in a range of research areas.

http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/

Reliability Engineering for the Business World (Online Edition)

Students have access to this self-paced course for 90 days!!

Registration Fee: 320

Course Description

This course is about becoming a leader in reliability engineering. While statistics are the tools of reliability engineering, it takes knowledge not only of these tools but also of the business. Developing knowledge of the business, from sales, engineering, customer service, to supply chain management can determine how effective you can be in improving reliability.

Never take anything for granted, even some rules of thumb in reliability can be misleading, this course will show you how to prove what truly happens in the real world and how to effect change in any part of the business where it is needed. We will explore the balance sheet, organizational structure, customers, service, and high volume manufacturing. It's not just about how often things fail, it is also about where the defect came from, what is the financial effect, the recovery, when should a business take field action, effect of human error, failure analysis/material science, reliability testing, and much more. I will also discuss how you develop executive buy in for change. The course assumes a basic knowledge in reliability statistics. There are 12 sessions that cover the following topics.

Course Outline

Basics – Measurements Business Model Design Model (HW and SW) HALT/RDT/Predictions
Manufacturing Model
Early Life Failures
Wear Out and Mid Life Crisis
Advanced Reliability

Course Objective

To teach you how to become the go to person in your business for objective business sensed reliability answers and requirements.

Instructor's Bio

Kevin is an innovative leader in reliability methodologies with more than 30 years experience in the storage industry. In his latest role as Director of Engineering, he developed a top down reliability/ availability management process for design organizations developing mission-critical storage systems. Kevin previously directed the most extensive HALT/HASS operation in the industry, with over 300 chambers worldwide. He has written several papers, consulted with many companies, 3 patents awarded and 2 pending related to systems reliability and test.

His most recent work has been performing system architectural analysis to optimize system availability, serviceability and costs. Providing guidance to development to maximize system reliability and reduce service costs. He has provided consultation to many large companies such as EMC, CISCO, AT+T, HP, Seagate and many others. His position and experience has enabled him to perform extensive field studies and design of experiments. Kevin has developed many

Introduction to Embedded Linux (Online Edition)

Students have access to this self-paced course for 90 days!! Registration Fee: 350

Course Summary:

This first of a 2-part series introduces the Linux Operating System and the use of Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part covers the methods for booting Embedded Linux distributions including embedded cross-development and target board considerations.

Who Should Attend:

The course is designed for real-time engineers who are building Embedded Linux solutions. It is also targeted at experienced developers requiring a refresher course on Embedded Linux. This course will clearly demonstrate both the strengths and weaknesses of the Linux Operating System in Embedded Systems.

Course Objectives:

To provide a basic understanding of the Linux OS and the Eclipse IDE framework.

To gain an understanding of the complexities of Embedded Linux Distributions and their use in embedded systems.

To give students confidence to apply these concepts to their next Embedded Linux project Hardware and Software Requirements

The student should have a working Linux desktop environment either directly installed or in a virtualization environment. The desktop Linux should have the GNU compiler and binary utilities (binutils) already installed. A working Eclipse C/C++ instal-

lation or prior knowledge of C-based Makefiles is useful for completion of lab exercises. Lab solutions are also provided with the course. An Embedded Linux target hardware platform is useful but not absolutely required for this course.

Additional Reference Materials

Linux Kernel Development by Robert Love Linux System Programming by Robert Love Linux Debugging and Performance Tuning by Steve Best

Optimizing Linux Performance by Phillip G. Ezolt Embedded Linux Primer by Christopher Hallinan Pro Linux Embedded Systems by Gene Sally Embedded Linux Development Using Eclipse by Doug Abbott

Linux Device Drivers by Jonathan Corbet et al Essential Linux Device Drivers by Sreekrishnan Venkateswaran

Course Downloadable Content:

Video Lecture
Hands-On Lab Instructions
Hands-On Lab Solutions
Additional Related Materials

The Basics

Linux Terminology, History and Versioning The Linux Community: Desktop & Embedded The GPL

Linux References (Books and Online)

Getting Started

Kernel Source Code Building the Kernel Embedded Linux Kernels Linux 2.6

Basic Kernel Capabilities

Process and Threads Management Signals and System Calls

Synchronization, IPC and Error Handling Timing and Timers Memory Management and Paging The I/O Subsystem: A Tale of Two Models Modularization

Debugging

Process-Level and System-Level Debug GDB and KGDB GDB Server and Remote Debugging

An Eclipse Debug Example

Other Debug and Test Tools
Other System-Level Debug Approaches
Process & Threads Management
What are Processes and Threads?
Virtual Memory Mapping
Creating and Managing Processes and Threads
Thread-Specific Data (TSD) POSIX
The Native POSIX Threading Library (NPTL)
Kernel Threads

Signals System Calls Scheduling

Linux 2.4 and 2.6 Scheduling Models The O(1) Scheduler The Completely Fair Scheduler (CFS)

Synchronization

Via Global Data Via Semaphores, Files and Signals

Inter-Process Communications (IPC)

Message Queues Semaphores Revisited Shared Memory Pipes, FIFOs and Futexes Remote Procedure Calls Networking

Error Handling

errno and perror strerror and strerror_r oops, panics and Segmentation Faults **Timing** How Linux Tells Time Kernel, POSIX and Interval Timers High-Resolution Timers (HRTs)

Memory Management and Paging

Demand Paging and Virtual Memory Allocating User and Kernel Memory Mapping Device Memory The Slab Allocator The OOM Killer Memory in Embedded Systems

Modularization

Creating a Module and Module Loading Dependency Issues In Embedded Systems

Shared Libraries

A Shared Library Example Static and Dynamic Libraries

The I/O Subsystem: A Tale of Two Models

The Original Device Driver Model
The Standard I/O Interface
The New Device Driver Model and Kernel Object
Classes
Initialization

Platform Devices, Busses, Adapters and Drivers Comparing the Two Models

Embedded Linux Trends

Development, Monitoring and Testing

Some Final Recommendations

Lecturer:

Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. A 20-year electronics veteran, he has held various positions at Tilera, Embedded Planet, Wind River Systems, Lockheed Sanders, Stratus Computer and Apollo Computer. RTETC, LLC is a provider of Eclipse-based development tools, training and consulting for the embedded systems market.

Last Notice Before Course Begins, Please Register Now!!!)

Practical RF PCB Design: Wireless Networks, Products and Telecommunications

Date & Time: Thursday & Friday, December 14 & 15; 9AM - 4:30PM

(13 hours of instruction!)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Henry Lau, Lexiwave Technology

Overview: One of the most demanding consumer products in the market is the wireless telecommunication product. A well-designed Radio Frequency Printed Circuit Board (RF PCB) contributes significantly to the success of any wireless product as the layout of the PCB greatly affects the performance, stability and reliability of the product. In today's highly competitive wireless products market with increasingly compressed development time-frame, there is a strong demand for RF professionals who possess the knowledge and experience to design top-performing RF PCBs in less number of iterations. What matters is whether your level of competence is up to the required standard to meet such demand.

Audience: RF Designers, Wireless Product Designers, Field Application Engineers, Design Managers and related professionals.

Benefits: This course aims to provide participants with an insightful training on RF PCB design from a practical, industrial perspective. Participants will be led through a systematic, theoretical presentation with case studies on commercial products in the training. The course will be conducted by an RF expert with rich industrial experience. It is suitable for RF professionals who want to keep up-to-date their skills and knowledge in RF PCB design and stay competitive.

OUTLINE

1. Printed circuit board design for RF circuits

From product design, circuit design to PCB design

Layer stack-up assignment

Grounding methods and techniques

Interconnects and I/O

Bypassing and decoupling

Partitioning methods

2. Printed circuits board design for other circuits

Clock circuits

Base-band circuits

Audio circuits

Power supplies

Impedance-controlled circuits

3. PCB design for EMC/EMI compliance

EMC/EMI compliance

Grounding methods

Decoupling methods

Shielding methods

4. Additional Design Techniques

Production concerns

Systematic product design approach

RF Modules

Evaluation boards

Other RF concerns

Casing design

5. Case studies

Expertise:

Henry Lau received his M.Sc. and MBA degrees from UK and USA respectively. He has more than 25 years of experience in designing RF systems, products and RFICs in both Hong Kong and US. He worked for Motorola and Conexant in US as Principal Engineer on developing RFICs for cellular phone and silicon tuner applications. Mr Lau holds five patents all in RF designs. He is currently running Lexiwave Technology, a fables semiconductor company in Hong Kong and US designing and selling RFICs, RF modules and RF solutions. He has also been teaching numerous RF-related courses internationally.

notes, lunch and coffee breaks included with registration

Decision (Run/Cancel) Date for this Courses is Monday, December 4, 2017

Payment received by November 29

IEEE Members \$405 Non-members \$435

Payment received after November 29

IEEE Members \$435 Non-members \$455

http://ieeeboston.org/practical-rf-pcb-design-wireless-networks-products-telecommunications-fall-2017

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is

http://ieeeboston.org/course-proposals/. Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gamil.com or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

CALL FOR PAPERS



2018 IEEE High Performance Extreme Computing Conference (HPEC '18)

Twenty-second Annual HPEC Conference



25 - 28 September 2018 Westin Hotel, Waltham, MA USA

www.ieee-hpec.org

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Administrative Contacts Mr. Robert Alongi IEEE Boston Section The IEEE High Performance Extreme Computing Conference (HPEC '18) will be held in the Greater Boston Area, Massachusetts, USA on 25 – 28 September 2018. The HPEC charter is to be the premier conference in the world on the confluence of HPC and Embedded Computing.

The technical committee seeks new presentations that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- Machine Learning
- Graph Analytics and Network Science
- Advanced Multicore Software Technologies
- Advanced Processor Architectures
- Automated Design Tools
- Big Data and Distributed Computing
- Big Data Meets Big Compute
- Case Studies and Benchmarking of Applications
- Cloud HPEC
- Computing Technologies for Challenging Form Factors
- ASIC and FPGA Advances

- Data Intensive Computing
- Digital Front Ends
- Fault-Tolerant Computing Embedded Cloud Computing
- General Purpose GPU Computing
- High Performance Data Analysis
- Interactive and Real-Time Supercomputing
- Mapping and Scheduling of Parallel and Real-Time Applications
- New Application Frontiers
- Open System Architectures
- Secure Computing & Anti-Tamper Technologies

HPEC accepts two types of submissions:

- 1. Full papers (up to 6 pages, references not included), and
- 2. Extended abstracts (up to 2 pages, references included).

IMPORTANT DATES:

Submission Deadline: May 18, 2018
Notification of Acceptance: July 1, 2018
Camera Ready Deadline: August 1, 2018

Preference will be given to papers with strong, quantitative results, demonstrating novel approaches or describing high quality prototypes. Authors of full papers can mark their preference for a poster display or an oral presentation. Presenters who wish to have hardware demonstrations are encouraged to mark their preference for a poster display. Accepted extended abstracts will be displayed as posters. All paper and extended abstract submissions need to use the approved IEEE templates. Full paper submissions with the highest peer review ratings will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions and extended abstracts are published on ieee-hpec.org. Vendors are encouraged to sign up for vendor booths. This will allow vendors to present their HPEC technologies in an interactive atmosphere suitable for product demonstration and promotion. Papers can be declared "student paper" if the first author was a student when doing the presented work, and will be eligible for the "IEEE HPEC best student paper award." Papers should not be anonymized. We welcome input (hpec@ieee-hpec.org) on tutorials, invited talks, special sessions, peer reviewed presentations, and vendor demos. Instructions for submitting will be posted on the conference web site shortly. Full paper submissions should use the approved IEEE templates. The highest scoring submissions will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions are published on ieee-hpec.org.

Advanced Embedded Linux Optimization

Time & Date: 6 - 9PM, Mondays, Jan. 8, 15, 22 & 29, 2018 (12 hours of instruction!)

Location: Woburn, MA area near to Rt. 95/128

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand debugging, profiling and testing high performance Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.
- To give students the confidence to apply these concepts to their next Embedded Linux project.

Course Schedule Day 1

Getting Started with Embedded Linux

Embedded Linux Training Overview

Terminology

Linux Versioning

The GPL

Building the Kernel Source Code

Embedded Linux Kernels

BSPs and SDKs

Linux References (Books and Online)

A Development Cycle Focused on Performance

A Basic Optimization Process

Basic Debugging Review

Embedded Applications Debug

GDB, GDB Server and the GDB Server Debugger

Other Debuggers

An Eclipse Remote Debug Example

Debugging with printk, syslog, syslogd and LTTng

System-Level Debug

System-Level Debug Tools

The /proc and /sys Filesystems

Basic Logging

KDB and KGDB

Crash Dumps and Post-Mortem Debugging

Debugging Embedded Linux Systems

Backend Debuggers

In-Circuit Emulators

Hardware Simulators

Analyzers

Course Schedule Day 2

Requirements Development

Performance Requirements **Derived Requirements** Testability and Traceability Reviewing Requirements Designing for Performance Design for Test (DFT) Agile Software Design Software and Linux Decomposition **Memory Management** CPU and OS Partitioning **Design Reviews** Coding for Performance Coding Standards and Consistency Languages, Libraries and Open Source Components Learning Magic Numbers Letting Compilers Work For You Global, Static and Local Variables Code Reviews Software Testing **Unit-Level Testing** System-Level Testing **Code Coverage Tools** gcov **Automated Testing** Some Embedded Linux Test Recommendations DebugFS Configuring DebugFS **DebugFS Capabilities** Advanced Logging LogFS Using Logwatch and Swatch Using syslogd and syslog-ng **Tracing** ptrace and strace **New Tracing Methods** SystemTap Ftrace, Tracepoints and Event Tracing Tracehooks and utrace **Profiling Basic Profiling** gprof and Oprofile

Performance Counters

LTTng

Another DDD Example

Manual Profiling
Instrumenting Code
Output Profiling
Timestamping

Output Profiling Timestamping Course Schedule Day 3 Addressing Performance Problems Types of Performance Problems Using Performance Tools to Find Areas for Improvement Application and System Optimization **CPU Usage Optimization** Memory Usage Optimization Disk I/O and Filesystem Usage Optimization Measuring Embedded Linux Performance Some Ideas on Performance Measurement **Common Considerations Uncommon Considerations** Using JTAG Methods **BootLoader Measurements Boot Time Measurements** The Perf Tool Origins of Perf The Perf Framework Perf Commands and Using Perf Listing Events **Counting Events** Profiling with Perf Static Tracing with Perf Dynamic Tracing with Perf Perf Reporting Performance Tool Assistance

Recording Commands and Performance System Error Messages and Event Logging Dynamic Probes Jprobes and Return Probes

Jprobes and Return Probes

Kernel Probes
Kexec and Kdump

Improving Boot Performance

Boot Time Optimization
The Linux Fastboot Capability
Building a Smaller Linux
Building a Smaller Application
Filesystem Tips and Tricks

Some Notes on Library Usage

Course Schedule Day 4

Improving Kernel Performance

Kernel Hacking

CONFIG_EMBEDDED

Configuring printk

Test Code

Configuring Kernel and IO Scheduling

Improving CPU Performance

Run Queue Statistics

Context Switches and Interrupts

CPU Utilization

Linux Performance Tools for CPU

Process-Specific CPU Performance Tools

Stupid Cache Tricks

<u>Improving System Memory Performance</u>

Memory Performance Statistics

Linux Performance Tools for Memory

Process-Specific Memory Performance Tools

More Stupid Cache Tricks

Improving I/O and Device Driver

Performance

Disk, Flash and General File I/O

Improving Overall Performance Using the

Compiler

Basic Compiler Optimizations

Architecture-Dependent and Independent Opti-

mization

Code Modification Optimizations

Feedback Based Optimization
Application Resource Optimization
The Hazard of Trust
An Iterative Process for Optimization
Improving Development Efficiency
The Future of Linux Performance Tools
Some Final Recommendations

Lecturer – Mike McCullough is President and CEO of RTETC, LLC. Mike has a BS in Computer Engineering and an MS in Systems Engineering from Boston University. He has held a variety of software engineering positions at LynuxWorks, Embedded Planet, Wind River Systems and Lockheed Sanders. RTETC, LLC provides real-time embedded training and consulting to many embedded systems companies. RTETC focuses on real-time operating systems (RTOS), Linux and Android solutions for the embedded systems market.

Decision (Run/Cancel) Date for this Course is Thursday, December 28, 2017

Payment received by December 26

IEEE Members \$395 Non-members \$415

Payment received after December 26

IEEE Members \$415 Non-members \$435

http://ieeeboston.org/advanced-embedded-linux-optimization-2

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Facebook: https://www.facebook.com/IEEEBoston

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Google+: https://plus.google.com/107894868975229024384/

LinkedIn: https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about

Last Notice Before Course Begins, Please Register Now!!!)

Writing Agile User Story and Acceptance Test Requirements -

Cut Creep Overruns, Disappointment, and Embarrassment

Date & Time: Tuesday, December 12; 8:30AM - 5:00PM (7.5 hours of instruction!)

Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA Location:

Speaker: Robin Goldsmith, President, GoPro Management

Everyone complains that poor requirements are the major cause of project problems. Yet, like the weather, nobody does much about it, at least not effectively. Traditional approaches advocate writing voluminous requirements documents that too often don't seem to help much and may even contribute to difficulties. Agile goes to the opposite extreme, relying on brief requirements in the form of threeline user stories that fit on the front an index card and a few user story acceptance criteria that fit on the card's back. Surprise, as Mark Twain noted, in some ways it's even harder to write Agile's brief requirements effectively. This interactive workshop reveals reasons user stories and their acceptance tests can fall short of their hype, explains critical concepts needed for effectiveness, and uses a real case to provide participants guided practice writing and evaluating user stories and their acceptance criteria/tests.

PARTICIPANTS WILL LEARN:

- Major sources of poor requirements that cause defects, rework, and cost/time overruns.
- How Agile user stories and their acceptance criteria/tests address these issues.

- Difficulties that still afflict requirements in Agile projects and why they persist.
- Writing more effective user stories and acceptance criteria/tests.
- What else is necessary to produce working software that provides real value.

WHO SHOULD ATTEND:

This course has been designed for product owners, analysts, developers, and other Agile (and other) project team members who are or should be involved in defining requirements.

AGILE, USER STORY FUNDAMENTALS

Agile Manifesto's relevant points Characterization of traditional approaches Waterfall and big up-front requirements Agile's sprints and backlogs alternative Agile project team roles User story "As a <role>..." (Card) User story acceptance criteria (Confirmation) Estimating user story size Splitting and refining Prioritizing and allocating to backlogs/sprint

Constructing/implementing (Conversations)

Reviewing, retrospectives

Grooming backlog and reprioritizing

REQUIREMENTS ARE REQUIREMENTS— OR MAYBE NOT

User stories are backlog items, features
Chicken and egg relation to use cases
Issues and inconsistencies
Business vs. product/system requirements
"Levels Model" of requirements
Other mistaken presumptions
Requirements overview
Where user stories should fit, do fit instead
Conversation conundrum

WRITING MORE SUITABLE USER STORIES

Problem Pyramid™ tool to get on track Exercise: Using the Problem Pyramid™

Exercise: Business Requirement

User Stories

Issues identifying requirements
Product owner and business analyst roles
Project team participation
Dictating vs. discovering
Data gathering and analysis
Planning an effective interview
Controlling with suitable questions
Then a miracle occurs...

Defects and new user stories Testing that user story focus misses Reactive vs. proactive risk analysis Given, when, then format

Exercise: Write User Story Acceptance Criteria

Exercise: Design their Tests

Exercise: Review Your User Stories/Tests

Speaker's Bio: Robin F. Goldsmith, JD is an internationally recognized authority on software development and acquisition methodology and management. He has more than 30 years of experience in requirements definition, quality and testing, development, project management, and process improvement. A frequent featured speaker at leading professional conferences and author of the recent Artech House book, Discovering REAL Business Requirements for Software Project Success, he regularly works with and trains business and systems professionals.

AND USER STORY ACCEPTANCE TESTS

Missed and unclear criteria
Turning criteria into tests, issues
How many tests are really needed
Test design techniques
Checklists and guidelines
Decision trees, decision tables
Boundary testing
Testing is main means to control risk

Decision (Run/Cancel) Date for this Courses is Tuesday, December 5, 2017

Payment received by Nov. 28

IEEE Members \$220 Non-members \$245

Payment received after Nov. 28

IEEE Members \$245 Non-members \$265

http://ieeeboston.org/writing-agile-user-story-acceptance-test-requirements-2



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Join/Renew



Last Notice Before Course Begins, Please Register Now!!!)

Risk Management Methods for Test Projects

Make Sure the Most Important Testing Is Done in Limited Available Time

Date & Time: Thursday, December 14; 8:30AM - 5:00PM (7.5 hours of instruction!)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Robin Goldsmith, President, GoPro Management

Testing is our primary means of reducing risks related to systems and software. All testing is risk-based in that there are more potential tests than we have time and resources to run, so we choose those that address higher risks. The difficulty is adequately identifying the potential risks, for which a number of structured techniques are described. Risk management involves obtaining, directing, and controlling resources for continuously planning, strategizing, identifying, analyzing, prioritizing, preventing, responding to, mitigating, monitoring, controlling, and reporting risk. Key types of risks and identification approaches are distinguished. Powerful Proactive Testing™ techniques are demonstrated that enhance conventional reactive testing risk analysis to enable testing higher risks not only more but earlier. Exercises aid learning by allowing participants to practice applying practical methods to realistic examples.

Participants will learn:

- The elements of risk and risk response, and their relation to software development and testing.
- Importance of distinguishing business, management, functional, and technical risk causes and effects.
- Alternative methods for identifying, analyzing, classifying, and prioritizing the several types of risks.
- Proactive Testing[™] methods that enhance conventional reactive testing risk identification, response.
- Monitoring, evaluating, adjusting, and reporting on risk activities, findings, and results.

WHO SHOULD ATTEND: This course has been designed for analysts, designers, programmers, testers, auditors, users, and managers who rely on, plan, oversee, and/or carry out testing of software products.

1 NATURE AND IMPORTANCE OF RISK

Murphy's Law; O'Brien's Law
Relation of risk to software and testing
Classical risk management
Impact and probability risk elements
Classical risk mitigation, contingency plans
Costs, ease of detecting, controlling vs. harm
Quantifying qualitative risk, tricks and traps
Types, classifications of risks
Threats, vulnerabilities, triggers
Risk identification analysis methods
Business, functional, and operational risks
Direct and indirect forms of injury
Management and technical risks
Effects vs. causes risk identification
Monitoring, controlling, reporting risks

2 PROJECT MANAGEMENT RISKS

Most frequently encountered risks
Changing requirements and scope creep
Lack of management support, priorities
Typically unrecognized interrelationships
Features/quality, resources, schedule risks
Software risks--or just poor management
Sizing implications for software QA/testing
Traditional checklists for project managers
Evaluating risk factor checklists usefulness
Software risk taxonomy
Monitoring and managing risk as a project

3 CONVENTIONAL RISK ANALYSIS

Testing riskier features, components more Costs, additional testing resources vs. fixed System, development practices checklists Design analysis vs. prioritizing test cases Common subjective risk judgment methods Rating vs. ranking, setting objective criteria Reporting, gaining agreement on risks

4 PROACTIVE RISK-BASED TESTING

Why typical risk-based testing is reactive
Proactive Testing™ Life Cycle
Structured model of test planning
Multiple levels, points of risk analysis
Prioritization demands knowing the choices
Project-level proactive risk analysis
Identifying overlooked project-specific risks
Refocusing on tests that reduce the key risks
Letting testing drive development
Gaining user, manager, developer support
Identifying and analyzing lower-level risks

Differentiating user and technical views
Risk analysis in test designs and test cases
Risks of not testing some things
Metrics to monitor effectiveness, efficiency
Anticipating and measuring operational risks
Risk management roles and responsibilities
Reporting risk status, expected and actual
Categorizing actuals, improving over time

Decision (Run/Cancel) Date for this Courses is Thursday, December 7, 2017

Payment received by Nov. 30

IEEE Members \$220 Non-members \$245

Payment received after Nov. 30

IEEE Members \$245 Non-members \$265

http://ieeeboston.org/risk-management-methods-test-projects/

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Facebook: https://www.facebook.com/IEEEBoston

YouTube: https://www.youtube.com/user/IEEEBostonSection

Google+: https://plus.google.com/107894868975229024384/

LinkedIn: https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about

Last Notice Before Course Begins, Please Register Now!!!)

Developing Reusable Test Designs

Be an Instant Expert--Run More, and More Thorough, Tests in Less Time

Date & Time: Friday, December 15; 8:30AM - 5:00PM (7.5 hours of instruction!)

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Would you like to be an instant testing expert, able to start testing effectively in new situations without delay? And would you like to spend more of your time running tests and less of your time creating the tests? Reusable test designs are a little-known but powerful test planning/design tool that make it possible for you to run more effective test cases in less time. This interactive seminar workshop shows you how to apply a systematic structured Proactive Testing™ approach that first enables you to design much more thorough tests than traditional methods. Then, you'll discover how to convert your test designs into reusable test designs that you can apply instantly in new situations. You'll develop several reusable test designs in class and be ready to add more to your toolkit back on the job. Exercises enhance learning by allowing participants to practice applying practical techniques to an actual case.

Participants will learn:

- How test designs fit into the overall test planning structure and provide special advantages
- Systematic reliably repeatable methods for identifying test designs to test a given system.
- Checklists and guidelines that enable you to spot the conditions traditional methods overlook.
- Converting your project-specific test designs into reusable test designs you can use for other systems.
- Applying reusable test designs to jumpstart your testing with instant expertise and effectiveness.
- Quickly and reliably selecting the subset of test cases suitable for scale and risk.

WHO SHOULD ATTEND: This course has been designed for testers, managers, analysts, designers, programmers, auditors, and users who plan, oversee, and/or carry out testing of software products.

PROACTIVE TEST DESIGN BENEFITS

Proactive vs traditional reactive testing
Proactive Testing™ Life Cycle advantages
IEEE Standard for Test Documentation
Often-overlooked key to proper prioritizing
Systematic drill-down strategy
Master and detailed test plans
Test design specifications
Test case specifications
How taking time to structure saves time
Structuring to make test sets manageable
Facilitating reconstruction of test data
Taking off the blinders to allow selectivity
Re-using instead of rebuilding test designs
Instant expertise for testing new situations

IDENTIFYING NEEDED TEST DESIGNS

Functional (black box) testing
Three-level approach to functional testing
Keys for thoroughness
Breaking down to manageable pieces
Functionality Matrix technique
Use case perspective
Technical software actions
Test design specifications that are needed

DESIGNING TESTS MORE THOROUGHLY

How designing adds thoroughness Traditional test design still misses a lot Focused brainstorming for a better start Checklists and guidelines to fill the gaps Tests based on data formats
Coverage of data and process models
Decision trees and tables
Concerns common to all types of testing
Equivalence classes and partitioning
Ranges and boundary testing
GUI and navigation issues
Often-overlooked other dimensions to test
Formal/informal test design specifications
Extracting the reusable elements
Enhancing with system-specific tests
Link to driving effective automated tests

SPECIFYING (REUSABLE) TEST CASES

Translating test designs into test cases Selecting scaled subset based on risk Reusable test case specifications Other essential test case component Finding and creating test data Test script and matrix formats Simple and sophisticated automation

Decision (Run/Cancel) Date for this Courses is Friday, December 8, 2017

Payment received by Dec. 1 IEEE Members \$220 Non-members \$245

Payment received after Dec. 1

IEEE Members \$245 Non-members \$265

http://ieeeboston.org/developing-reusable-test-designs/

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