BOSTON

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TABLE OF CONTENTS

IEEE Boston Section Online Courses:

Verilog101:Verilog Foundations CLASS DESCRIPTION: Verilog is IEEE standard 1364. It is a Hardware Description Language that is the corner stone of much of the simulation world. Verilog Foundations is a comprehensive introduction to the IEEE 1364 (Verilog). The Verilog Foundations class has a slightly different approach to learning Verilog than other methods. There is a lecture section for each main topic. This presents a basic foundation for the language. What makes Verilog Foundations exciting is the emphasis on labs/examples. There are nearly 100 labs/examples giving comprehensive "how to" examples of most Verilog language constructs. There are working solutions for each lab and the students can use the lab database for developing their own models later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace.
(Register at http://www.ieeeboston.org) and click on course title

System Verilog 101: Design Constructs CLASS DESCRIPTION: SytemVerilog is an extensive set of language constructs to the IEEE 1364-2001 standard. It's meant to aid in the creation and verification of models. There are two parts to the language extension. The first part covered by this class, is new design constructs. The second part of SystemVerilog is verification constructs, covered by SystemVerilog102. There are over 100 labs/examples giving comprehensive "how to" examples of most SystemVerilog language constructs. There are working solutions for each lab and the students can use the lab database for developing their own models later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace. There are self-grading quizzes for each chapter that allow the student to see if he/she is learning the material. The goals of this course are to make you familiar with the new part of the language. Students taking SystremVerilog101 will have a 90-day access to it. The lab database you will be able to download and is yours to keep. **(Register at http://www.ieeeboston.org) and click on course title**

System Verilog 102: Verification Constructs CLASS DESCRIPTION:SytemVerilog is an extensive set of language constructs to the IEEE 1364-2001 standard. It's meant to aid in the creation and verification of models. There are two parts to the language extension. The first part covered by SV101, is new design constructs. SV102, this class, covers verification constructs. SystemVerilog102, like all CBE classes, is lab based. There are over 30 verification labs/examples giving comprehensive "how to" examples of most SystemVerilog verification language constructs. There are working solutions for each lab and the students can use the lab database for developing their own assertions later. The class is also self paced. All the work can be done independently by the engineers, at their own computer, and at their own pace. **(Register at http://www.ieeeboston.org) and click on course title**

Introduction to Embedded Linux Part I CLASS DESCRIPTION: This first of a 2-part series introduces the Linux Operating System and the use of Embedded Linux Distributions. The course focuses on the development and creation of applications in an Embedded Linux context using the Eclipse IDE. The first part of the course focuses on acquiring an understanding of the basic Linux Operating System, highlighting areas of concern for Embedded Linux applications development using Eclipse. The latter part covers the methods for booting Embedded Linux distributions including embedded cross-development and target board considerations.

High Performance Project Managment CLASS DESCRIPTION: This12 hour course(broken into short 10 to 20 minute independent modules) provides the project methodology, concepts, and techniques that ensure successful completion (on time, on budget, with the quality required) of projects, large and small. Participants learn the steps to take before, during, and at the end of a project to hone planning and execution to a strategically built process that delivers project success when used. Additionally, the course provides the interpersonal and leadership techniques to ensure everyone involved with the project whether a team member, organization member, or outside of the organization commits to the success of the project—voluntarily—and provides the support and assistance to ensure its success. In addition to learning how to master the technical skills that have evolved over thousands of years of project implementation and practice, the course provides the advanced team building, leadership, and interpersonal skills that ensure the technical skills can be used, they way they are designed to be used, resulting in a process that delivers the on time, on or under budget, with the quality required completed project consistently.

Whew! What a Year!

Kevin Flavin, Chair, IEEE Boston Section

We made it! It's December! It has been one doozy of a year! I don't even remember what this past spring was like, I can barely remember this summer - did I go to the beach or was that last year? With holidays right around the corner, it feel like there isn't a moment to take a breath. We now have 'Black Friday' sales starting a week early, how is that supposed work?

For me, my work is ending as Chair of the Boston Section. To be honest, I am satisfied with the progress we made as a section.

We added new chapters. Most actively, the new Technology and Engineering Management chapter. They've been aggressively reaching out and Karthik Geneson keeps the Excom updated with their activities.

We've had a 'couple a three' very successful conferences, with challenges to overcome for next year, as always. Phased Array had excellent attendance and support, and the nascent Student Conference held at MIT this fall was an overwhelming success. As you read this, the Women in Engineering Conference, held here in Boston this year is either running or just finished - with experts from around the country flying in to speak for us.

We're moving to more online courses - it is the way of the future and mobile learning. Len Long, the Chair-elect, is leading that charge. Maybe it's because of the 'Internet of Things', but we have seen a sharp uptick in embedded linux topics. We're looking at other topics related to IoT that could be promising.

We, as a team, have learned a lot. We are making some changes to react to the new mobile, digital, and faster pace of our society. Creating electronic communications, like this digital magazine, and creating online courses are a strong step in that direction.

Also, we've taken a step back and thought hard about what we are doing as a section and how we can best serve the members and the non-member technologists. We came up with a strategy that is basically boiled down to three phases of delivering value to the membership

Phase 1: what would our members and stakeholders want to learn about, what do they need to know?

Phase 2: how would they want to consume what we find in Phase 1?

Phase 3: how do we communicate what we made in Phase 2 to them?

Whatever the answers are, they could be different next fall. The answers were different two years ago, even one year ago. This sounds simple, but answering these questions, thoroughly, correctly, and quickly because we need to do this RIGHT NOW, is not simple. But we are working on it. It's going to be a great year ahead, I can feel it.

Women In Engineering – 12:00PM, Sunday, 4 November

Holiday Luncheon

IEEE WIE Boston gathers annually for a casual holiday lunch where you can get to know some of the WIE Boston members in a relaxed atmosphere while enjoying some great food.

If you are not already a WIE member - it's a great time to think about joining, or if you are a member looking to become more active, that's great, too! We would like to meet you.

Meeting Location: Cheesecake Factory, Burlington Mall, 75 Middlesex Turnpike, Burlington, MA

Please register at:
https://events.vtools.ieee.org/m/42113

Entrepreneurs' Network – 6:30PM, Tuesday, 6 December

Critical Legal Issues for Early Stage Companies

Meeting Location – Constant Contact, 3rd Floor Great Room, 1601 Trapelo Road, Waltham, MA . PRE-MEETING DINNER at 5:15 PM (sharp) at Bertucci's, Waltham

Early stage companies have to address numerous legal issues, including, but not limited to: where to incorporate, founders equity and employee stock option plans, employee agreements including confidentiality and assignment of invention agreements, non-compete agreements, documenting innovations and potential inventions, provisional, utility, and design patents, trademarks and copyrights. Our panel of legal experts will address these legal fundamental issues that early stage companies must consider during their earliest days in order to lay a strong foundation for success.

Speaker: Steve Henry, Esq., IP and General Counsel, Ab Initio Software LLC

Steve Henry, an IEEE Life Member and Certified Licensing Professional, is currently IP and General Counsel at Ab Initio Software LLC, after a long career in private practice. He has over 40 year experience, SB and SM degrees in Electrical Engineering and Computer Science from MIT, and a law degree from Georgetown. Steve's private practice career involved the representation of companies of all sizes, universities, individual professionals, investors and other members of the IP community, and covered the full range of IP activities, including portfolio building, licensing and other IP transactions, litigation (as both plaintiff and defendant), providing risk management opinions to companies and investors, as well as IP strategy development and execution. An advocate of small business, Steve counseled numerous startups, several to the point of successful acquisitions. He has extensive experience in a range of technical areas such as semiconductors, communications, imaging, gene sequencing and software, including open source software agreements and management of the use of open source software. Steve's attention is frequently focused on the practical business implications of IP and contractual issues - avoiding risks and creating opportunities.

Speaker: Marc Johannes, Shareholder, Wolf Greenfield & Sachs

Marc Johannes has 15 years of experience in all aspects of patent prosecution and client counseling including patent procurement, patent portfolio strategy and development, patent validity and infringement opinions, due diligence, clearance studies and advising clients in both offensive and defensive utilization of their intellectual property.

Marc's experience spans a variety of technologies such as extensive experience in imaging technologies including x-ray, magnetic resonance imaging (MRI), medical imaging and equipment, computer vision and image processing, pattern recognition, and also includes experience in speech recognition and speech synthesis, electrical and optical devices, semiconductor devices, networking, MEMS devices and all aspects of software.

Prior to joining the firm, Marc served as a software engineer with Scansoft, Inc. where he was responsible for the design and development of an image acquisition, Image Processing, and Optical Character Recognition application programming interface for document analysis and management applications. Marc's graduate research has included projects in

the areas of pattern recognition, computer vision and shape modeling, image understanding, and speech recognition systems.

Speaker: Justin Nesbit, Partner, Gesmer Updegrove

Justin Nesbit loves to help build things (and companies). He represents emerging and established companies with many aspects of their legal affairs. Justin enjoys providing advice on complicated legal and business issues and always strives to be a part of his clients' growth and success.

What has Justin "built" in the past? 1) He has negotiated and formed numerous licensing, consulting, sales, development and distribution contracts, many on behalf of one of the world's preeminent universities. 2) He has helped to "put together" and close mergers, acquisitions and financings, and he enjoys rolling up his sleeves and working on many aspects of each transaction. 3) Clients rely on him for a wide variety of advice on the day-to-day corporate matters that every company must address if they wish to build a world-class enterprise. 4) Nothing makes Justin happier than building strong relationships with his clients, whether that involves discussing the search for the perfect college for a client's child or learning about what pressing issues keep the client up at night.

Moderator: Bob Weber, Managing Director, Patent Kinetics, LLC

Robert Weber is a successful intellectual property professional, inventor, serial entrepreneur, management consultant, and senior executive. Presently, he is Managing Director, Patent Kinetics, LLC, a company that helps entrepreneurs and patent owners build and monetize valuable patent portfolios. Weber is an inventor with 28 issued US patents and a number of foreign counterparts assigned to Intertrust Technologies, where he served as SVP Business and Technology Strategy, 1996-1999. The Intertrust portfolio was characterized in the Wall Street Journal as a once in a generation billion dollar licensing opportunity. (Intertrust is presently a joint venture of Sony and Philips.) Most recently, Patent Kinetics and its legal team successfully resolved a patent and trademark case brought on behalf of the inventor and trademark owner. Previously, in his role of Vice President, Corporate Development and Licensing (part time), for Open Security Solutions, LLC., Weber was instrumental in licensing a patent portfolio relating to information security to a well-known patent licensing and assertion company and in obtaining a resolution of patent litigation that had been pending in the Eastern District of Texas. In 2009, this litigation was resolved in favor of OSS and its partner company. Weber has also been a Principal Consultant at Northeast Consulting Resources, Inc. At NCRI, his consulting practice focused on the intersection of business and technology. Weber divides his time between Boston and Silicon Valley. He is a former Vice Chair, Programs, of the Boston Entrepreneurs Network and is a member of the Licensing Executives Society.

Meeting Location: Constant Contact, Inc., Reservoir Place, 3rd Floor Great Room, 1601 Trapelo Rd., Waltham, MA (Exit 28B, I-95/Route 128). Pre-meeting Dinner at 5:15 PM (sharp) at Bertucci's, Waltham, (Exit 27B, Route 128)
Check for Updates: Boston Entrepreneurs' Network Website at (http://www.boston-enet.org)
Directions: http://www.constantcontact.com/about-constant-contact/office-location-waltham.jsp

Reservations: ENET Constant Contact meetings are free to ENET members and $20 for non-members. No reservations are needed for the dinner. To expedite sign-in for the meeting, we ask that everyone -- members as well as non-members -- pre-register for the meeting online. Pre-registration is available until midnight the day before the meeting. If you cannot pre-register, you are welcome to register at the door.

Young Professionals – 5:30PM, Wednesday, 7 December

Winter Networking Night

Young Professionals will be hosting a winter networking night on Wednesday, 7 December at 5:30PM. It will be hosted by Mintz Levin and their IP law group at One Financial Center downtown.

This is a great opportunity to meet other young professionals in the IEEE community and learn about plans for expanding the Young Professionals program in the future.

Young professionals are invited to bring along their friends and colleagues for a get-together. Join us for a relaxed evening of drinks, snacks, networking and fun at our Winter Mixer hosted by Mintz Levin. This evening will offer the opportunity for networking, sharing our professional experiences and personal hobbies, and learning from each other.

Meeting Location: Mintz Levin, 1 Financial Center, Floor 38, Boston, MA 02111
Please register at:
https://ieee-yp-winter2016.eventbrite.com.

Also, to assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

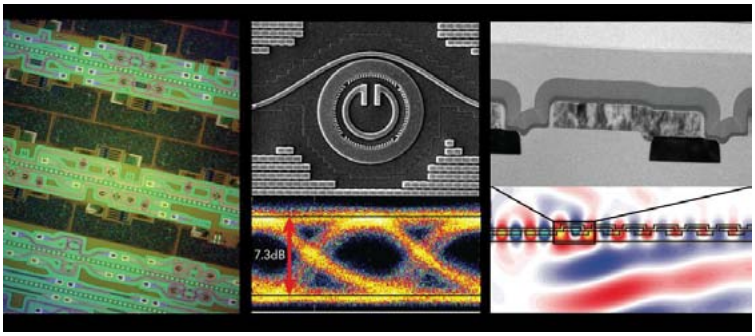
Photonics Society – 6:00PM, Thursday, 8 December

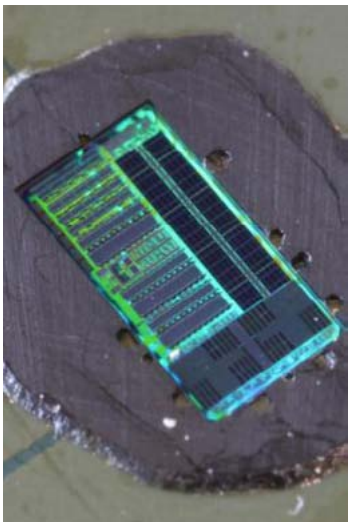
Building the First Microprocessor that Communicates using Light

Prof. Miloš A. Popović - Department of Electrical and Computer Engineering, Boston University

Four decades on from the pioneering first steps at Bell Labs, microphotonics is at a transition from a few components to large-scale integrated systems on chip. In the near term, this can address severe bottlenecks seen in complex digital electronic systems – through integration with relatively simple but efficient photonic systems. In the longer term, tight integration and control means complex passive, active and nonlinear photonic structures enabling novel functions will become practical and may enable a new generation of integrated systems-on-chip for analog signal processing, computation, metrology and sensing.

In this talk, I will describe work on a new CMOS technology that enabled the simultaneous integration of millions of advanced CMOS transistors and thousands of photonic devices side-by-side on a single chip for the first time. The approach, “zero change CMOS photonics”, bucked the trend in the photonics community of tailoring fabrication to design, instead pursuing a “design for manufacture” philosophy to photonic device design within





fixed advanced-node CMOS microelectronics technology. It produced the efficient electronic-photonic systems of unprecedented integration scale, including record-energy optical transmitters, receivers and links, and resulted in the demonstration of the first microprocessor that communicates using light, with significant implications for computer architecture.

I will describe the approach, some of the device innovations and the system demonstrations they made possible, and will address some of the implications of this work in computing and its potential in other domains including datacom, quantum information processing, RF front ends and LIDAR.

Miloš Popović is on the faculty of Electrical Engineering at Boston University since July 2016. Previously he was at the University of Colorado Boulder from 2010 to 2016. He received his B.Sc.E. in Electrical Engineering from Queen's University, Canada in 1999, and the M.S. and Ph.D. degrees from Massachusetts Institute of Technology in 2002 and 2007.

His research interests include first-principles theory and design of integrated photonic devices and circuits, CMOS photonics integration, nano-optomechanical devices based on light forces, mechanical motion and acoustic wave engineering, and nonlinear and quantum integrated photonics. He is author or coauthor of over 25 patents and 150 journal and conference papers. In 2012, he was named a Fellow of the David & Lucile Packard Foundation. He is co-founder and advisor at Ayar Labs.

Directions to Forbes Rd Lincoln Laboratory: (from interstate I-95/Route 128)

- Take Exit 30B onto Marrett Rd in Lexington – Merge into left lane
- Make the first Left onto Forbes Rd.
- Proceed straight through the small rotary and enter the parking lot.
- The entrance is on your right.

To assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

Reliability Society – 5:30PM, Wednesday, 14 December

Microwave and Millimeter Wave Power Amplifiers: Technology, Applications, Benchmarks, and Future Trends

James J. Komiak, Ph.D. of BAE Systems, IEEE Distinguished Lecturer

This event is the Chapter's annual past chairs dinner and monthly meeting. The past chairs dinner recognizes past chairs of the IEEE Boston Reliability Chapter for their years of dedication and contributions to the chapter. Traditionally, this meeting starts with social networking, followed by dinner & announcements followed by a presentation.

Solid State Transistor Device Technology is ubiquitous in communications, radar, electronic warfare,

and instrumentation applications. This abridged presentation will cover Si LDMOS, PHEMT, InP HEMT/MHEMT and GaN HEMT. Content includes principles of operation, structures, characteristics, classes of operation, and device state of the art benchmarks. The art of power amplifier design is approached from a historical perspective. Power amplifiers utilizing these device technologies covering UHF through sub-millimeter wave are described including amplifier state of the art benchmarks. Future trends are highlighted and summarized.

James J. Komiak (M'89-SM'90-F'05) received a Ph.D. in Electrical Engineering from Cornell University in 1978. Dissertation research developed the "Real Frequency Technique" for broadband matching an arbitrary load to a resistive generator. He has 37 years experience in system, module, and MMIC design for EW, communication, and radar applications. Currently he is a BAE Systems Global Engineering/Scientific Fellow at Electronic Systems in Nashua, NH. He has over 100 publications and 12 patents. Elected to the grade of IEEE Fellow in 2005 for "Contributions to Monolithic Microwave Integrated Circuits, High Power Amplifiers, and Transmit/Receive Modules." Received the Martin Marietta Jefferson Cup Award--"Outstanding Technical Leadership in Development and Demonstration of High Power and High Efficiency Monolithic Microwave Integrated Circuit Amplifiers and T/R Modules for Phased Array Radar (June 1993)" and his work is represented in the MTT Symposium MMIC Historical Exhibit "World's First Octave Band MMIC with Power Output in Excess of 10 Watts (1989)". Silver Award Winner of the BAE Systems Chairman's Award for Innovation for "Blue Force Locator & Monitor" (2001) and "Next Generation Power Amplifiers" (2012). Received the BAE Systems Engineering Fellows Leave A Legacy Award (2007). Inducted into the Association of Old Crows Electronic Warfare Technology Hall of Fame in 2008. MTT-S, IMS TPC/TPRC, MTT-5, GaAs IC Symposium (2000 Chairman), former ABET ECE PEV, CEAA. Dr. Komiak is an IEEE MTT-S Distinguished Microwave Lecturer (2014-2016).

This event will be held Wednesday, December 14th at MIT Lincoln Laboratory Forbes Road Facility, 3 Forbes Road, Lexington, MA 02420. It will begin with personal networking at 5:30 PM. The annual dinner will be served at 6:00 PM. The presentation will follow the annual chapter announcements at 6:50 PM. IEEE members and non-members are welcome.

There is no charge for the dinner or presentation but we request that you register to attend by Friday, December 3, so we can finalize dinner arrangements.

Meeting Location: MIT Lincoln Laboratory, 3 Forbes, Road, Lexington, MA

To assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

Locally held IEEE Conferences

2017 IEEE International Symposium on Technolgies for Homeland Security
April 25 - 26, 2017
www.ieee-hst.org
(The technical program will be online by January 1, 2017)

2017 IEEE Hogh performance Extreme Computing Conference HPEC '17
September 12 - 14, 2017
www.ieee-hpec.org
Submission deadline is
May 19, 2017

Life Members - co-sponsored by the New Hampshire Life Members Affinity Group - 4:00PM, Wednesday, 14 December

Re-Balancing Economics with Ethics

Paul H Carr, Ph.D. IEEE Life Fellow, AF Research Laboratory Emeritus

The Golden Rule of ethics must re-balance our economy. At present, those with the gold make the rules.

"Any economic system should serve people, not the other way around" (Pope Francis message to the World Economic Forum 2014).

According to economist Thomas Piketty's recent "Inequality of Capital," the top income earners now have 60% of our national income. From 1942 to 1980, however, the same high income people had only 34%. I will show what happened after 1980 to bring about our present income inequality. It has contributed to the unexpected political success of Donald Trump and Bernie Sanders.

How does income inequality in the US compare with other countries? Is "trickle-up" economics a better way to approach equality than "trickle down?" Adam Smith (1776) proposed that the "invisible hand" of lasses-faire economics led the pursuit of individual gain towards the common good. How can this be balanced with the "Tragedy of the Commons," of William Forster Lloyd (1833), in which the pursuit of individual gain leads to negation of the common good?

Biographical Sketch of Paul H. Carr: BS MIT, PhD Brandeis U, IEEE Life Fellow. From 1967 to 1995, he led the Component Technology Branch of the Air Force Research Laboratory, Bedford, MA. His branch developed the surface acoustic wave (SAW) technology used in compact, signal-processing filters for radar, cell phones, and TV. After his retirement from AFRL, he taught philosophy courses at U Mass Lowell that inspired his book, Beauty in Science & Spirit (2006). He published "Weather extremes from anthropogenic global warming" in Natural Science, Jan 2013 and participated in an IEEE Climate Discussion/Debate on NewTV in August 2014. His web page: www.MirrorOfNature.org

The meeting will be held at the Lincoln Lab Auditorium, 244 Wood Street. Lexington, MA at 4:00 PM and is being co-sponsored by the New Hampshire Life Members Affinity Group.

Refreshments will be served at 3:30 PM. Registration is in the main lobby.

Foreign national visitors to Lincoln Lab require visit requests.

Please pre-register by e-mail to reception@ll.mit.edu and indicate your citizenship.

Also, please register on the IEEEBostonwebsite or at https://docs.google.com/forms/d/1V-AilJpIQcN-FtHRFLVEMNUhuJKiQXUjNESNXoXl0WE/ so we can plan for the meeting and refreshments.

Please use the Wood Street Gate. For directions go to http://www.ll.mit.edu/ For other information, contact Steve Teahan, Steve.F.Teahan@raytheon.com or Paul H. Carr, paulcarr@alum.mit.edu

To assist us in planning this meeting, please pre-register at http://www.ieeeboston.org/Register/.

60th IEEE International Midwest Symposium on Circuits and Systems

Boston, MA, USA | August 6th-9th, 2017
www.mwscas2017.org

Tufts University · DRAPER · IEEE · CAS

CALL FOR PAPERS IEEE INTERNATIONAL MWSCAS 2017

The IEEE International Midwest Symposium on Circuits and Systems is the oldest Circuits and Systems Symposium sponsored by IEEE. The 60th edition will be held on the campus of Tufts University, Boston, MA, USA, August 6 - 9, 2017. MWSCAS 2017 will include oral and poster sessions, student paper contest, tutorials given by experts in circuits and systems topics, and special sessions. Topics include, but are not limited to:

Track 1. Analog Circuits and Systems I
- 1.1 Analog Circuits
- 1.2 Analog Systems
- 1.3 Biomedical Electronics
- 1.4 Bioengineering Systems and Bio Chips
- 1.5 Other Analog Circuits and Systems

Track 2. Analog Circuits and Systems II
- 2.1 Linear Analog Systems
- 2.2 Non-linear Analog Systems
- 2.3 System Architectures
- 2.4 Neuromorphic Systems

Track 3. Digital Circuits and Systems I
- 3.1 Digital Integrated Circuits
- 3.2 System On a Chip (SOC) and Network on a Chip (NOC)

Track 4. Digital Circuits and Systems II
- 4.1 Digital Filters
- 4.2 Hardware-Software Co-Design
- 4.3 Other Digital Circuits and Systems

Track 5. Communications Circuits and Systems
- 5.1 Communications Circuits, Computers and Applications
- 5.2 Communications Systems and Control
- 5.3 Information Theory, Coding and Security
- 5.4 Communications Theory
- 5.5 Other Communications Circuits and Systems

Track 6. RF and Wireless Circuits and Systems
- 6.1 RF Front-End Circuits
- 6.2 Mixed-Signal RF and Analog and Baseline Circuits
- 6.3 Wireless Mobile Circuits and Systems and Connectivity
- 6.4 VCO's and Frequency Multipliers, PLL's and Synthesizers
- 6.5 Other RR and Wireless Circuits and Systems

Track 7. Sensor Circuits and Systems
- 7.1 Technologies for Smart Sensors
- 7.2 Sensor Fusion
- 7.3 Control Systems
- 7.4 Mechatronics and Robotics
- 7.5 Other Sensor Circuits and Systems

Track 8. Converter Circuits and Systems
- 8.1 Analog to Digital Converters
- 8.2 Digital to Analog Converters
- 8.3 DC-DC Converters
- 8.4 Other Converter Circuits and Systems

Track 9. Signal and Image Processing
- 9.1 Analog and Mixed Signal Processing
- 9.2 Digital Signal Processing
- 9.3 Signal Processing Theory and Methods
- 9.4 Image, Video and Multi-Dimensional Signal Processing
- 9.5 Other Signal and Image Processing

Track 10. Hardware Design
- 10.1 Processor and Memory Design
- 10.2 MEMS/NEMS
- 10.3 Nano-Electronics and Technology
- 10.4 Optics and Photonics
- 10.5 Power Management, Power Harvesting and Power Electronics
- 10.6 Photovoltaic Devices/Panels and Energy Harvesting

Track 11. Hardware Security
- 11.1 Hardware Authentication and Physically Unclonable Functions (PUFs)
- 11.2 Trusted Microelectronics
- 11.3 Hardware Anti-Tamper
- 11.4 Architectural System Security
- 11.5 Other Hardware Security

Prospective authors are invited to submit a full paper (4 pages) describing original work. Only electronic submissions will be accepted. Papers should include title, abstract, and topic category from the list above in standard IEEE two-column format for consideration as lecture or poster. Both formats have the same value, and presentation method will be chosen for suitability. All submissions should be made electronically through the MWSCAS 2017 web site (http://www.mwscas2017.org). Students are encouraged to participate in the best student paper award contest. Accepted papers will be published in the conference proceedings subject to advance registration of at least one of the authors.

IMPORTANT DATES

March 18: Tutorial and Special Session proposals deadline
March 18: Regular and Student paper submission deadline
April 1: Special session and invited paper submission deadline
April 29: Notice of acceptance
May 20: Final camera-ready paper deadline

www.mwscas2017.org

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www.ieee-hpec.org

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IEEE Boston Section

The IEEE High Performance Extreme Computing Conference (HPEC '17) will be held in the Greater Boston Area, Massachusetts, USA on 12 – 14 September 2017. The HPEC charter is to be the premier conference in the world on the confluence of HPC and Embedded Computing.

The technical committee seeks new presentations that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- Advanced Multicore Software Technologies
- Case Studies and Benchmarking of Applications
- Automated Design Tools
- Mapping and Scheduling of Parallel and Real-Time Applications
- Computing Technologies for Challenging Form Factors
- ASIC and FPGA Advances
- Open System Architectures
- Data Intensive Computing
- Big Data and Distributed Computing
- Interactive and Real-Time Supercomputing
- Graph Analytics and Network Science
- Fault-Tolerant Computing
- Embedded Cloud Computing
- Digital Front Ends
- General Purpose GPU Computing
- Advanced Processor Architectures
- Secure Computing & Anti-Tamper Technologies
- New Application Frontiers
- High Performance Data Analysis
- Cloud HPEC
- Big Data Meets Big Compute

HPEC accepts two types of submissions:

1. Full papers (up to 6 pages, references not included), and
2. Extended abstract (up to 2 pages, references included).

IMPORTANT DATES:

Submission Deadline: **May 19, 2017**
Notification of Acceptance: **June 16, 2017**

Preference will be given to papers with strong, quantitative results, demonstrating novel approaches or describing high quality prototypes. Authors of full papers can mark their preference for a poster display or an oral presentation. Presenters who wish to have hardware demonstrations are encouraged to mark their preference for a poster display. Accepted extended abstracts will be displayed as posters. All paper and extended abstract submissions must use the approved IEEE templates. Full paper submissions with the highest peer review ratings will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions and extended abstracts are published on ieee-hpec.org. Vendors are encouraged to sign up for vendor booths. This will allow vendors to present their HPEC technologies in an interactive atmosphere suitable for product demonstration and promotion.

We welcome input (hpec@ieee-hpec.org) on tutorials, invited talks, special sessions, peer reviewed presentations, and vendor demos. Instructions for submitting will be posted on the conference web site shortly.

Last Notice Before Course Begins, Please Register Now!!!!

Practical RF PCB Design: Wireless Networks, Products and Telecommunications

Date & Time: Thursday & Friday, December 15 & 16; 9AM - 4:30PM

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Henry Lau, Lexiwave Technology

Overview: One of the most demanding consumer products in the market is the wireless telecommunication product. A well-designed Radio Frequency Printed Circuit Board (RF PCB) contributes significantly to the success of any wireless product as the layout of the PCB greatly affects the performance, stability and reliability of the product. In today's highly competitive wireless products market with increasingly compressed development time-frame, there is a strong demand for RF professionals who possess the knowledge and experience to design top-performing RF PCBs in less number of iterations. What matters is whether your level of competence is up to the required standard to meet such demand.

Audience: RF Designers, Wireless Product Designers, Field Application Engineers, Design Managers and related professionals.

Benefits: This course aims to provide participants with an insightful training on RF PCB design from a practical, industrial perspective. Participants will be led through a systematic, theoretical presentation with case studies on commercial products in the training. The course will be conducted by an RF expert with rich industrial experience. It is suitable for RF professionals who want to keep up-to-date their skills and knowledge in RF PCB design and stay competitive.

OUTLINE

1. Printed circuit board design for RF circuits
From product design, circuit design to PCB design
Layer stack-up assignment
Grounding methods and techniques
Interconnects and I/O
Bypassing and decoupling
Partitioning methods

2. Printed circuits board design for other circuits
Clock circuits
Base-band circuits
Audio circuits
Power supplies
Impedance-controlled circuits

3. PCB design for EMC/EMI compliance
EMC/EMI compliance
Grounding methods
Decoupling methods
Shielding methods

4. Additional Design Techniques
Production concerns
Systematic product design approach
RF Modules
Evaluation boards
Other RF concerns
Casing design

5. Case studies

Expertise:

Henry Lau received his M.Sc. and MBA degrees from UK and USA respectively. He has more than 25 years of experience in designing RF systems, products and RFICs in both Hong Kong and US. He worked for Motorola and Conexant in US as Principal Engineer on developing RFICs for cellular phone and silicon tuner applications. Mr Lau holds five patents all in RF designs. He is currently running Lexiwave Technology, a fables semiconductor company in Hong Kong and US designing and selling RFICs, RF modules and RF solutions. He has also been teaching numerous RF-related courses internationally.

Decision (Run/Cancel) Date for this Courses is Friday, December 9, 2016

Payment received by December 5
IEEE Members $405
Non-members $435

Payment received after December 5
IEEE Members $435
Non-members $455

http://ieeeboston.org/practical-RF-PCB-Design/

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.

If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at sec.boston@ieee.org or 781 245 5405.

- Honoraria can be considered for course lecturers
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Advanced Embedded Linux Optimization

Time & Date: 6 - 9PM, Mondays, January 9, 16, 23, 30, 2017

Location: Crowne Plaza Hotel, 15 Middlesex Canal Park Road, Woburn, MA

Speaker: Mike McCullough, RTETC, LLC

Course Summary - This 4-day technical training course provides advanced training in the debugging, testing, profiling and performance optimization of Embedded Linux software. The first part of the course focuses on advanced debugging, testing and profiling in an Embedded Linux context with a focus on using Eclipse, Backend Debuggers, JTAG and In-Circuit Emulators as well as Kernel Logging capabilities and Kernel Hacking. The latter part of the course covers performance measurement and optimization affecting boot, memory, I/O and CPU performance and key performance optimization tools for Embedded Linux software including the perf tool, advanced cache usage and compiler-based optimization.

Who Should Attend - The course is designed for real-time engineers who are developing high-performance Linux applications and device drivers using Embedded Linux distributions. It is also targeted at experienced developers requiring a refresher course on Advanced Embedded Linux optimization.

Course Objectives

- To understand methods for debugging, profiling and testing Embedded Linux software.
- To provide an overview of Linux application performance measurement and optimization.
- To understand the tools used for performance optimization of Embedded Linux software.
- To give students the confidence to apply these concepts to their next Embedded Linux project.

OUTLINE

Course Schedule Day 1

Getting Started with Embedded Linux
Linux and the GPL
Building the Kernel Source Code
Embedded Linux Kernels
BSPs and SDKs
Linux References (Books and Online)
Basic Debugging Review
Embedded Applications Debugging
GDB, GDB Server and the GDB Server Debugger
An Eclipse Remote Debug Example
Debugging with printk and LTTng
System Logs
Other Debuggers
System-Level Debug
System-Level Debug Tools
The /proc and /sys Filesystems
Basic Logging
KGDB and KDB
Crash Dumps and Post-Mortem Debugging
Debugging Embedded Linux Systems
Backend Debuggers
JTAG and In-Circuit Emulators
Hardware Simulators
Analyzers
Debugging Device Drivers
Kernel Probes
Kexec and Kdump
Kernel Profiling

Course Schedule Day 2

Testing
Design for Test
Agile Software Design
Unit-Level Testing
System-Level Testing
Code Coverage Tools
gcov
Automated Testing
DebugFS
Configuring DebugFS
DebugFS Capabilities
Advanced Logging
LogFS
Using Logwatch and Swatch
Using syslogd and syslog-ng

Kernel Hacking
Configuring Kernel Hacking
Kernel Hacking Capabilities
Tracing
ptrace and strace
New Tracing Methods
SystemTap
Ftrace, Tracepoints and Event Tracing
Tracehooks and utrace

Course Schedule Day 3

Profiling
Basic Profiling
gprof and Oprofile
Performance Counters
LTTng
Another DDD Example
Manual Profiling
Instrumenting Code
Output Profiling
Timestamping
Measuring Embedded Linux Performance
Some Ideas on Performance Measurement
Common Considerations
Uncommon Considerations
Using JTAG Methods
BootLoader Optimizations
Boot Time Measurements
Effective Memory and Flash Usage
Filesystem Choices
Addressing Performance Problems
Types of Performance Problems
Using Performance Tools to Find Areas for Improvement
Application and System Optimization
Device Driver Optimization
CPU Usage Optimization
Memory Usage Optimization
Disk I/O and Filesystem Usage Optimization
The Perf Tool
Improving Boot Performance
Boot Time Optimization
The Linux Fastboot Capability
Building a Smaller Linux
Building a Smaller Application
Filesystem Tips and Tricks
Some Notes on Library Usage
Performance Tool Assistance
Recording Commands and Performance
System Error Messages and Event Logging
Dynamic Probes
User Mode Linux and Virtualization

Course Schedule Day 4

Improving CPU Performance
Run Queue Statistics
Context Switches and Interrupts
CPU Utilization
Linux Performance Tools for CPU
Process-Specific CPU Performance Tools
Stupid Cache Tricks
Improving System Memory Performance
Memory Performance Statistics
Linux Performance Tools for Memory
Process-Specific Memory Performance Tools
More Stupid Cache Tricks
Improving I/O and Device Driver Performance
Disk, Flash and General File I/O
Improving Overall Performance Using the Compiler
Basic Compiler Optimizations
Architecture-Dependent and Independent Optimization
Code Modification Optimizations
Feedback Based Optimization
Application Resource Optimization
The Hazard of Trust
An Iterative Process for Optimization
Improving Development Efficiency
The Future of Linux Performance Tools
Some Final Recommendations

Decision (Run/Cancel) Date for this Courses is Friday, December, 30, 2016

Payment received by December 27
IEEE Members $395
Non-members $415

Payment received after December 27
IEEE Members $415
Non-members $435

http://ieeeboston.org/advanced-embedded-linux-optimization/

Call for Technical Articles

Now that the Reflector is all electronic, we are expanding the content the publication. One of the new features we will be adding are technical and professional development articles of interest to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional articles will be reviewed by the publications committee for suitability.The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to; eeebostonsection@gmail.com