Boston Section

Supporting students, working engineers and retirees through professional development, education and resources.

THE Reflector

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IEEE
Boston Section

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Robert's Rules

By Dr. Karen Panetta, Editor, *The Reflector*

So many people are afraid of taking risks or doing new things for the fear of failure. As engineers, we try to say we are aware that failure is integral to being an engineer. Still, no matter how many times we say it, it doesn't remove the sting when we do fail. We manage to get back up, and limp forward with our head held high, but often proceed with caution when another opportunity arises.

I have found that I am more willing to take on a new volunteer role when I know there is someone behind the scenes to help guide me through the valley of death.

In the IEEE Boston Section, that individual has been Robert (Bob) Alongi, our long time IEEE Boston Section Manager. We are very fortunate that our section has a full-time manager. Other IEEE sections often tell me how "rich" the Boston section is to be able to have a "Bob."

Bob was hired by past IEEE-President and our own esteemed Boston Section volunteer Dr. Arthur Winston. Since Arthur is known for his impeccable ability to identify outstanding talent, we knew that we had a winner in selecting Bob to organize the herd of cats (volunteers) in the section.

Well, thanks to Bob, our section volunteers have learned to juggle professional education programs, students support initiatives, numerous society events and develop sustainable productive industry collaborations. And yes, with Bob's help, every conference he touches is a financial success because he ensures we learn key skills in planning, budgeting and keeping our volunteers on task.

Bob sounds more like a volunteer leader rather than a full-time staff person, whose job it is to keep an innovative group of deep thinkers grounded in financial stability. He is an integral part of our team and is the "Mr. Wizard" of forecasting the financials for the section.

I believe one of the most difficult aspects of his job is telling an individual who holds a PhD and tends to believe they are an expert in everything and are never wrong, that they are, well, wrong!

Bob does this with great finesse by asking questions that help lead that “expert” to understand the flaw in their perfectionist logic. I have witnessed many a financial disaster averted because of the “Robert (Alongi) rules” of financial awareness trainings.

For many years, I considered volunteer roles like auditor and treasurer to be boring roles for trolls. However, when my IEEE societies and boards needed a willing victim to turn to the dark side and take on these roles, I stepped forward because I had gained experience in the Boston section with Bob behind me as a safety net. Besides, I am a natural when it comes to spending money, so how hard could it be?

Coming into a new role requires acceptance that mistakes will be made and that we must not be afraid to ask questions or ask for help. Bob has always been there in the Boston section as a resource for all of us to ask questions, and to listen to our financially insane and infeasible project proposals. He has done this without making us feel like we are so clueless that we should have our engineering degrees revoked. He has educated us, kept us operating as a tight knit team and made being part of the section feel like home.

The IEEE Boston Section has won several awards for its excellence and chapter successes. While the leaders of the IEEE Boston section often receive the credit for these awards, we all know that it would not have been possible without the infrastructure and support Bob has created for us.

Bob Alongi thinks he is going to retire soon, but as I mentioned, we have always had trouble distinguishing Bob as a staff person versus a volunteer. While Bob may officially retire, we fully expect he will continue to engage with the Section. I say this with confidence because I am one of those individuals with a PhD, who is an expert and am never wrong.

Thank you, Bob, for all you have done for the IEEE Boston Section!

IEEE Boston Section Awards
Call for Nominations

Deadline Extended to August 20, 2024

The IEEE Boston Section is seeking qualified candidates for its section awards.
The three section awards are

- **Distinguished Service Award**
- **Distinguished Member Award**
- **Student Achievement Award**

More information about the awards can be found here:
https://ieeeboston.org/ieee-boston-section-awards/

Consumer Technology Society
Call for Volunteers!

We are currently looking for volunteers who would be interested in pushing forward the mission of the Consumer Technology (CT-S), Boston Chapter. The chapter is looking for volunteers to help organize chapter meetings and help meet the needs of the local CT-S member needs.

The Boston Section is organizing chapters into groups of similar technical interest areas to pool their resources for easier and better chapter collaboration in planning the chapter events.

If you have interest in volunteering for a chapter leadership position or are interested in learning more about what these volunteer positions may entail, please send an email to Karen Safina in the IEEE Boston Section office at, ieeebostonsection@gmail.com

Aakash Deliwala, Chair, IEEE Boston Consumer Technology Chapter

Engineering in Medicine & Biology Society
Call for Volunteers!

We are currently looking for volunteers who would be interested in pushing forward the mission of the Engineering in Medicine & Biology Society (EMBS), Boston Chapter. The EMBS - Boston Chapter was recently approved in July 2021, and we're looking to make a significant impact in the area of Biomedicine, Bioengineering, and Biotechnology in the region. The chapter is looking for volunteers to help organize chapter meetings and help meet the needs of the local EMBS members.

The Boston Section is organizing chapters into groups of similar technical interest areas to pool their resources for easier and better chapter collaboration in planning the chapter events.

If you have interest in volunteering for a chapter leadership position or are interested in learning more about what these volunteer positions may entail, please send an email to Karen Safina in the IEEE Boston Section office at, ieeebostonsection@gmail.com.

Aseem Singh, Marie Tupaj, Co-Chairs, Boston EMBS Chapter

IEEE Boston Section Online Courses:

(Students have 180 day access to all online, self-paced courses)

Electronic Reliability Tutorial Series
Full course description and registration at ,
http://ieeeboston.org/electronic-reliability/

Introduction to Embedded Linux Part I
Full course description and registration at ,
http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/

Embedded Linux Optimization - Tools and Techniques
Full course description and registration at ,
http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/

Embedded Linux Board Support Packages and Device Drivers
Full course description and registration at ,
http://ieeeboston.org/embedded-linux-bsps-device-drivers-line-course/

Software Development for Medical Device Manufacturers
Full course description and registration at ,
http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/

Fundamental Mathematics Concepts Relating to Electromagnetics
Full course description and registration at ,
http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/

Reliability Engineering for the Business World
Full course description and registration at ,
http://ieeeboston.org/reliability-engineering-business-world-line-course/

Design Thinking for Today's Technical Work
http://ieeeboston.org/design-thinking-technical-work-line-course/

Fundamentals of Real-Time Operating Systems
http://ieeeboston.org/fundamentals-of-real-time-operating-systems-rt201-on-line-course/

NEW

Reliability Tutorial Series: Electronic Failure Mechanisms
https://ieeeboston.org/event/ieee-ansys-reliability-tutorial-series-electronic-reliability/?instance_id=3635

NEW

Reliability Tutorial Series – Accelerated Life Testing for Electronics Reliability
https://ieeeboston.org/event/ieee-ansys-reliability-tutorial-series/?instance_id=3634

ANNOUNCEMENT

2024 IEEE International Symposium on Phased Array Systems and Technology

IEEE

15 - 18 October 2024
Hynes Convention Center, Boston, Massachusetts, USA
www.ieee-array.org

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About the Symposium

Phased array systems continue to be a rapidly evolving technology with steady advances motivated by the challenges presented to modern military and commercial applications. This symposium will present the most recent advances in phased array technology and offer a unique opportunity for members of the international community to interact with colleagues in the field of phased array systems and technology.

The committee is thrilled to announce two major changes to the symposium to better reflect the interest and pace of technology development: (1) moving to the larger Hynes Convention Center in the Back-Bay neighborhood of Boston; and (2) increasing the symposium frequency to a two-year cadence.

Be a Symposium Sponsor or Exhibitor

For sponsorship and exhibit opportunities please reach out to Mark McClure and Marc Angelucci at: sponsorships@ieee-array.org.

Session Topics

- 5G Arrays
- Array Design
- Array Measurements
- Array Signal Processing
- Automotive Arrays
- Beamforming & Calibration
- Digital Array Architectures
- Dual Polarized Arrays
- Low-Cost Commercial Arrays
- MIMO Arrays
- Medical Applications
- Metamaterial Phased Arrays
- mmWave and Terahertz
- T/R Modules
- SATCOM Arrays

Special Sessions

- European Phased Arrays
  - *Michael Brandfass & Alfonso Farina*
- Commercial Satellite Arrays
  - *Gabriel Rebeiz & Will Moulder*
- Wideband Arrays
  - *Justin Kasemodel & John Volakis*
- Low Frequency Arrays
  - *Cecelia Franzini & Eric Robinson*
- Weather Arrays
  - *Caleb Fulton & Matt Harger*
- EurAAP Lens-Array Combination
  - *Stefania Monni & Oscar Quevedo*
- 3D Printing Techniques for Phased Arrays
  - *Esteban Menargues & Maria Garcia-Vigueras*

Committee

Symposium Chairs
Sean Duffy (C), MIT LL
Wajih Elsallal (VC), MITRE

Technical Program Chairs
David Mooradd (C), MIT LL
Glenn Hopkins (VC), GTRI

Special Sessions Chairs
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Kenneth E. Kolodziej, MIT LL

Plenary Session Chair
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William Weedon, Applied Radar

Student Paper Competition
Matilda Livadaru, Raytheon
Justin Kasemodel, Raytheon

Tutorials
Cara Kataria, MIT LL
Frank Vliet, TNO

Sponsorship and Exhibits
Marc Angelucci, LMC
Mark McClure, STR

Digital Platforms Chairs
Pierre Dufilie, Raytheon
Jacob Houck, GTRI
Mark Fosberry, MITRE
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Jack Logan, NRL
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Poster Sessions Chair
Honglei Chen, MathWorks

Advisors
Daniel Culkin, NGC
Alan J. Fenn, MIT LL
Jeffery S. Herd, MIT LL
Bradley Perry, MIT LL

Arrangements/ Administration
Robert Alongi, IEEE Boston
Kathleen Ballos, Ballos Assoc.

IEEE Video Series

A collaborative discussion panel featuring esteemed members from the Institute of Electrical and Electronics Engineers has convened in 2021 to produce educational video presentations that embrace IEEE's mission of advancing technology for humanity.

Among the programs they've produced include "Electric Vehicles: Fun Saving Our Planet", "Greener Power For More Electric Vehicles", "Overcoming Nuclear Fears To Achieve Net Zero CO2 By 2050" and "Achieving a Net Zero Carbon Future", "Green Energy's Economic Progress", and "Net-Zero CO2 with Nuclear, Hydrogen and Geothermal". Projects currently in production include the expansive topic of futurology, with a focus on increasing the efficiency and transformation of aging electrical power generating stations and infrastructure to accommodate nuclear power; reviewing the viability of alternative energy (such as geothermal, wind and solar); and focusing on 'cleaner' fossil fuels that are more environmentally-friendly to slow the rate of climate change.

These shows are produced and directed by Lennart E. Long, IEEE Senior Life Member from the Executive Committee and Past Chair of the Boston Section; Dr. Paul H Carr, BS, MS, MIT; PhD Brandeis U, IEEE Life Fellow; Dr. Ted Kochanski, SB (MIT), Ph.D (U.Texas, Austin), IEEE Global Education for Microelectronic Systems and former Boston Section Chair; and Dr. Ken Laker, B.E. (Manhattan College), M.S. and Ph.D. (New York University), IEEE Life Fellow and past President of IEEE.

The panel is moderated by five-time Boston/New England Emmy Award-winner and television personality and star of "The Folklorist," John Horrigan. These video programs with presentations and discussions can be accessed at the IEEE Boston Section video portal at https://vimeo.com/user18608275.

We are looking for any IEEE members that would like to appear on the program in the role of presenter or discussion expert. Simply reach out to Robert Alongi at the Boston Section at, ieeebostonsection@gmail.com.

Call for Articles

Now that the Reflector is all electronic, we are expanding the content of the publication. One of the new features we will be adding are technical, professional development, and general interest articles to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development or general interest articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional/interest articles will be reviewed by the Publications Committee for suitability.The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to;
ieeebostonsection@gmail.com

IEEE Boston Section Volunteers Wanted!

Are you passionate about technology and eager to contribute to the advancement of your field? The IEEE Boston Section is excited to announce a call for volunteers to join our dynamic team of professionals and enthusiasts. By becoming a volunteer, you'll have the opportunity to collaborate with like-minded individuals, develop new skills, and make a meaningful impact on the local technology community.

About IEEE Boston Section:
The IEEE Boston Section is a thriving community of engineers, researchers, students, and industry professionals dedicated to promoting technological innovation and knowledge sharing. Our section hosts a variety of events, workshops, seminars, and conferences throughout the year, providing members with opportunities to learn, network, and stay updated on the latest developments in their fields.

Volunteer Opportunities:
We are currently seeking volunteers to help on the following committees:

The Fellow and Awards Committee - activities include recommending qualified members of the Section for advancement to Fellow grade and for receipt of the various IEEE (IEEE/Region/MGA/Section) awards. Identifying and building a database of the various IEEE awards available for nomination and searching out qualified candidates, for preparing the necessary written recommendations, and for assembling all required supporting documentation and submit its recommendations directly to the appropriate IEEE body.
Time Commitment: Meets 4 times a year for 1 – 2 hours per meeting (virtual or in person)

Local Conferences Committee - activities include identifying timely topical areas for conference development. Identify champions of these conferences to run the identified conference organizing committees. The section local conference committee is not charged with organizing and executing individual conferences.
Time Commitment: Meets 4 times per year 1 – 2 hours per meeting (virtual or in person)

Professional Development & Education Committee - activities include identifying topics, speakers, and/or organizers for appropriate technical lecture series or seminars. The subject matter should be timely, of interest to a large segment of the membership, and well organized with regard to speakers and written subject matter.
Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

The Membership Development Committee - activities include actively promoting membership in the IEEE and shall encourage members to advance to the highest grade of membership for which they are qualified. To these ends this committee shall include wide representation within the Section territory, shall maintain lists of prospects and members qualified for advancement, and shall provide information and assistance to preparing applications.
Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Student Activities Committee - activities include attracting a broad and diverse group of undergraduate and graduate students to IEEE and to engage them in activities that promote their own professional development as well as the ongoing growth of IEEE. The Student Activities Committee shall include among its members the IEEE Counselors at the universities, colleges, and technical institutes that lie within the Section territory. It shall be responsible for liaison with the Student Branches at these institutions and advise the Executive Committee on all other matters affecting the Student Members of the Section.
Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Young Professionals Affinity Group - activities include organizing programs, and initiatives aimed to address the needs of early-career professionals pursuing technology-related careers in engineering, business, management, marketing, and law. This committee is committed to helping young professionals evaluate their career goals, polish their professional image, and create the building blocks of a lifelong and diverse professional network.
Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Benefits of Volunteering:
Volunteering with IEEE Boston Section offers numerous benefits, including:

- Networking opportunities with professionals in your field.
- Skill development and enhancement through hands-on experience.
- Contribution to the local technology community and its growth.
- Access to cutting-edge information and discussions.

How to Get Involved:
If you're enthusiastic about technology and want to make a difference, we invite you to join us as a volunteer. To express your interest and learn more about specific roles, please visit our website and fill out the volunteer application form. Our team will get in touch with you to discuss opportunities that align with your interests and skills.

Thank you for considering this opportunity to contribute to the IEEE Boston Section. Your dedication and passion are what drive the success of our community and its impact on the world of technology.

Volunteer Here!
https://ieeeboston.org/volunteer/

JOIN US!

Are you ready to dive into the world of cutting-edge technology and innovation?
Look no further – the IEEE HPEC 2024 VIRTUAL conference is just around the corner!

This is your opportunity to connect with and learn from some of the brightest minds in the field.

2024 Distinguished Speakers

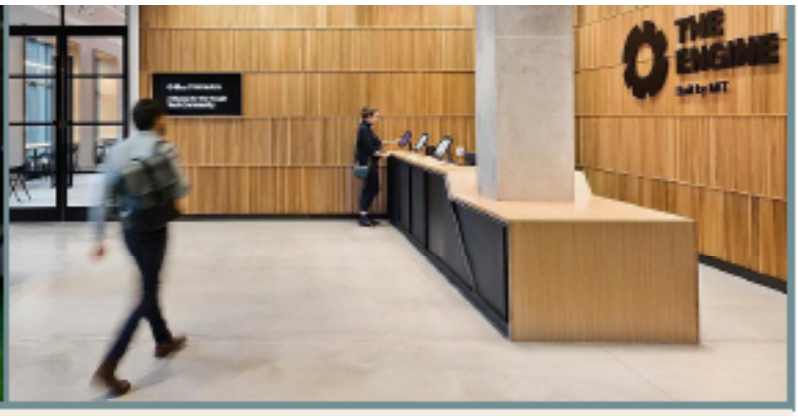
- Dr. Eric Evans (Fmr Director MIT Lincoln Laboratory, Chair Defense Science Board, IEEE & AIAA Fellow, NAE)
- Prof. Peter Fisher (MIT Vice Provost & Assoc VP for Research Computing & Data, AAAS & APS Fellow)
- Prof. Shafi Goldwasser (Director Simons Theory of Computing Institute, ACM A.M. Turing Award, AAAS, NAS, NAE)
- Gary Grider (Los Alamos National Laboratory HPC Dept. Division Leader)
- Robert Knake (Fmr Deputy National Cyber Director, White House Director Cybersecurity)
- Dr. Dan Stanzione (University of Texas Assoc VP for Research & Director Advanced Computing Center)
- Dr. Scott Yockel (Harvard University Research Computing Officer)

Visit the conference website **ieee-hpec.org** to complete your registration and learn more about the conference program, speakers, workshops, and more.

REGISTER NOW!

Early Bird discount ends September 8

IEEE-HPEC.ORG



IEEE SiPS 2024

IEEE Workshop on Signal Processing Systems

4–6 November 2024
Cambridge, Massachusetts, U.S.A.

The 37th IEEE Workshop on Signal Processing Systems (SiPS) is a premier international forum in the area of design and implementation of signal processing systems. It addresses all aspects of architecture and design methods of these systems. Emphasis is on current and future challenges in research and development in both academia and industry.

Submitting a Paper

We invite prospective authors to submit original papers (up to 6 pages) in areas including, but not limited to:

Software Implementation of Signal Processing Systems
- Software on programmable digital signal processors
- Application-specific instruction-set processor (ASIP) architectures and systems
- SIMD, VLIW, and multi-core CPU architectures
- GPU-based massively parallel implementations

Hardware Implementation of Signal Processing Systems
- Low-power signal processing circuits and applications
- High-performance VLSI systems
- FPGA and reconfigurable architecture-based systems
- System-on-chip and network-on-chip
- VLSI for sensor network and RF identification systems
- Quantum signal processing
- Processing-in-memory signal processing systems

Design Methods of Signal Processing Systems
- Optimization of signal processing algorithms
- Compilers and tools for signal processing systems
- Algorithm-to-architecture transformation
- Dataflow-based design methodologies
- Error-tolerant techniques for signal processing

Machine Learning for Signal Processing
- Circuits and systems for AI
- Deep learning/machine learning/AI algorithms
- Tools/platforms for AI
- Transfer learning
- Distributed/federated learning
- Hardware/neuromorphic accelerators
- Hardware/software co-design and automation for AI

Signal Processing Application Systems
- Audio, speech, and language processing
- Biomedical signal processing and bioinformatics
- Image, video, and multimedia signal processing
- Information forensics, security, and cryptography
- Sensing and sensor signal processing
- Signal processing for non-volatile memory systems
- Latency-and power-constrained signal processing
- Wireless communications and MIMO systems
- Coding and compression
- Signal processing for mixed-signal technologies

Important Dates

Technical Papers:	03 April 2024
Paper Notifications:	26 June 2024
Special Session Proposals:	31 July 2024
Tutorial Proposals:	31 July 2024

Committee

General Chairs
John McAllister, QUB
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Program Chairs
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Local Organizing Chair
Brian Telfer, MIT Lincoln Laboratory

eee-sips.org

IEEE CAS IEEE Signal Processing Society

Introduction to Neural Networks and Deep Learning (Part I)

Web-based Course with live Instructor!

Times & Dates: 8:30AM - 12:30PM ET, Saturday, October 26, 2024

Speaker: CL Kim

Course Format: Live Webinar, 4 hours of instruction!

Series Overview: Neural networks and deep learning currently provides the best solutions to many problems in image recognition, speech recognition, and natural language processing."

Reference book: "Neural Networks and Deep Learning" by Michael Nielsen, http://neuralnetworksanddeeplearning.com/

This Part 1 and the planned Part 2 (to be confirmed) series of courses will teach many of the core concepts behind neural networks and deep learning.

More from the book introduction: We'll learn the core principles behind neural networks and deep learning by attacking a concrete problem: the problem of teaching a computer to recognize handwritten digits. …it can be solved pretty well using a simple neural network, with just a few tens of lines of code, and no special libraries."

"But you don't need to be a professional programmer."

The code provided is in Python, which even if you don't program in Python, should be easy to understand with just a little effort.

Benefits of attending the series:
* Learn the core principles behind neural networks and deep learning.
* See a simple Python program that solves a concrete problem: teaching a computer to recognize a handwritten digit.
* Improve the result through incorporating more and more core ideas about neural networks and deep learning.
* Understand the theory, with worked-out proofs of fundamental equations of backpropagation for those interested.
* Run straightforward Python demo code example.

The demo Python program (updated from version provided in the book) can be downloaded from the speaker's GitHub account. The demo program is run in a Docker container that runs on your Mac, Windows, or Linux personal computer; we plan to provide instructions on doing that in advance of the class.

(That would be one good reason to register early if you plan to attend, in order that you can receive the straightforward instructions and leave yourself with plenty of time to prepare the Git and Docker software that are widely used among software professionals.)

Course Background and Content: This is a live instructor-led introductory course on Neural Networks and Deep Learning. It is planned to be a two-part series of courses. The first course is complete by itself and covers a feedforward neural network (but not convolutional neural network in Part 1). It will be a pre-requisite for the planned Part 2 second course. The class material is mostly from the highly-regarded and free online book "Neural Networks and Deep Learning" by Michael Nielsen, plus additional material such as some proofs of fundamental equations not provided in the book.

Outline:
Feedforward Neural Networks.
* Simple (Python) Network to classify a handwritten digit
* Learning with Stochastic Gradient Descent
* How the backpropagation algorithm works
* Improving the way neural networks learn:
    ** Cross-entropy cost function
    ** Softmax activation function and log-likelihood cost function
    ** Rectified Linear Unit
    ** Overfitting and Regularization:
        *** L2 regularization
        *** Dropout
        *** Artificially expanding data set

Pre-requisites: There is some heavier mathematics in learning the four fundamental equations behind backpropagation, so a basic familiarity with multivariable calculus and matrix algebra is expected, but nothing advanced is required. (The backpropagation equations can be also just accepted without bothering with the proofs since the provided Python code for the simple network just make use of the equations.) Basic familiarity with Python or similar computer language.

Speaker Background: CL Kim works in Software Engineering at CarGurus, Inc. He has graduate degrees in Business Administration and in Computer and Information Science from the University of Pennsylvania. He had previously taught for a few years the well-rated IEEE Boston Section class on introduction to the Android platform and API.

Decision (Run/Cancel) Date for this Course is Friday, October 18, 2024

Payment	on/by Oct. 1	After Oct. 1
IEEE Members	$95	$110
Non-members	$115	$130

https://ieeeboston.org/event/neuralnetworks/?instance_id=3598

NOMINATE A COLLEAGUE FOR AN IEEE BOSTON SECTION AWARD

More information about the awards can be found here,
https://ieeeboston.org/ieee-boston-section-awards/

The deadline for nominations is August 20, 2024

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.
If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- **Honoraria can be considered for course lecturers**
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Python Applications for Digital Design and Signal Processing

Dates & Times: **Live Workshops: 6:00 - 7:30PM ET; Thursdays, September 5, 12, 19 & 26**
First Video Release, Thursday, Aug. 29, 2024, additional videos released weekly in advance of that week's live session!

Speaker: **Dan Boschen**

Location: **Zoom**

This is a hands-on course combining pre-recorded lectures with live Q&A and workshop sessions in the popular and powerful open-source Python programming language.
Course Information will be distributed on Thursday, August 19, 2024 in advance of and in preparation for the first live workshop session.
Attendees will have access to the recorded session and exercises for two months (until December 26, 2024) after the last live session ends!

New Format with Pre-Recorded Videos: The course format has been updated to release pre-recorded video lectures that students can watch on their own schedule, and an unlimited number of times, prior to live Q&A workshop sessions on Zoom with the instructor. The videos will also be available to the students for viewing for up to two months after the conclusion of the course.

Overview: Dan provides simple, straight-forward navigation through the multiple configurations and options, providing a best-practices approach for quickly getting up to speed using Python for modelling and analysis for applications in signal processing and digital design verification. Students will be using the Anaconda distribution, which combines Python with the most popular data science applications, and Jupyter Notebooks for a rich, interactive experience.

The course begins with basic Python data structures and constructs, including key "Pythonic" concepts, followed by an overview and use of popular packages for scientific computing enabling rapid prototyping for During the course students will create example designs including a sigma delta converter and direct digital synthesizer both in floating point and fixed point. This will include considerations for cycle and bit accurate models useful for digital design verification (FPGA/ASIC), while bringing forward the signal processing tools for frequency and time domain analysis.

Jupyter Notebooks: This course makes extensive use of Jupyter Notebooks which combines running Python code with interactive plots and graphics for a rich user experience. Jupyter Notebooks is an open-source web-based application (that can be run locally) that allows users to create and share visually appealing documents containing code, graphics, visualizations and interactive plots. Students will be able to interact with the notebook contents and use "take-it-with-you" results for future applications in signal processing.

Target Audience: This course is targeted toward users with little to no prior experience in Python, however familiarity with other modern programming languages and an exposure to object-oriented constructs is very helpful. Students should be comfortable with basic signal processing concepts in the frequency and time domain. Familiarity with Matlab or Octave is not required, but the equivalent operations in Python using the NumPy package will be provided for those students that do currently use Matlab and/or Octave for signal processing applications.

Benefits of Attending / Goals of Course: Attendees will gain an overall appreciation of using Python and quickly get up to speed in best practice use of Python

Topics / Schedule:

Pre-recorded lectures (3 hours each) will be distributed Friday prior to each week's workshop dates. Workshop/ Q&A Sessions are 6 - 7pm on the dates listed below:

Class 1

Topic 1: Intro to Jupyter Notebooks, the Spyder IDE and the course design examples. Core Python constructs.

Class 2

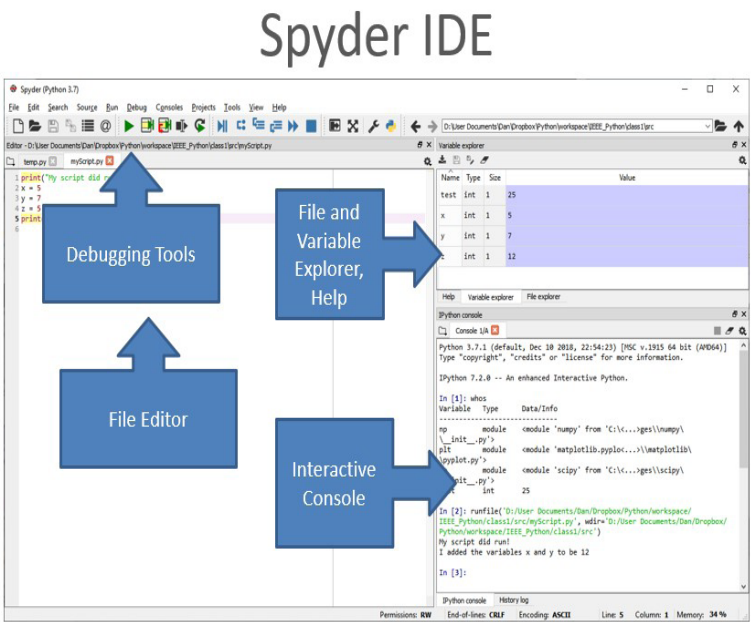
Topic 2: Core Python constructs; iterators, functions, reading writing data files.

Class 3

Topic 3: Signal processing simulation with popular packages including NumPy, SciPy, and Matplotlib.

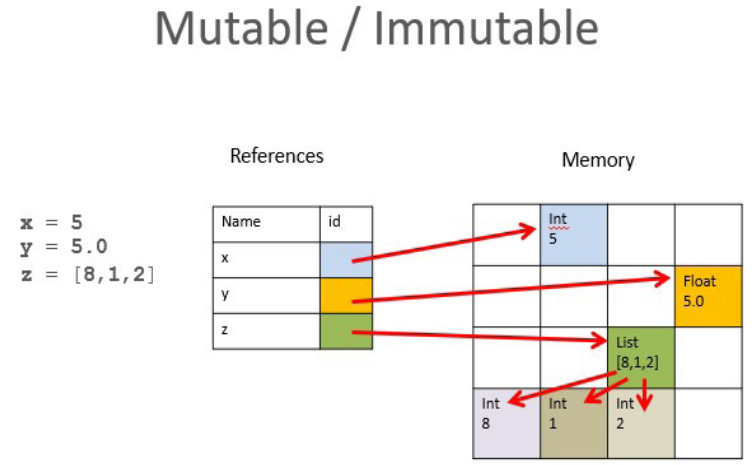
Class 4

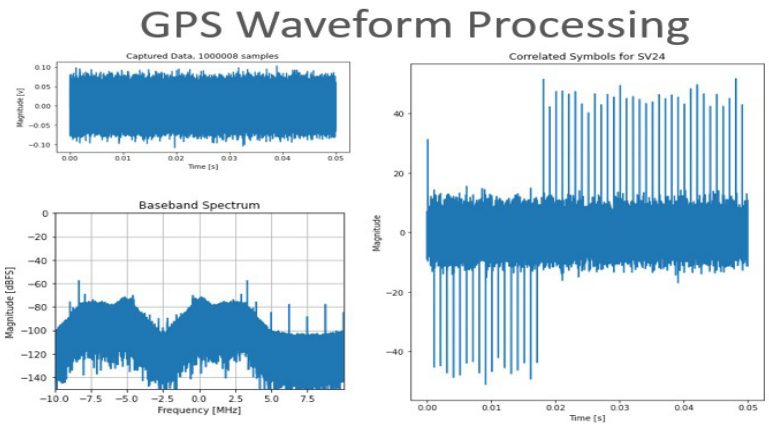
Topic 4: Bit/cycle accurate modelling and analysis using the design examples and simulation packages



Speaker's Bio: Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems and has taught courses on DSP to international audiences for over 15 years. Dan is a contributor to Signal Processing Stack Exchange https://dsp.stackexchange.com/, and is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page (https://www.linkedin.com/in/dan-boschen/)





Decision (Run/Cancel) Date for this Course is Monday August 19, 2024

Payment	on/by Aug. 10	After Aug. 10
IEEE Members	$190	$285
Non-members	$210	$315

https://ieeeboston.org/event/pythonapplications/?instance_id=3636

DSP for Wireless Communications

Dates & Times: **Live Workshops: 6:00 - 7:30 PM ET, Thursdays, Oct. 17, 24, 31 & Nov. 7 & 14, 2024**
First Video Release, October 10, 2024, (Orientation) 6:00 - 6:30 PM
Additional videos released weekly in advance of that week's live session

Speaker: **Dan Boschen**

Location: **Zoom Webinar**

New Format Combining Live Workshops with Pre-recorded Video - This is a hands-on course providing pre-recorded lectures that students can watch **on their own schedule** and an **unlimited number of times** prior to live Q&A/Workshop sessions with the instructor. Ten 1.5 hour videos released 2 per week while the course is in session will be available for up to two months after the conclusion of the course...until January 14, 2025.

Course Summary

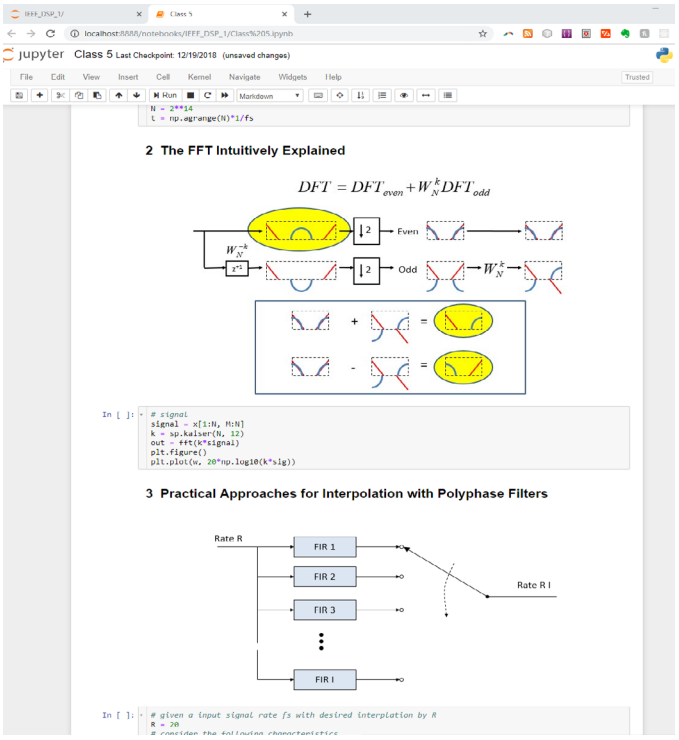
This course is a fresh view of the fundamental and practical concepts of digital signal processing applicable to the design of mixed signal design with A/D conversion, digital filters, operations with the FFT, and multi-rate signal processing. This course will build an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and applications in GPS and mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges in both the analog and digital domains, and not a tutorial on working with specific DSP processor hardware.

Now with Jupyter Notebooks!

This long-running IEEE Course has been updated to include Jupyter Notebooks which incorporates graphics together with Python simulation code to provide a "take-it-with-you" interactive user experience. No knowledge of Python is required but the notebooks will provide a basic framework for proceeding with further signal processing development using that tools for those that have interest in doing so.

This course will not be teaching Python, but using it for demonstration. A more detailed course on Python itself is covered in a separate IEEE Course "Python Applications for Digital Design and Signal Processing."

Students will be encouraged but not required to load all the Python tools needed, and all set-up information for installation will be provided prior to the start of class.



Target Audience:

All engineers involved in or interested in signal processing applications. Engineers with significant experience with DSP will also appreciate this opportunity for an in-depth review of the fundamental DSP concepts from a different perspective than that given in a traditional introductory DSP course.

Benefits of Attending/ Goals of Course:

Attendees will build a stronger intuitive understanding of the fundamental signal processing concepts involved with digital filtering and mixed signal analog and digital design. With this, attendees will be able to implement more creative and efficient signal processing architectures in both the analog and digital domains. The knowledge gained from this course will have immediate practical value for any work in the signal processing field.

Topics / Schedule:

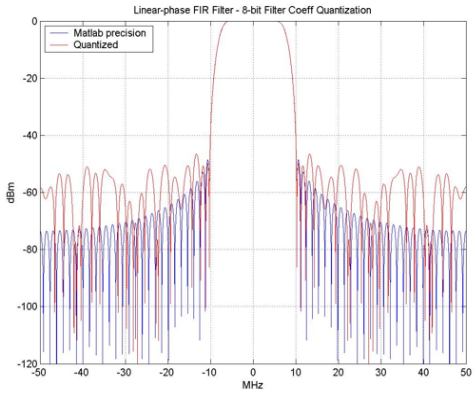
Class 1: Correlation, Fourier Transform, Laplace Transform
Class 2: Sampling and A/D Conversion, Z –transform, D/A Conversion
Class 3: IIR and FIR Digital filters, Direct Fourier Transform
Class 4: Windowing, Digital Filter Design, Fixed Point vs Floating Point
Class 5: Fast Fourier Transform, Multi-rate Signal Processing, Multi-rate Filters

Speaker's Bio:

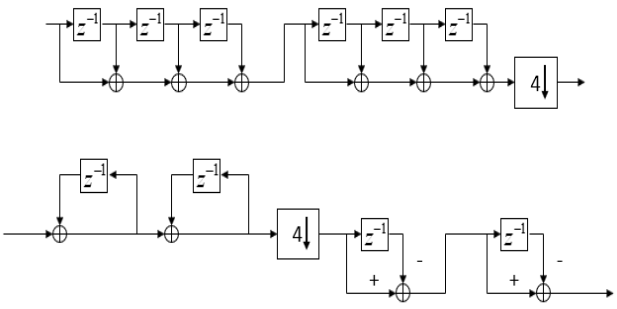
Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems. Dan is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page at: http://www.linkedin.com/in/dan-boschen

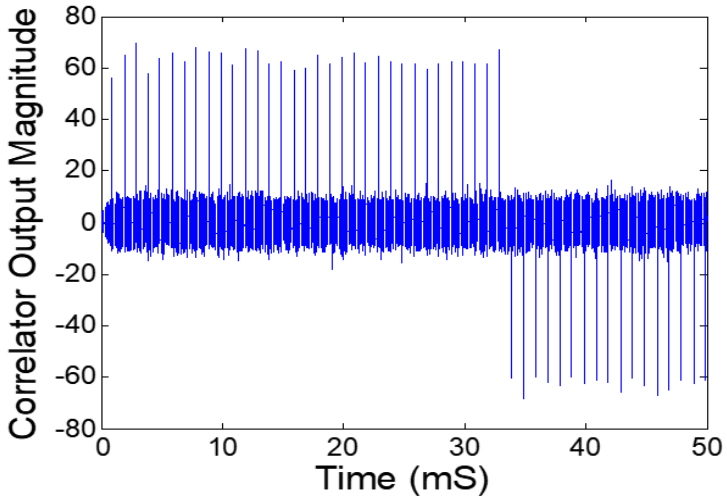
Linear Phase FIR Filter
(8-bit quantized filter coefficients)



Multi-stage CIC



Sliding Correlation



Decision (Run/Cancel) Date for this Course is Friday, October 4, 2024

Payment	on/by Oct. 1	After Oct. 1
IEEE Members	$190	$285
Non-members	$210	$315

https://ieeeboston.org/event/digital-signal-processing-for-wireless-communications/?instance_id=3620

Advanced Digital Design:
Implementing Deep Machine Learning on FPGA

Times & Dates: 6 - 7:30PM, Mondays, September 16, 23, 30, October 7
Speaker: Kendall Farnham, Dartmouth College

Location: MITRE Corporation, Bedford, MA
(This course will be offered in person and live online)

Hosted by

MITRE | SOLVING PROBLEMS FOR A SAFER WORLD®

Course Overview:
Field-programmable gate arrays (FPGAs) are versatile integrated circuits that offer a flexible and reconfigurable hardware platform for implementing custom digital circuits, particularly in applications requiring specialized architectures. Unlike application-specific integrated circuits (ASICs), FPGAs can be programmed and reprogrammed after manufacturing using hardware description languages (HDLs), enabling rapid prototyping and iterative design processes. FPGAs can be found in telecommunications, signal processing, aerospace, and other scenarios demanding high-performance computing, parallel processing, low-latency data processing, and real-time operations. The newest trends include integrating FPGAs with systems on chip (SoCs) for implementing low-latency machine learning (ML) and artificial intelligence.

This Advanced Digital Design course is an intensive program designed to build upon foundational concepts in digital logic design and equip students with the skills needed to implement robust high-speed ML algorithms on an FPGA. Through a combination of theoretical lectures, hands-on exercises, and practical projects, students will explore advanced FPGA topics encompassing architectural considerations, signal integrity, timing analysis, and optimization techniques to achieve reliable and efficient high-speed designs. Additionally, this course will encourage students to explore current research papers and real-world industry applications to foster a deeper appreciation for advancements in state-of-the-art FPGA design.

Target audience:
Students and professionals with a base knowledge of FPGA design looking to advance hardware design skills for developing complex customized circuits for efficient implementation of ML.

Benefits of attending:
- Valuable professional development creating skills that lead to job offers
- Reinforce and expand knowledge of VHDL and FPGA-specific design methodology.
- Develop skills for implementing high-speed, robust, reliable circuits on FPGAs.
- Gain understanding of real-world industry applications of FPGAs and SoCs.

Course Objectives:
By the end of this course, students will possess the expertise needed to tackle complex high-speed hardware design challenges using FPGAs. They will be well-prepared to contribute to cutting-edge research, industry projects, and advancements in areas such as telecommunications, data centers, embedded systems, and high-performance computing.

Prerequisites:
- Understanding of digital logic design principles and methodology (e.g., Boolean algebra, finite state machines, data path elements)
- Familiarity with VHDL programming (or Verilog)
- Experience with FPGA development boards and tools (e.g., Vivado)

Speaker Bio:
Kendall Farnham is a PhD candidate in Dr. Ryan Halter's bioimpedance lab at the Thayer School of Engineering, Dartmouth College. She has 10+ years of experience in the electrical and computer engineering (ECE) field and 5+ years of teaching and mentoring experience, having held several leadership positions within academia and industry. She received her bachelor's degree in ECE in 2014, worked in the defense industry as a software engineer for 4 years where she discovered her passion for research, and returned to

school to expand her education to include hardware design for space medicine applications. Specifically, she is interested in FPGA-based biomedical device design, currently working to develop space-compatible technologies that use impedance to monitor and detect physiological effects of space travel. Her expertise includes high-performance FPGA-based digital system design, analog circuit design, multi-modal imaging algorithms, and system integration.

Course Outline:

1. Review of Digital Logic Design and FPGA Programming
- Boolean algebra, combinational and sequential circuits, finite state machines
- FPGA, SoC, and SoM architectures and toolchains
- VHDL programming techniques and design methodology
- Writing effective testbenches, RTL simulation in Vivado
- Introduction to ML algorithms and FPGA-specific optimization strategies

2. High-throughput Communication on FPGAs
- Pipelining and parallelism for high-speed designs
- Synchronous vs. asynchronous communication protocols (SPI, SCI, UART, LVDS, I2C, PCIe, USB, Ethernet, etc.)
- Compare hardware/software/firmware implementations of ML: throughput speeds, resource utilization, and latency
- Methods used to achieve ultra-high sampling rates (>> system clock, GS/s range)
- Utilizing advanced IP cores and IO buffers for high-speed interfaces and data storage

3. Advanced FPGA Techniques for High-speed Systems
- Clock domain crossing verification and synchronization techniques
- Resource utilization, critical path identification, and optimization strategies
- Timing constraints, static and dynamic timing analysis
- Signal integrity analysis

4. High-Speed Design Verification and Testing
- Simulation-based verification techniques, advanced debugging, and waveform analysis
- Post-layout verification and back-annotation
- Test and validation strategies for high-speed designs
- Utilizing debug cores for real-time logic analysis

5. Machine Learning on FPGAs
- Algorithm validation and verification in software
- Compare capabilities and implementation strategies of ML on FPGAs, SoCs, and SoMs
- Optimization strategies for efficient ML implementation in hardware (e.g., convolution)

6. Digital Systems in Industry
- Techniques and best practices for scalable, reusable, reliable, and robust FPGA design
- Board-level considerations for high-speed signals: PCB layout guidelines, power distribution and decoupling, transmission line theory and termination techniques
- Emerging trends for FPGA-based digital signal processing (DSP) applications

CEU/PDH are are availabe upon request. A small fee may apply for the credits

Decision (Run/Cancel) Date for this Course is Monday, September 9, 2024

Payment	By Sept. 3	After Sept. 3
IEEE Members	$120	$140
Non-members	$250	$300

https://ieeeboston.org/event/advanced-digital-design/?instance_id=3481