

Boston Section

Supporting students, working engineers and retirees through professional development, education and resources.

THE *Reflector*

ISSUE #6
JUNE 2024

2024 IEEE INTERNATIONAL
SYMPOSIUM ON PHASED
ARRAY SYSTEMS AND
TECHNOLOGY

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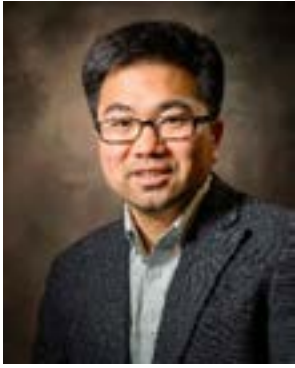


Boston Section

ieeeboston.org

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Celebrating Innovation at the IEEE VICS2024

by Rui Ma, Past Chair, IEEE Boston Section

On May 3rd, I had the distinct pleasure of attending the IEEE Vision Innovation Challenges Summit (VICS) held in our vibrant city. This event was a remarkable convergence of ingenuity, collaboration, networking, and celebration, highlighting the extraordinary contributions of the IEEE Medal Recipients 2024 to technological advancement and the world.

The summit, which coincided with IEEE's 140th anniversary, was a testament to the enduring legacy and forward-looking vision of IEEE. There are several panel sessions covering topics such as AI, Quantum, and Networking technologies. Insightful questions were asked, and opinions were debated on how we better navigate the future with the aid of cutting-edge technologies. As a proud sponsor, our Boston Section had an important role in enhancing the visibility of IEEE's mission and values here at VICS. We had a Boston Section booth and we sponsored the dessert reception and strengthened our commitment to support the local IEEE community including engineers and our student members.

One of the highlights of VICS was the recognition of medal winners whose pioneering work has significantly advanced technology. Their contributions are milestones that inspire future generations of engineers and innovators and had a huge impact on our lives. The gala dinner was a splendid affair, combining elegance with a spirit of celebration. It was a time to honor achievements, renew friendships, and make new connections. This celebratory evening was a fitting tribute to the remarkable journey of IEEE over the past 140 years.

Among the many impressive demonstrations at the summit, Boston Dynamics stood out with its cut-

ting-edge robotics. Their demos showcased the incredible strides being made in the field of robotics, offering a glimpse into a future where robots and humans work seamlessly together. The photo where the Spot- the agile mobile Robot stands in front of the IEEE Medal of Honor Wall is quite intriguing, reflecting both the past and the future. I like it very much!

The IEEE VICS was not just an event; it was a reaffirmation of our shared commitment to advancing technology for the benefit of humanity. It reinforced the importance of collaboration, learning, and continuous improvement. As we look to the future, events like VICS remind us of the collective potential we hold when we unite under the banner of IEEE.



For more details on the event, please visit the IEEE VICS 2024 Honors Ceremony and Gala. Here you may find more detailed info on the VICS program, and next year it will be held in Tokyo and I hope to see you there. <https://corporate-awards.ieee.org/event/2024-ieee-vic-summit-honors-ceremony-gala/> ing Innovation at the IEEE VICS2024

Letter to the Editor

Dear Dean Panetta:

I read with great interest your Boston IEEE Reflector posting “Who Wants to be an Engineer? As a past faculty member and a practicing engineer since 1961, I found your observations interesting about the loss of EEs in first circuits courses. The blunt fact is we need more electrical engineers and to lose otherwise capable students! To stem the loss engineering students in my opinion requires a deeper understanding of the culture surrounding today’s students as well as more efficient and effective teaching.

Remarkably, Tufts has a program to enhance faculty-student education initiatives and personal development skills but I didn’t see where it applies to the student population we are talking about. I don’t believe the old way of conveying the fundamentals of circuit theory (and other fundamental courses) work. Young faculty focus on their research because that’s what they are graded on and older established faculty perhaps having kept up the dramatic changes that culture has visited on young engineering students.

I agree completely with the students that circuit theory is a big challenge. They are being subjected to a change of thinking transitioning from passion-oriented teaching subjects and style to learning to thing numerically,

mathematically and systematically. It is not only a “new language” but an entirely new way of thinking. Thinking in a way most of their friends can’t and don’t want to relate to. This atmosphere is student-toxic when the instruction style takes no note of the students’ need to relate.

I have an idea, somewhat related to the Tufts Center for the Enhancement of Teaching and Learning. I propose developing a “Teaching Faculty” using retired senior or ex-faculty electrical engineers who could broaden the foundational courses with practical real-life examples, include simulation tools augmenting abstract theory and lab based or illustrative demonstrations of the basic principles. I see that there are so many aspects involved in the solution of this real life problem for both the profession and students.

Thank you for taking the time to discuss this important subject.

Sincerely,

Dr. Edward P. Sayre, P. E,
President and CTO
North East Systems Associates, Inc.

IEEE Boston Section Awards Call for Nominations

The IEEE Boston Section is seeking qualified candidates for its section awards.
The three section awards are

- **Distinguished Service Award**
- **Distinguished Member Award**
- **Student Achievement Award**

More information about the awards can be found here,
<https://ieeeboston.org/ieee-boston-section-awards/>
The deadline for nominations is August 1, 2024

IEEE Boston Section Social Media Links:

Twitter: <https://twitter.com/ieeeboston>

Facebook: <https://www.facebook.com/IEEEBoston>

YouTube: <https://www.youtube.com/user/IEEEBostonSection>

Instagram: <https://www.instagram.com/ieeeboston/>

LinkedIn: <https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about>

Consumer Technology Society Call for Volunteers!

We are currently looking for volunteers who would be interested in pushing forward the mission of the Consumer Technology (CT-S), Boston Chapter. The chapter is looking for volunteers to help organize chapter meetings and help meet the needs of the local CT-S member needs.

The Boston Section is organizing chapters into groups of similar technical interest areas to pool their resources for easier and better chapter collaboration in planning the chapter events.

If you have interest in volunteering for a chapter leadership position or are interested in learning more about what these volunteer positions may entail, please send an email to Karen Safina in the IEEE Boston Section office at, ieebostonsection@gmail.com

Aakash Deliwala, Chair, IEEE Boston Consumer Technology Chapter

Engineering in Medicine & Biology Society Call for Volunteers!

We are currently looking for volunteers who would be interested in pushing forward the mission of the Engineering in Medicine & Biology Society (EMBS), Boston Chapter. The EMBS - Boston Chapter was recently approved in July 2021, and we're looking to make a significant impact in the area of Biomedicine, Bioengineering, and Biotechnology in the region. The chapter is looking for volunteers to help organize chapter meetings and help meet the needs of the local EMBS members.

The Boston Section is organizing chapters into groups of similar technical interest areas to pool their resources for easier and better chapter collaboration in planning the chapter events.

If you have interest in volunteering for a chapter leadership position or are interested in learning more about what these volunteer positions may entail, please send an email to Karen Safina in the IEEE Boston Section office at, ieebostonsection@gmail.com.

Aseem Singh, Marie Tupaj, Co-Chairs, Boston EMBS Chapter



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KNOWLEDGE

COMMUNITY

PROFESSIONAL DEVELOPMENT

CAREER ADVANCEMENT

IEEE Boston Section Online Courses:

(Students have 180 day access to all online, self-paced courses)

Electronic Reliability Tutorial Series

Full course description and registration at ,
<http://ieeeboston.org/electronic-reliability/>

Introduction to Embedded Linux Part I

Full course description and registration at ,
<http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/>

Embedded Linux Optimization - Tools and Techniques

Full course description and registration at ,
<http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/>

Embedded Linux Board Support Packages and Device Drivers

Full course description and registration at ,
<http://ieeeboston.org/embedded-linux-bsps-device-drivers-line-course/>

Software Development for Medical Device Manufacturers

Full course description and registration at ,
<http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/>

Fundamental Mathematics Concepts Relating to Electromagnetics

Full course description and registration at ,
<http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/>

Reliability Engineering for the Business World

Full course description and registration at ,
<http://ieeeboston.org/reliability-engineering-business-world-line-course/>

Design Thinking for Today's Technical Work

<http://ieeeboston.org/design-thinking-technical-work-line-course/>

Fundamentals of Real-Time Operating Systems

<http://ieeeboston.org/fundamentals-of-real-time-operating-systems-rt201-on-line-course/>

NEW

Reliability Tutorial Series: Electronic Failure Mechanisms

https://ieeeboston.org/event/ieee-ansys-reliability-tutorial-series-electronic-reliability/?instance_id=3635

NEW

Reliability Tutorial Series – Accelerated Life Testing for Electronics Reliability

https://ieeeboston.org/event/ieee-ansys-reliability-tutorial-series/?instance_id=3634

ANNOUNCEMENT

2024 IEEE International Symposium on Phased Array Systems and Technology



15 - 18 October 2024

Hynes Convention Center, Boston, Massachusetts, USA

www.ieee-array.org


Platinum Sponsors



Gold Sponsors



Silver Sponsors



Technical Co-Sponsors



Media Sponsor



About the Symposium

Phased array systems continue to be a rapidly evolving technology with steady advances motivated by the challenges presented to modern military and commercial applications. This symposium will present the most recent advances in phased array technology and offer a unique opportunity for members of the international community to interact with colleagues in the field of phased array systems and technology.

The committee is thrilled to announce two major changes to the symposium to better reflect the interest and pace of technology development: (1) moving to the larger [Hynes Convention Center](http://www.hynesconventioncenter.com) in the Back-Bay neighborhood of Boston; and (2) increasing the symposium frequency to a two-year cadence.

Be a Symposium Sponsor or Exhibitor

For sponsorship and exhibit opportunities please reach out to Mark McClure and Marc Angelucci at: sponsorships@ieee-array.org.

Session Topics

- 5G Arrays
- Array Design
- Array Measurements
- Array Signal Processing
- Automotive Arrays
- Beamforming & Calibration
- Digital Array Architectures
- Dual Polarized Arrays
- Low-Cost Commercial Arrays
- MIMO Arrays
- Medical Applications
- Metamaterial Phased Arrays
- mmWave and Terahertz
- T/R Modules
- SATCOM Arrays

Special Sessions

- European Phased Arrays
 - *Michael Brandfass & Alfonso Farina*
- Commercial Satellite Arrays
 - *Gabriel Rebeiz & Will Moulder*
- Wideband Arrays
 - *Justin Kasemodel & John Volakis*
- Low Frequency Arrays
 - *Cecelia Franzini & Eric Robinson*
- Weather Arrays
 - *Caleb Fulton & Matt Harger*
- EurAAP Lens-Array Combination
 - *Stefania Monni & Oscar Quevedo*
- 3D Printing Techniques for Phased Arrays
 - *Esteban Menargues & Maria Garcia-Vigueras*

Committee

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Wajih Elsallal (VC), MITRE

Technical Program Chairs

David Mooradd (C), MIT LL
Glenn Hopkins (VC), GTRI

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William Weedon, Applied Radar

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Justin Kasemodel, Raytheon

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Frank Vliet, TNO

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Mark Fosberry, MITRE
Shireen Warnock, MIT LL

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Jack Logan, NRL
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Honglei Chen, MathWorks

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Daniel Culkin, NGC
Alan J. Fenn, MIT LL
Jeffery S. Herd, MIT LL
Bradley Perry, MIT LL

Arrangements/ Administration

Robert Alongi, IEEE Boston
Kathleen Ballos, Ballos Assoc.

IEEE Video Series

A collaborative discussion panel featuring esteemed members from the Institute of Electrical and Electronics Engineers has convened in 2021 to produce educational video presentations that embrace IEEE's mission of advancing technology for humanity.

Among the programs they've produced include "Electric Vehicles: Fun Saving Our Planet", "Greener Power For More Electric Vehicles", "Overcoming Nuclear Fears To Achieve Net Zero CO2 By 2050" and "Achieving a Net Zero Carbon Future", "Green Energy's Economic Progress", and "Net-Zero CO2 with Nuclear, Hydrogen and Geothermal". Projects currently in production include the expansive topic of futurology, with a focus on increasing the efficiency and transformation of aging electrical power generating stations and infrastructure to accommodate nuclear power; reviewing the viability of alternative energy (such as geothermal, wind and solar); and focusing on 'cleaner' fossil fuels that are more environmentally-friendly to slow the rate of climate change.

These shows are produced and directed by Lennart E. Long, IEEE Senior Life Member from the Executive Committee and Past Chair of the Boston Section; Dr. Paul H Carr, BS, MS, MIT; PhD Brandeis U, IEEE Life Fellow; Dr. Ted Kochanski, SB (MIT), Ph.D (U.Texas, Austin), IEEE Global Education for Microelectronic Systems and former Boston Section Chair; and Dr. Ken Laker, B.E. (Manhattan College), M.S. and Ph.D. (New York University), IEEE Life Fellow and past President of IEEE.

The panel is moderated by five-time Boston/New England Emmy Award-winner and television personality and star of "The Folklorist," John Horrigan. These video programs with presentations and discussions can be accessed at the IEEE Boston Section video portal at <https://vimeo.com/user18608275>.

We are looking for any IEEE members that would like to appear on the program in the role of presenter or discussion expert. Simply reach out to Robert Alongi at the Boston Section at, ieebostonsection@gmail.com.

Call for Articles

Now that the Reflector is all electronic, we are expanding the content of the publication. One of the new features we will be adding are technical, professional development, and general interest articles to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development or general interest articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required.

A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional/interest articles will be reviewed by the Publications Committee for suitability. The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to;
ieebostonsection@gmail.com

IEEE Boston Section Volunteers Wanted!

Are you passionate about technology and eager to contribute to the advancement of your field? The IEEE Boston Section is excited to announce a call for volunteers to join our dynamic team of professionals and enthusiasts. By becoming a volunteer, you'll have the opportunity to collaborate with like-minded individuals, develop new skills, and make a meaningful impact on the local technology community.

About IEEE Boston Section:

The IEEE Boston Section is a thriving community of engineers, researchers, students, and industry professionals dedicated to promoting technological innovation and knowledge sharing. Our section hosts a variety of events, workshops, seminars, and conferences throughout the year, providing members with opportunities to learn, network, and stay updated on the latest developments in their fields.

Volunteer Opportunities:

We are currently seeking volunteers to help on the following committees:

The Fellow and Awards Committee - activities include recommending qualified members of the Section for advancement to Fellow grade and for receipt of the various IEEE (IEEE/Region/MGA/Section) awards. Identifying and building a database of the various IEEE awards available for nomination and searching out qualified candidates, for preparing the necessary written recommendations, and for assembling all required supporting documentation and submit its recommendations directly to the appropriate IEEE body.

Time Commitment: Meets 4 times a year for 1 – 2 hours per meeting (virtual or in person)

Local Conferences Committee - activities include identifying timely topical areas for conference development. Identify champions of these conferences to run the identified conference organizing committees. The section local conference committee is not charged with organizing and executing individual conferences.

Time Commitment: Meets 4 times per year 1 – 2 hours per meeting (virtual or in person)

Professional Development & Education Committee - activities include identifying topics, speakers, and/or organizers for appropriate technical lecture series or seminars. The subject matter should be timely, of interest to a large segment of the membership, and well organized with regard to speakers and written subject matter.

Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

The Membership Development Committee - activities include actively promoting membership in the IEEE and shall encourage members to advance to the highest grade of membership for which they are qualified. To these ends this committee shall include wide representation within the Section territory, shall maintain lists of

prospects and members qualified for advancement, and shall provide information and assistance to preparing applications.

Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Student Activities Committee - activities include attracting a broad and diverse group of undergraduate and graduate students to IEEE and to engage them in activities that promote their own professional development as well as the ongoing growth of IEEE. The Student Activities Committee shall include among its members the IEEE Counselors at the universities, colleges, and technical institutes that lie within the Section territory. It shall be responsible for liaison with the Student Branches at these institutions and advise the Executive Committee on all other matters affecting the Student Members of the Section.

Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Young Professionals Affinity Group - activities include organizing programs, and initiatives aimed to address the needs of early-career professionals pursuing technology-related careers in engineering, business, management, marketing, and law. This committee is committed to helping young professionals evaluate their career goals, polish their professional image, and create the building blocks of a lifelong and diverse professional network.

Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Benefits of Volunteering:

Volunteering with IEEE Boston Section offers numerous benefits, including:

- Networking opportunities with professionals in your field.
- Skill development and enhancement through hands-on experience.
- Contribution to the local technology community and its growth.
- Access to cutting-edge information and discussions.

How to Get Involved:

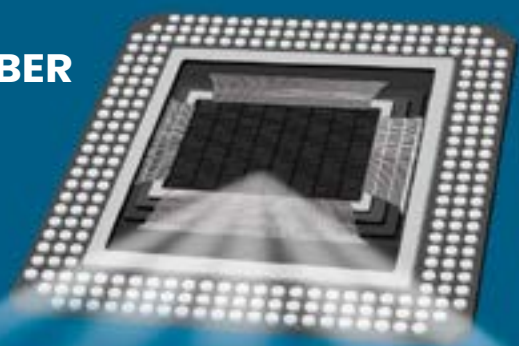
If you're enthusiastic about technology and want to make a difference, we invite you to join us as a volunteer. To express your interest and learn more about specific roles, please visit our website and fill out the volunteer application form. Our team will get in touch with you to discuss opportunities that align with your interests and skills.

Thank you for considering this opportunity to contribute to the IEEE Boston Section. Your dedication and passion are what drive the success of our community and its impact on the world of technology.

Volunteer Here!

<https://ieeeboston.org/volunteer/>

**23 – 27
SEPTEMBER
2024**



IEEE HPEC
High Performance Extreme Computing

HPEC is the largest computing conference in New England and is the premier conference in the world on the convergence of High Performance and Embedded Computing.

The technical committee seeks new submissions that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- High Performance Computing
- AI / Machine Learning
- Performance Engineering for AI
- AI for Performance Engineering
- AI at Scale and AI on the Edge
- LLMs, CNNs, DNNs, other AI/ML Methods
- Low/Mixed Precision Approaches
- Big Data and Distributed Computing
- Data Intensive Computing
- High Performance Data Analysis
- General Purpose GPU Computing
- Cyber Analysis and Secure Computing
- Interactive and Real-Time Supercomputing
- Supercomputing
- Graph Analytics and Network Science
- ASIC and FPGA Advances
- Advanced Multicore Software Technologies
- Advanced Processor Architectures
- Automated Design Tools
- Case Studies and Benchmarking of Applications
- Mapping and Scheduling of Parallel and Real-Time Applications
- Quantum and Non-Deterministic Computing
- New Application Frontiers
- Computing Technologies for Challenging Form Factors
- High Performance Embedded Computing
- Fault-Tolerant Computing

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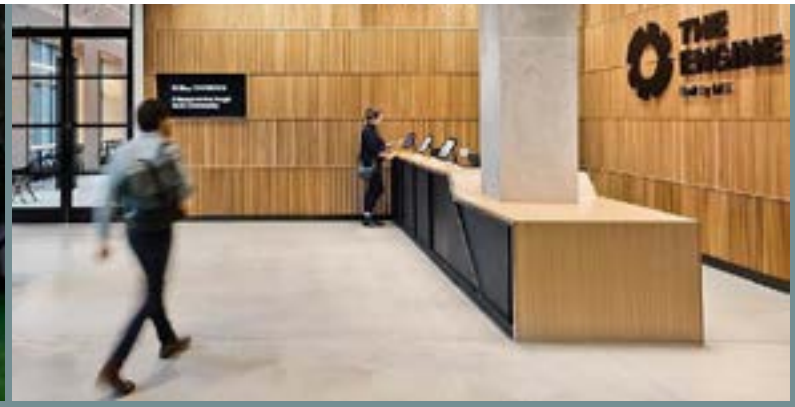
Mr. Robert Alongi / IEEE Boston Section

Submission Deadline:

07 July 2024

Submission Guidelines:

<https://iee-hpec.org/index.php/submit/>



IEEE SiPS 2024

IEEE Workshop on Signal Processing Systems

4–6 November 2024

Cambridge, Massachusetts, U.S.A.

The 37th IEEE Workshop on Signal Processing Systems (SiPS) is a premier international forum in the area of design and implementation of signal processing systems. It addresses all aspects of architecture and design methods of these systems. Emphasis is on current and future challenges in research and development in both academia and industry.

Submitting a Paper

We invite prospective authors to submit original papers (up to 6 pages) in areas including, but not limited to:

Software Implementation of Signal Processing Systems

- Software on programmable digital signal processors
- Application-specific instruction-set processor (ASIP) architectures and systems
- SIMD, VLIW, and multi-core CPU architectures
- GPU-based massively parallel implementations

Hardware Implementation of Signal Processing Systems

- Low-power signal processing circuits and applications
- High-performance VLSI systems
- FPGA and reconfigurable architecture-based systems
- System-on-chip and network-on-chip
- VLSI for sensor network and RF identification systems
- Quantum signal processing
- Processing-in-memory signal processing systems

Design Methods of Signal Processing Systems

- Optimization of signal processing algorithms
- Compilers and tools for signal processing systems
- Algorithm-to-architecture transformation
- Dataflow-based design methodologies
- Error-tolerant techniques for signal processing

Machine Learning for Signal Processing

- Circuits and systems for AI
- Deep learning/machine learning/AI algorithms
- Tools/platforms for AI
- Transfer learning
- Distributed/federated learning
- Hardware/neuromorphic accelerators
- Hardware/software co-design and automation for AI

Signal Processing Application Systems

- Audio, speech, and language processing
- Biomedical signal processing and bioinformatics
- Image, video, and multimedia signal processing
- Information forensics, security, and cryptography
- Sensing and sensor signal processing
- Signal processing for non-volatile memory systems
- Latency-and power-constrained signal processing
- Wireless communications and MIMO systems
- Coding and compression
- Signal processing for mixed-signal technologies

Important Dates

Technical Papers:	03 April 2024
Paper Notifications:	26 June 2024
Special Session Proposals:	31 July 2024
Tutorial Proposals:	31 July 2024

Committee

General Chairs

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Program Chairs

Jari Nurmi, Tampere Univ.
Jani Boutellier, Univ. of Vaasa

Local Organizing Chair

Brian Telfer, MIT Lincoln Laboratory

eee-sips.org



IEEE RFID 2024 - SUBMIT NOW!

The 18th IEEE International Conference on RFID (IEEE RFID 2024) is seeking high-quality submissions for papers and posters (see submission options below) in all areas of technical RFID research and application.

IEEE RFID 2024 offers a unique opportunity to share, discuss, and witness research results in all areas of RFID technologies and their applications.

COME JOIN US IN BOSTON, JUNE 4–6, 2024!



Date: June 4-6, 2024



MIT Media Lab, Cambridge MA



IMPORTANT DATES

PAPER SUBMISSION DEADLINE:
FEBRUARY 26TH, 2024

WORKSHOP PROPOSAL DEADLINE:
MARCH 11TH, 2024

NOTIFICATION OF ACCEPTANCE:
APRIL 22ND, 2024

POSTER SUBMISSION:
APRIL 29TH, 2024

FINAL PAPER SUBMISSION:
MAY 13TH, 2024

ALL DEADLINES ARE AT
11:59PM UTC-12

CALL FOR PAPERS

The IEEE RFID 2024 accepts paper and poster submissions formatted in the IEEE conference style. Manuscripts should be 6 pages, submitted by the advertised conference deadline (Feb 26, 2024). Posters follow the 1-page format (deadline April 29, 2024)

Selected papers will be invited to be published in Journal of Radio Frequency Identification (JRFID)

General Track Topics and Workshops

GENERAL TRACK TOPICS

ANTENNAS & PROPAGATIONS
APPLICATIONS & SOFTWARE
PROTOCOLS & SECURITY
CIRCUITS, DEVICES & INTERROGATIONS
NEXT-GEN RFID & ID+
SENSORS
MOTION CAPTURE (MOCAP)

GENERAL TRACK TOPICS

ENERGY HARVESTING
ARTIFICIAL INTELLIGENCE (AI) FOR RFID
DIGITAL TWINS
OCEAN INTERNET OF THINGS (IOT)
BIOMEDICAL SYSTEMS
SMART MATERIALS
GEN. 3 RFID



Visit the website:



Guest Article

The U.S. Patent Office Continues to Clarify that Patent Inventorship Requires Conception, Despite Broader Language Used by Courts

By Craig R. Smith

Inventors capture our imagination by making dreams possible. Famous inventors, such as Thomas Edison and Alexander Graham Bell, not only advance the state of technology but create whole new industries based on their ideas. Conception of an invention is the key to being considered an inventor. The U.S. Patent Office has consistently emphasized that you must contribute to the conception of the invention to be deemed an inventor. Unfortunately, courts have explained the requirements for inventorship in broader terms, creating some confusion over who is entitled to be an inventor on a patent. Courts should clarify the requirements for inventorship to ensure that conception remains the touchstone for being an inventor.

When applying for a patent on an invention, the U.S. Patent Office provides specific guidance on who can be considered an inventor.

The definition for inventorship can be simply stated: “The threshold question in determining inventorship is who conceived the invention. Unless a person contributes to the conception of the invention, he is not an inventor. ... Insofar as defining an inventor is concerned, reduction to practice, per se, is irrelevant. One must contribute to the conception to be an inventor.” *In re Hardee*, 223 USPQ 1122, 1123 (Comm’r Pat. 1984). Manual of Patent Examining Procedure (“MPEP”) 2109.

Conception of the invention is key to inventorship. Courts have explained that “[c]onception is the ‘formation in the mind of the inventor, of a definite and permanent idea of the complete and operative invention, as it is hereafter to be applied in practice.’” *Ethicon, Inc. v. U.S. Surgical Corp.*, 135 F.3d 1456, 1460 (Fed. Cir. 1998) (quoting *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1376, 231 USPQ 81, 87 (Fed.Cir.1986)). Once an invention has been conceived, however, the steps required to reduce it to practice do not make someone an inventor.

The Patent Office and courts should define inventorship

in the same way, but they do not always do so. For example, the Federal Circuit has repeatedly used broader language to describe the requirements for inventorship, creating confusion among patent practitioners and tech companies. In the *Pannu* case, the Federal Circuit set forth the requirements for being considered a joint inventor:

All that is required of a joint inventor is that he or she (1) contribute in some significant manner to the conception or reduction to practice of the invention, (2) make a contribution to the claimed invention that is not insignificant in quality, when that contribution is measured against the dimension of the full invention, and (3) do more than merely explain to the real inventors well-known concepts and/or the current state of the art.

Pannu v. Iolab Corp., 155 F.3d 1344, 1351 (Fed. Cir. 1998). The court’s requirements broaden the definition of an inventor to a person who contributes to either the conception or reduction to practice of the invention. In other words, conception alone is not required to be considered an inventor. If applied as written, the court’s statement would create a new standard, allowing an inventor to contribute only to the reduction to practice of the invention. This broader standard would conflict with the court’s own precedent on inventorship and the Patent Office’s guidance.

The *Pannu* court cited two cases in support of its inventorship requirements: *Fina Oil and Ethicon. Fina Oil & Chem. Co. v. Ewen*, 123 F.3d 1466, 1473 (Fed.Cir.1997) and *Ethicon, Inc. v. United States Surgical Corp.*, 135 F.3d 1456, 1460 (Fed.Cir.1998). Neither one of these cases supports the proposition that “reduction to practice” alone is sufficient to be considered an inventor.

In *Fina*, the Federal Circuit confirmed that “[c]onception is the touchstone to determining inventorship.” *Fina*, 123 F.3d at 1473. Likewise in *Ethicon*, the court held that conception is the key issue and “one does not qualify as a joint inventor by merely assisting the actual inventor

after conception of the claimed invention.” *Ethicon*, 135 F.3d at 1460. Thus, reducing the invention to practice does not make a person an inventor: “one of ordinary skill in the art who simply reduced the inventor’s idea to practice is not necessarily a joint inventor.” *Id.*

Nevertheless, after *Pannu*, the Federal Circuit and district courts have continued to cite the same *Pannu* factors for determining inventorship. For example, last year the Federal Circuit again repeated the *Pannu* factors that “a joint inventor must contribute in a significant manner to the conception or reduction to practice of the invention, make a contribution to the invention that is not insignificant, and do more than explain well known concepts or the current state of the art.” *HIP, Inc. v. Hormel Foods Corp.*, 66 F.4th 1346, 1353 (Fed. Cir. 2023); see also *Plastipak Packaging, Inc. v. Premium Waters, Inc.*, 55 F.4th 1332, 1340 (Fed. Cir. 2022); *In re VerHoef*, 888 F.3d 1362, 1366 (Fed. Cir. 2018); *Audionics Sys., Inc. v. AAMP of Fla., Inc.*, No. CV1210763MMM/JEMX, 2015 WL 12712288, at *47 (C.D. Cal. July 10, 2015); *Illinois Tool Works, Inc. v. MOC Prod. Co.*, 856 F. Supp. 2d 1156, 1185 (S.D. Cal. 2012).

The Patent Office has taken note of the court’s broader language and explained that the Patent Office’s test for inventorship has not changed. A recent Patent Office paper on inventorship took pains to clarify why the Federal Circuit’s *Pannu* factors do not change its requirement for conception of the invention:

While these [*Pannu*] factors do refer to reduction to practice, applicants are reminded that the main inquiry is who conceived of the invention. Reduction to practice, per se, is generally irrelevant to this inquiry. *MPEP* 2109(II) (citing *Fiers v. Revel*, 984 F.2d 1164, 1168 (Fed. Cir. 1993)). The mention of reduction to practice in the *Pannu* factors is an acknowledgement of the simultaneous conception and reduction to practice doctrine used in unpredictable technologies. See, e.g., *Amgen, Inc. v. Chugai Pharm. Co.*, 927 F.2d 1200, 1206 (Fed. Cir. 1991). The *Pannu* factors are not a basis to conclude that reduction to practice, alone, is sufficient to demonstrate inventorship.

Patent & Trademark Office: “Inventorship Guidance for AI-assisted Inventions,” page 13, footnote 32. <https://www.federalregister.gov/documents/2024/02/13/2024-02623/inventorship-guidance-for-ai-assisted-inventions>. The Patent Office’s guidance makes plain that conception alone remains the critical issue for inventorship. Reduction to practice is generally irrelevant and cannot, on its own, be sufficient to show inventorship.

The court’s confusing inventorship language may be the

result of unique cases where conception of the invention required reduction to practice. “In some instances, an inventor is unable to establish a conception until he has reduced the invention to practice through a successful experiment. This situation results in a simultaneous conception and reduction to practice.” *Amgen, Inc. v. Chugai Pharm. Co.*, 927 F.2d 1200, 1206 (Fed. Cir. 1991).

Simultaneous conception and reduction to practice may occur in unpredictable scientific fields, such as biotechnology. For instance, the conception of a specific DNA sequence may not occur until it has been reduced to practice. “We hold that when an inventor is unable to envision the detailed constitution of a gene so as to distinguish it from other materials, as well as a method for obtaining it, conception has not been achieved until reduction to practice has occurred, i.e., until after the gene has been isolated.” *Amgen*, 927 F.2d at 1206; see also *Fiers v. Revel*, 984 F.2d 1164, 1169 (Fed. Cir. 1993).

The holdings in *Amgen* and similar cases do not support the broader definition of an inventor set forth in *Pannu*. *Amgen* recognizes that the conception of some inventions requires reduction to practice. In other words, “conception is not complete if the subsequent course of experimentation, especially experimental failures, reveals uncertainty that so undermines the specificity of the inventor’s idea that it is not yet a definite and permanent reflection of the complete invention as it will be used in practice.” *Burroughs Wellcome Co. v. Barr Lab’ys, Inc.*, 40 F.3d 1223, 1229 (Fed. Cir. 1994). In these unique cases, conception of the invention was not complete until reduction to practice occurred.

Cases involving simultaneous conception and reduction to practice do not change the requirement that inventorship is based on conception. Once an invention has been conceived, reduction to practice is irrelevant to inventorship. In short, reduction to practice alone is insufficient to satisfy the requirement for inventorship.

Moving forward, courts should be more precise in describing the requirements for inventorship. The first requirement for inventorship under the *Pannu* test should read: “All that is required of a joint inventor is that he or she (1) contribute in some significant manner to the conception of the invention, ...” This language is consistent with the court’s prior precedent and the Patent Office’s guidance on inventorship.

Craig Smith is a partner at intellectual property law firm, Lando & Anastasi, LLP. He can be reached at csmith@lalaw.com or 617-395-7081.

Entrepreneurs' Network – 6:00PM, Tuesday, June 4

Exits

As a dedicated entrepreneur, who has poured heart and soul into your startup to launch and scale the business for success, have you taken the time to plan for a potential exit?

Having an exit strategy is an important part of your startup's overall business strategy to provide a vision of how you can capitalize on your investment. Decisions you make today about the structure and operation of the business can have huge implications down the road for your exit. Investors will want to see that you have thought about potential exits.

Learn about the prep work needed for successful exits from startup experts, including exit strategy planning, and learn perspectives from serial entrepreneurs, financial advisors, and M&A professionals, in both the high technology and life science fields. After the presentation, you will have an opportunity to ask questions to the panelists, then network with the experts and other attendees during the last half hour of the event.

Attendees will have the option to join us in-person at Lasell University in Newton, MA or online via Zoom.

The meeting description will be posted soon!

Registration will be opened soon!
<https://bostonenet.org/events/exits/>

A question-and-answer session will follow the panel discussion, and the panelists will be available afterward for responses to individual questions.

(All times are USA Eastern time, webinars will not be recorded, except that ENET members can review a recording of this webinar after the meeting.)

This is a hybrid event. You may choose to participate in-person or online.

In-person Participation (check-in begins at 6:00 PM)
LOCATION: Lasell University, Newton MA

PARKING: Parking is available.

REFRESHMENTS: Pizza and soft drinks will be served.

Online Participation: Zoom links will be sent to all registrants after registration.

Cost and Reservations: This event is free for ENET members and \$15 for non-members. Click [here](#) to learn how to become a member. To expedite sign-in for the event, we ask that everyone — members as well as non-members — pre-register. If you cannot pre-register, you are welcome to register in person at the door while seats are available.

Event Schedule

6:00 pm ET: Registration - On-Site Check-in and Networking

7:00 pm ET: Introduction - ENET Chairperson's announcements

7:10 pm ET: eMinute Pitch - up to 3 startups give a 90-second elevator pitch

7:25 pm ET: Expert Panel - expert speakers on the night's topic

8:15 pm ET: Q & A - Moderator and Audience Q & A with the speakers

8:30 pm ET: Networking - Final Networking, including the night's speakers

Double check your email address – if it is incorrect, you will not get the email confirmation and the Zoom link.

REFUND POLICY: If you cancel your registration before the event, ENET will refund your registration fee in the form of a credit towards a future ENET event.

Antennas & Propagation – 12:00PM, Wednesday, June 12

Electronically Reconfigurable Filtennas for S-Band And X-Band Operation



Next-generation wireless RF systems are expected to contain multi-functional, highly flexible, and tightly integrated front-ends for achieving agile use of the frequency spectrum. In the past decade, this has led to research on filtering antennas, or filtennas, in which

the functionality of the antenna and filter is combined into a single highly integrated module that achieves the function of both components with a higher-order transfer function. These filtennas can have improved performance, size, and cost. Furthermore, by incorporating frequency-agility, a filtenna can provide adaptation to changing radio environments. One of the challenges in realizing a reconfigurable filtenna is that two dissimilar elements need to be tuned in tandem.

This presentation covers recent developments in the design of reconfigurable filtennas in the S-band (2-4 GHz) and X-band (8-12 GHz). The filtennas are based on using evanescent-mode cavities as the backing for slot antennas. A discussion of available tuning mechanisms and the challenges of going from S-band to X-band is included. Second-order reconfigurable filtenna proof-of-concept prototypes are shown in both frequency bands. The prototype filtennas are created using commercially available printed circuit board materials and tuning elements and measured in an anechoic chamber. The S-band filtenna can continuously tune from 2 to 2.6 GHz while achieving a realized gain between 2.7 to 5.2 dB, respectively. The X-band filtenna demonstrates tuning from 9.6 to 11.1 GHz, with a maximum gain of 5 dB. Overall, with the demonstrated performance, these elements are promising components for future wireless communications and radar systems.

Jessica E. Ruyle (M'05--SM'16) was born in Shawnee, OK USA in 1984. She received a B.S. degree in electrical engineering from Texas A&M University, College Station in 2006 and an M.S and Ph.D. degree in electrical engineering from the University of Illinois at Urbana-Champaign in 2008 and 2011 respectively.

From 2006 to 2011, she was a Graduate Research Assistant at the University of Illinois at Urbana-Champaign. From 2012 to 2019, she was an Assistant Professor with the School of Electrical and Computer Engineering, University of Oklahoma, Norman. In 2019 she was promoted to Associate Professor in Electrical and Computer Engineering at the University of Oklahoma. She is an Advanced Radar Research Center (ARRC) member at the University of Oklahoma (OU). She holds two patents for her antenna designs. Her research interests are in the development and characterization of new electromagnetic devices and platforms such as antennas and packaging to improve the performance of radiating systems in challenging environments.

Prof. Ruyle is a member of Tau Beta Pi and Eta Kappa Nu. She is the recipient of a DARPA Young Faculty Award for her work in highly conformal, placement insensitive antennas and was named a William H. Barlow Presidential Professor at OU. She is also an IEEE Senior Member and an Associate Editor for IEEE Antennas and Wireless Propagation Letters.

Zoom link will be sent to registrants before the event.

Registration:

<https://events.vtools.ieee.org/m/418644>

Boston/Providence/New Hampshire Reliability Society – 5:30PM, Wednesday, June 12

Perfect Accelerated Life Testing

Measuring the Reliability of new technology is critical for any development team. Accelerated Life Testing (ALT) measures a new product's life by testing at elevated stresses. It saves valuable time & resources; giving teams the right information rapidly. Join this webinar to get an overview of ALT and a few tips and tricks to ensure you avoid common pitfalls.



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Agenda:

5:30 PM Pizza, salad, soft drinks, and Networking
 6:00 PM Technical Presentation
 6:45 PM Questions and Answers
 7:00 PM Adjournment

Adam Bahret is the founder of Apex Ridge Consulting and a leading reliability expert who writes, speaks and coaches engineering teams on reliability as a competitive edge. His reliability strategy has delivered millions in savings for clients while mitigating risk and forming a foundation for reliability-fueled growth and brand dominance. His clients range across multiple industry segments, including medical devices, robotics, semiconductor, aerospace, consumer, and automotive.

Adam works with technical teams to improve the design while mentoring leadership teams in adopting the processes, language, and behaviors to build a reliability culture. He also introduces key reliability metrics such as "time-to-reliability" that guide organizational thinking and build a robust reliability culture that's the

hallmark of dominant top-performing technology companies.

Adam is the author of three books on reliability engineering: *Devastate the Competition*, *How to Take Market Share Through Robust Design* (2023), *Reliability Culture*, *How Leaders Build Organizations that Create Reliable Products* (Wiley 2021), and *How Reliable is Your Product*, *50 Ways to Improve Product Reliability* (2nd Ed 2016). Adam has also released a series of small handbooks on specific reliability tools called "Adam's The Perfect Reliability Tool" book series. "The Perfect HALT", "The Perfect Accelerated Life Test", "The Perfect Reliability Growth Test", and "The Perfect DFMEA."

Adam has deep technical expertise and over 25 years of experience in product development and reliability engineering. He has an MS in Mechanical Engineering from Northeastern University, is an ASQ nationally certified reliability engineer, and an international speaker on technology, leadership, and product development. More information on Adam and Apex Ridge can be found at www.adambahret.com.

The meeting is open to all. You do not need to belong to the IEEE to attend this event; however, we welcome your consideration of IEEE membership as a career enhancing technical affiliation.

There is no cost to register or attend, but registration is required (so that we may purchase enough food!)

Location: In Person and Virtual Event. ASMPT NEXX, 900 Middlesex Turnpike, Billerica, MA. Building 6

FREE In Person and Virtual Event

Registration:

<https://events.vtools.ieee.org/m/415811>

Consultants' Network – 12:00PM, Monday, June 17

CNET Meeting: Board of Directors (members only)



Location: Raagini Indian Bistro, 209 N Main Street, Andover

Free lunch starts at 12:00 PM

Meeting starts at 1:00 PM - On-site and Zoom

David Connor

An IEEE Member for more than 42 years, David is the founder and president of Striper Solutions LLC.

He brings many years of successful experience in engineering consulting for product development and regulatory compliance.

Members in good standing are encouraged to attend. If you are unable to attend, then we will also be on Zoom.

Your registration confirmation email contains the Zoom details.

Join us!

<https://bostonconsultants.org>

Registration:

<https://bostonconsultants.org/event-5740097>

Call for Articles

Now that the Reflector is all electronic, we are expanding the content of the publication. One of the new features we will be adding are technical, professional development, and general interest articles to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development or general interest articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or pay-

ment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional/interest articles will be reviewed by the Publications Committee for suitability. The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to;
ieeebostonsection@gmail.com

Power & Energy Society – 6:00PM, Tuesday, June 18

Real-Time Synchrophasor-Based Situational Awareness, Analysis, Monitoring, and Control of Transmission and Distribution Systems



As the electric grid undergoes significant transformations and becomes increasingly affected by more frequent and severe weather events, the resilience and reliability of transmission and distribution systems become extremely important. The advancement of Energy Management Systems (EMS) is crucial for maintaining the reliable operation of power systems. A Phasor Measurement Unit (PMU)-based framework enhances state estimation accuracy, thereby improving the effectiveness of modern EMS applications, such as security assessments. By leveraging synchronized measurements, this framework enhances the reliability and efficiency of EMS, optimizing system operation and performance. The changing energy generation mix, the growth of DERs, and the integration of renewable energy resources at both large scale and individual user level necessitate stronger grid resilience and greater consumer choice.

To meet these evolving requirements, enhanced real-time visibility and control of bidirectional energy flows across the distribution grid are essential. The deployment of advanced technologies, such as the Distribution Linear State Estimator (DLSE), is key to addressing these challenges. This presentation will discuss the critical roles of PMU-based EMS and network analysis applications, and DLSE in enhancing the situational awareness, analysis, monitoring, and control of modern transmission and distribution systems, ensuring their resilient and reliable operation.

Marianna Vaiman is the Co-founder and CEO of V&R Energy. She has over 30 years of experience in the de-

velopment and deployment of innovative technologies for the electric utility industry. She has B.Sc. and M.Sc. in Electrical Engineering and her areas of expertise include stability, resilience, optimization, and control in power systems with high penetration of inverter-based resources; use of synchrophasor measurements for enhanced situational awareness and control; use of machine learning; and analysis of cascading outages. Marianna is an IEEE Fellow and has been recognized as IEEE PES Women Engineers and Achievers in Power & Energy. She is a member of Power & Energy Magazine Editorial Board, the immediate past Co-Chair of IEEE PES Corporate Engagement Program, a member of IEEE PES Industry Technical Support Leadership Committee, a member of Long-Range Planning subcommittee, and a VP of Marketing at CIGRE US National Committee. She's active in NERC, WECC, and NASPI communities.

Free and Open to the Public; RSVP is appreciated Visit the IEEE PES Boston Chapter website for further details - <https://site.ieee.org/boston-pes/>

For any questions regarding this presentation or any IEEE PES Boston Technical Meetings, please contact: Risa Karanxha (risa.karanxha@nationalgrid.com) or Chris Sweeny (christopher.sweeny@1898andco.com)

Time: Refreshments start at 6:00pm; Talk begins at 6:30pm

Location: Wentworth Institute of Technology Beatty 426 (Building: Beatty Hall) 550 Huntington Ave, Boston, MA 02115 (Free Parking at West Parking Lot)

Low Frequency Signal Integrity with Hardware Demonstrations



Lee Hill – SILENT Solutions LLC & GmbH

Sponsored by SILENT Solutions LLC & GmbH

The technical presentation will commence at 7:00PM following a social hour at 6:00 PM. Food and refreshments are provided.

Since most electrical engineers and PCB designers did not learn about low frequency signal integrity and grounding in school, it can be challenging for them to achieve good low frequency signal integrity that is vital to the performance of closed-loop systems. Precision measurements and A/D conversion of temperature, flow, pressure, current, and voltage in modern energy conversion and motion control systems are simply not possible without excellent low frequency signal integrity. During this presentation, using a signal generator, current and magnetic field probes, and an oscilloscope, Lee will model, demonstrate, and measure the signal integrity, emissions, and immunity problems that can arise in low frequency circuits.

Schedule:

6:00 pm: Registration/check-in, complimentary food and refreshments
 6:50 pm: Welcome from TÜV Rheinland North America and IEEE EMC Boston Chapter
 7:00 pm: Presentation by Lee Hill SILENT Solutions LLC & GmbH (abstract and bio below)
 7:45 pm: Q&A

Lee Hill has over 35 years of experience providing hands-on hardware troubleshooting and design reviews to solve and prevent elusive regulatory and functional electrical noise problems. Lee teaches EMC worldwide with enthusiasm, humor, and a pelican case full of hardware demos. He is Founding Partner of SILENT Solutions LLC and GmbH, two electromagnetic compatibility (EMC) and RF design, troubleshooting, and training firms established in 1992 and 2017. He is an EMC instructor for Worcester Polytechnic Institute (WPI) and University of Oxford (England). Lee enjoys jogging, motorcycling, table tennis, ham radio, and international travel. He speaks English, German, and rusty Spanish and sign language.

He earned his MSEE in electromagnetics from the Missouri University of Science and Technology EMC Laboratory. Lee is the named inventor of three US patents for EMI control in electronic systems and provides expert witness services for patent litigation.

Location: TÜV Rheinland North America, Technology and Innovation Center, 400 Beaver Brook Road, Boxborough, MA. Complimentary parking is available

Register:

<https://events.vtools.ieee.org/event/register/421240>

Please register no later than June 15 in order to ensure adequate seating & catering.

Thank you to our meeting sponsor!

Boston/Providence/New Hampshire Reliability Society – 5:30PM, Wednesday, June 26

Radiation Effects in Electronics: Brief Overview and History



We will begin with a brief overview of radiation effects in electronics, and their effect on reliability. Then we will cover the history of the discovery and our growing awareness of them, with special attention paid to the place of the Harvard Cyclotron Laboratory (HCL)/Massachusetts General Hospital (MGH) Rad Test program in that history. We will then look at what factors made HCL so prominent in the early work of understanding these effects, and why the re-purposing of equipment built at HCL for the MGH program was particularly useful in electronics reliability testing. Finally, we will finish with a few words on the future of the MGH test program.

Schedule:

5:30 PM Pizza, salad, soda, and networking
6:00 PM Technical Presentation
6:45 PM Questions and Answers
7:00 PM Adjournment

Ethan Cascio - Radiation Effects in Electronics: Brief Overview and History

Ethan Cascio joined the staff of the Harvard Cyclotron Laboratory (HCL) in 1985 after receiving his BA in Physics from Reed college. Over the next 17 years at HCL he worked on both the joint project to develop proton therapy in collaboration with Massachusetts General Hospital (MGH) and the radiation effects testing program at HCL. He eventually became Operations Man-

ager of the lab and primarily responsible for the radiation effects program. When Harvard closed HCL in 2002 following the transfer of the clinical treatment programs to the newly built Northeast Proton Therapy Center at MGH (later re-named the Burr Proton Therapy Center) he moved with the project over to MGH and became the Radiation Test Program Manager at the Burr center. At the Burr Center he established and continues to run the radiation test program, as well as provides clinical physics and engineering support for the proton therapy program. He is the author and co-author of numerous papers on the subjects of proton therapy, dosimetry, radiation effects in electronics and proton beamline design and instrumentation.

The meeting is open to all. You do not need to belong to the IEEE to attend this event; however, we welcome your consideration of IEEE membership as a career enhancing technical affiliation.

Please visit <https://r1.ieee.org/boston-rl/>

Location: In Person and Virtual Event – Lincoln Laboratory, 244 Wood Street, Lexington, MA. Main Cafeteria

There is no cost to register or attend, but registration is required.

Registration:

<https://events.vtools.ieee.org/m/420285>

IEEE Boston Section Social Media Links:

Twitter: <https://twitter.com/ieeeboston>

Facebook: <https://www.facebook.com/IEEEBoston>

YouTube: <https://www.youtube.com/user/IEEEBostonSection>

LinkedIn: <https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about>

Introduction to Neural Networks and Deep Learning (Part I)

Web-based Course with live Instructor!

Times & Dates: 8:30AM - 12:30PM ET, Saturday, October 26, 2024

Speaker: CL Kim

Course Format: Live Webinar, 4 hours of instruction!

Series Overview: Neural networks and deep learning currently provides the best solutions to many problems in image recognition, speech recognition, and natural language processing."

Reference book: "Neural Networks and Deep Learning" by Michael Nielsen, <http://neuralnetworksanddeeplearning.com/>

This Part 1 and the planned Part 2 (to be confirmed) series of courses will teach many of the core concepts behind neural networks and deep learning.

More from the book introduction: We'll learn the core principles behind neural networks and deep learning by attacking a concrete problem: the problem of teaching a computer to recognize handwritten digits. ...it can be solved pretty well using a simple neural network, with just a few tens of lines of code, and no special libraries."

"But you don't need to be a professional programmer."

The code provided is in Python, which even if you don't program in Python, should be easy to understand with just a little effort.

Benefits of attending the series:

- * Learn the core principles behind neural networks and deep learning.
- * See a simple Python program that solves a concrete problem: teaching a computer to recognize a handwritten digit.
- * Improve the result through incorporating more and more core ideas about neural networks and deep learning.
- * Understand the theory, with worked-out proofs of fundamental equations of backpropagation for those interested.
- * Run straightforward Python demo code example.

The demo Python program (updated from version provided in the book) can be downloaded from the speaker's GitHub account. The demo program is run in a Docker container that runs on your Mac, Windows, or Linux personal computer; we plan to provide instructions on doing that in advance of the class.

(That would be one good reason to register early if you plan to attend, in order that you can receive the straightforward instructions and leave yourself with plenty of time to prepare the Git and Docker software that are widely used among software professionals.)

Course Background and Content: This is a live instructor-led introductory course on Neural Networks and Deep Learning. It is planned to be a two-part series of courses. The first course is complete by itself and covers a feedforward neural network (but not convolutional neural network in Part 1). It will be a pre-requisite for the planned Part 2 second course. The class material is mostly from the highly-regarded and free online book "Neural Networks and Deep Learning" by Michael Nielsen, plus additional material such as some proofs of fundamental equations not provided in the book.

Outline:

Feedforward Neural Networks.

- * Simple (Python) Network to classify a handwritten digit
- * Learning with Stochastic Gradient Descent
- * How the backpropagation algorithm works
- * Improving the way neural networks learn:
 - ** Cross-entropy cost function
 - ** Softmax activation function and log-likelihood cost function
 - ** Rectified Linear Unit
 - ** Overfitting and Regularization:
 - *** L2 regularization
 - *** Dropout
 - *** Artificially expanding data set

Pre-requisites: There is some heavier mathematics in learning the four fundamental equations behind backpropagation, so a basic familiarity with multivariable calculus and matrix algebra is expected, but nothing advanced is required. (The backpropagation equations can be also just accepted without bothering with the proofs since the provided Python code for the simple network just make use of the equations.) Basic familiarity with Python or similar computer language.

Speaker Background: CL Kim works in Software Engineering at CarGurus, Inc. He has graduate degrees in Business Administration and in Computer and Information Science from the University of Pennsylvania. He had previously taught for a few years the well-rated IEEE Boston Section class on introduction to the Android platform and API.

**Decision (Run/Cancel) Date for this Course is
Friday, October 18, 2024**

Payment	on/by Oct. 1	After Oct. 1
IEEE Members	\$95	\$110
Non-members	\$115	\$130

https://ieeeboston.org/event/neuralnetworks/?instance_id=3598

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically diverse sections of the IEEE. We have over 20 active chapters and affinity groups. If you have an expertise that you feel might be of

interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is

<http://ieeeboston.org/course-proposals/>. Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- **Honoraria can be considered for course lecturers**
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course)
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Digital Signal Processing (DSP) for Software Radio

Dates & Times: Course Kick-off/Orientation, 6 - 6:30PM ET, Thursday, June 13
 Live Workshops: 6:00 - 7:30PM ET; Thursdays, June 20, 27, July 11, 18, 25
 First Video Release, Thursday, June 13, 2024, additional videos released weekly in advance of that week's live session!

Speaker: Dan Boschen
Location: Zoom

Attendees will have access to the recorded session and exercises for two months (until August 20, 2024) after the last live session ends!

This is a hands-on course providing pre-recorded lectures that students can watch on their own schedule and an unlimited number of times prior to live Q&A/Workshop sessions with the instructor. Ten 1.5 hour videos released 2 per week while the course is in session will be available for up to two months after the conclusion of the course.

Course Summary This course builds on the IEEE course "DSP for Wireless Communications" also taught by Dan Boschen, further detailing digital signal processing most applicable to practical real-world problems and applications in radio communication systems. Students need not have taken the prior course if they are familiar with fundamental DSP concepts such as the Laplace and Z transform and basic digital filter design principles.

This course brings together core DSP concepts to address signal processing challenges encountered in radios and modems for modern wireless communications. Specific areas covered include carrier and timing recovery, equalization, automatic gain control, and considerations to mitigate the effects of RF and channel distortions such as multipath, phase noise and amplitude/phase offsets.

Dan builds an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real-world applications for mixed

signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges, rather than a tutorial on implementations with DSP processors.

Now with Jupyter Notebooks! This long-running IEEE Course has been updated to include Jupyter Notebooks which incorporates graphics together with Python simulation code to provide a "take-it-with-you" interactive user experience. No knowledge of Python is required but the notebooks will provide a basic framework for proceeding with further signal processing development using that tools for those that have interest in doing so.

This course will not be teaching Python, but using it for demonstration. A more detailed course on Python itself is covered in a separate IEEE Course routinely taught by Dan titled "Python Applications for Digital Design and Signal Processing".

All set-up information for installation of all tools used will be provided prior to the start of class.

Target Audience: All engineers involved in or interested in signal processing for wireless communications. Students should have either taken the earlier course "DSP for Wireless Communications" or have been sufficiently exposed to basic signal processing concepts such as Fourier, Laplace, and Z-transforms, Digital filter (FIR/IIR) structures, and representation of complex digital and analog signals in the time and frequency do-

if you are uncertain about your background or if you would like more information on the course.

Benefits of Attending/ Goals of Course:

Attendees will gain a strong intuitive understanding of the practical and common signal processing implementations found in modern radio and modem architectures and be able to apply these concepts directly to communications system design.

Topics / Schedule:

Class 1: DSP Review, Radio Architectures, Digital Mapping, Pulse Shaping, Eye Diagrams

Class 2: ADC Receiver, CORDIC Rotator, Digital Down Converters, Numerically Controlled Oscillators

Class 3: Digital Control Loops; Output Power Control, Automatic Gain Control

Class 4: Digital Control Loops; Carrier and Timing Recovery, Sigma Delta Converters

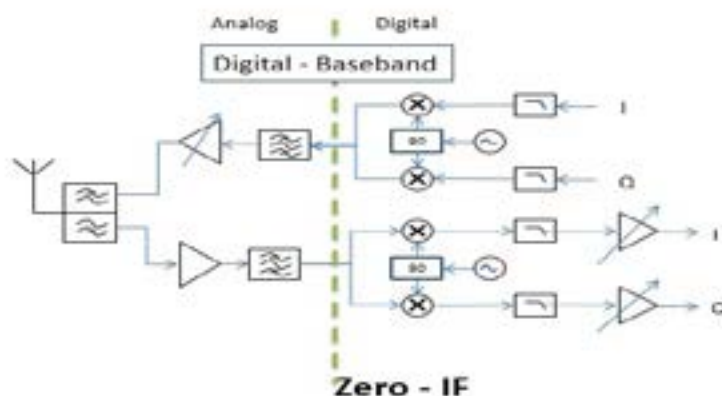
Class 5: RF Signal Impairments, Equalization and Compensation, Linear Feedback Shift Registers

Speaker's Bio:

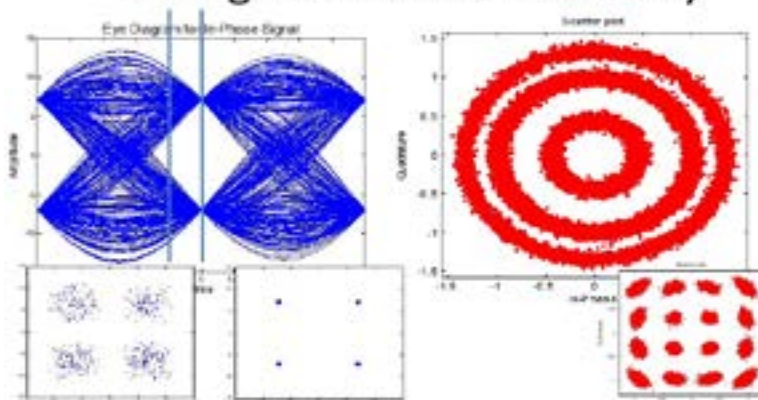
Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems and has taught courses on DSP to international audiences for over 15 years. Dan is a contributor to Signal Processing Stack Exchange <https://dsp.stackexchange.com/>, and is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page at: <http://www.linkedin.com/in/dan-boschen>

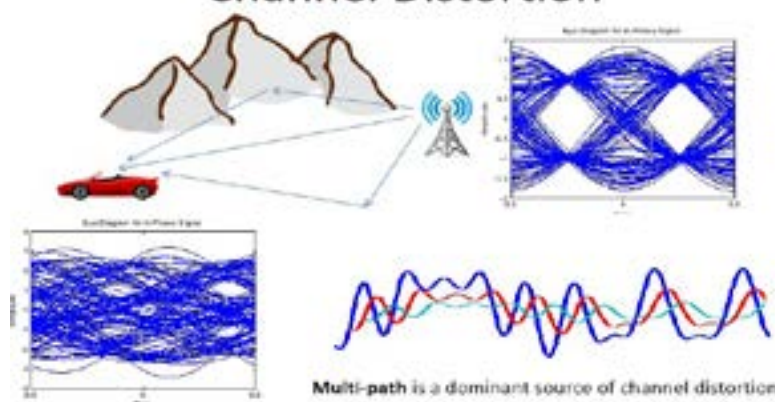
Radio Architectures



Timing and Carrier Recovery



Channel Distortion



**Decision (Run/Cancel) Date for this Course is
Thursday, June 6, 2024**

	By May 30	After May 30
IEEE Members	\$190	\$285
Non-members	\$210	\$315

https://ieeeboston.org/event/dspswradio/?instance_id=3560

Advanced Digital Design: Implementing Deep Machine Learning on FPGA

Times & Dates: 6 - 7:30PM, Mondays, September 16, 23, 30, October 7
Speaker: Kendall Farnham, Dartmouth College

Hosted by

Location: MITRE Corporation, Bedford, MA
 (This course will be offered in person and live online)



Course Overview:

Field-programmable gate arrays (FPGAs) are versatile integrated circuits that offer a flexible and reconfigurable hardware platform for implementing custom digital circuits, particularly in applications requiring specialized architectures. Unlike application-specific integrated circuits (ASICs), FPGAs can be programmed and re-programmed after manufacturing using hardware description languages (HDLs), enabling rapid prototyping and iterative design processes. FPGAs can be found in telecommunications, signal processing, aerospace, and other scenarios demanding high-performance computing, parallel processing, low-latency data processing, and real-time operations. The newest trends include integrating FPGAs with systems on chip (SoCs) for implementing low-latency machine learning (ML) and artificial intelligence.

This Advanced Digital Design course is an intensive program designed to build upon foundational concepts in digital logic design and equip students with the skills needed to implement robust high-speed ML algorithms on an FPGA. Through a combination of theoretical lectures, hands-on exercises, and practical projects, students will explore advanced FPGA topics encompassing architectural considerations, signal integrity, timing analysis, and optimization techniques to achieve reliable and efficient high-speed designs. Additionally, this course will encourage students to explore current research papers and real-world industry applications to foster a deeper appreciation for advancements in state-of-the-art FPGA design.

Target audience:

Students and professionals with a base knowledge of FPGA design looking to advance hardware design skills for developing complex customized circuits for efficient implementation of ML.

Benefits of attending:

- Valuable professional development creating skills that lead to job offers
- Reinforce and expand knowledge of VHDL and FPGA-specific design methodology.
- Develop skills for implementing high-speed, robust, reliable circuits on FPGAs.
- Gain understanding of real-world industry applications of FPGAs and SoCs.

Course Objectives:

By the end of this course, students will possess the expertise needed to tackle complex high-speed hardware design challenges using FPGAs. They will be well-prepared to contribute to cutting-edge research, industry projects, and advancements in areas such as telecommunications, data centers, embedded systems, and high-performance computing.

Prerequisites:

- Understanding of digital logic design principles and methodology (e.g., Boolean algebra, finite state machines, data path elements)
- Familiarity with VHDL programming (or Verilog)
- Experience with FPGA development boards and tools (e.g., Vivado)

Speaker Bio:

Kendall Farnham is a PhD candidate in Dr. Ryan Halter's bioimpedance lab at the Thayer School of Engineering, Dartmouth College. She has 10+ years of experience in the electrical and computer engineering (ECE) field and 5+ years of teaching and mentoring experience, having held several leadership positions within academia and industry. She received her bachelor's degree in ECE in 2014, worked in the defense industry as a software engineer for 4 years where she discovered her passion for research, and returned to

school to expand her education to include hardware design for space medicine applications. Specifically, she is interested in FPGA-based biomedical device design, currently working to develop space-compatible technologies that use impedance to monitor and detect physiological effects of space travel. Her expertise includes high-performance FPGA-based digital system design, analog circuit design, multi-modal imaging algorithms, and system integration.

Course Outline:

1. Review of Digital Logic Design and FPGA Programming

- Boolean algebra, combinational and sequential circuits, finite state machines
- FPGA, SoC, and SoM architectures and tool-chains
- VHDL programming techniques and design methodology
- Writing effective testbenches, RTL simulation in Vivado
- Introduction to ML algorithms and FPGA-specific optimization strategies

2. High-throughput Communication on FPGAs

- Pipelining and parallelism for high-speed designs
- Synchronous vs. asynchronous communication protocols (SPI, SCI, UART, LVDS, I2C, PCIe, USB, Ethernet, etc.)
- Compare hardware/software/firmware implementations of ML: throughput speeds, resource utilization, and latency
- Methods used to achieve ultra-high sampling rates ($\gg$ system clock, GS/s range)
- Utilizing advanced IP cores and IO buffers for high-speed interfaces and data storage

3. Advanced FPGA Techniques for High-speed Systems

- Clock domain crossing verification and synchronization techniques

- Resource utilization, critical path identification, and optimization strategies
- Timing constraints, static and dynamic timing analysis
- Signal integrity analysis

4. High-Speed Design Verification and Testing

- Simulation-based verification techniques, advanced debugging, and waveform analysis
- Post-layout verification and back-annotation
- Test and validation strategies for high-speed designs

- Utilizing debug cores for real-time logic analysis

5. Machine Learning on FPGAs

- Algorithm validation and verification in software
- Compare capabilities and implementation strategies of ML on FPGAs, SoCs, and SoMs
- Optimization strategies for efficient ML implementation in hardware (e.g., convolution)

6. Digital Systems in Industry

- Techniques and best practices for scalable, reusable, reliable, and robust FPGA design
- Board-level considerations for high-speed signals: PCB layout guidelines, power distribution and decoupling, transmission line theory and termination techniques
- Emerging trends for FPGA-based digital signal processing (DSP) applications

CEU/PDH are available upon request. A small fee may apply for the credits

**Decision (Run/Cancel) Date for this Course is
Monday, September 9, 2024**

Payment	By Sept. 3	After Sept. 3
IEEE Members	\$120	\$140
Non-members	\$250	\$300

https://ieeeboston.org/event/advanced-digital-design/?instance_id=3481



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