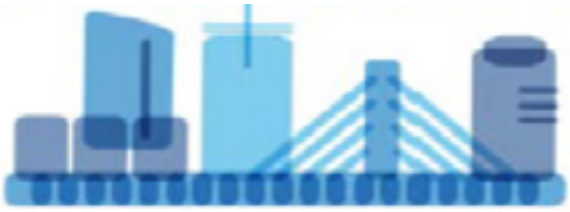

Boston Section

Supporting students, working engineers and retirees through professional development, education and resources.

THE Reflector

ISSUE #9
SEPTEMBER 2025

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IEEE HPEC: New England's Flagship Conference for High Performance and Embedded Computing

By Dr. Joseph Campbell, IEEE Life Fellow, Laboratory Fellow, MIT Lincoln Laboratory

Dr. Joseph Campbell

Introduction

I'm honored to contribute my first editorial to The Reflector. I'm grateful to IEEE President Kathleen Kramer for appointing me to membership development roles in both IEEE Region 1 and the IEEE Boston Section. This led to me joining the Executive Committee, which I'm thoroughly enjoying and I highly recommend IEEE volunteering activities!

The timing for this piece couldn't be better. The IEEE High Performance Extreme Computing (HPEC) Conference is just around the corner (September 15-19). Registration will remain open throughout the conference—check it out at: https://ieee-hpec.org

HPEC's Unique Mission

IEEE HPEC's mission is simple but bold: advance the art and science of extreme computing in support of academic, government, and commercial needs. It focuses on performance at every level; from single-chip innovations to global-scale infrastructure, from theory to implementation, and from training AI models to deploying them on the edge.

Unlike other major computing conferences, HPEC prioritizes broadening the field. HPEC's peer-review philosophy focuses on accepting all qualified papers to ensure that strong, relevant work, especially from students, early-career researchers, and interdisciplinary teams, gets the attention it deserves.

Virtual by Design, Not Just by Necessity

HPEC went fully virtual in 2020, but not just as a stopgap. According to IEEE Senior Member Dr. Jeremy Kepner, the shift was already under discussion before the pandemic. Once the opportunity emerged, the team committed early, communicated clearly, and built a custom infrastructure to support a virtual-first future.

This strategic pivot paid off: submissions surged, registration costs were cut in half, and participation expanded dramatically across geographic and institutional boundaries. Attendance per session now averages 70–150, compared to 20–25 in the in-person era, and 2025 saw a record number of paper submissions. HPEC runs five days of sequential, high-tempo programming, with each session as its own event, optimized for short attention spans and global time zones, further enhancing accessibility.

Importantly, HPEC has full archival proceedings in IEEE Xplore, but HPEC is not recorded. As Dr. Kepner puts it, "We treat it like live theater." This encourages spontaneity, minimizes speaker concerns about recordings, and allows post-session breakout rooms for deeper conversations to virtually recreate the hallway chats and Q&A clusters that give conferences life. Building on this success, HPEC doubled down on another core value: accessibility.

Dr. Jeremy Kepner

Accessibility as a Core Value

Accessibility is more than a buzzword, it's HPEC's design principle. Virtual participation allows those with family obligations, physical limitations, or travel restrictions to engage deeply without leaving home. Many attend only the sessions most relevant to them, a flexibility that's rare in traditional formats. And thanks to support from corporate sponsors and IEEE Boston Section, complimentary registration is available to many non-authors. This creates a virtuous cycle: greater accessibility brings broader participation, richer discussions, and more visibility for accepted work.

"Accessibility is everything to us," said Dr. Kepner. "The number of people who see each presentation has dramatically increased. Our goal is to grow the field and that means lowering barriers for everyone interested in extreme computing."

For other IEEE Sections or organizers considering hybrid or virtual futures, the HPEC model is a strong case study. It leverages a suite of tools (including Zoom, Cvent, Microsoft CMT, Engagez, and in-house automation) to provide a seamless integrated experience for chairs, presenters, and especially attendees. IEEE Senior Member Dr. Albert Reuther added, "The custom automation and integration of the suite of tools enables us to go from paper submission, through the review process and paper updates, to presentations during the conference week in about two months, this enables researchers to present and share results with the community in a very timely manner."

HPEC's success stems from continuity, trust, and the strategic vision of a stable team that includes not just Kepner and Reuther, but IEEE Boston Section Business Manager Trina Lorigan; former IEEE Boston Section Business Manager Bob Alongi; IEEE Boston Section Office Manager Karen Safina; and web developer Kathleen Ballos, whose years of support have made consistent delivery possible.

A Home for Cutting-Edge Work

Because of the world-leading nature of today's supercomputing platforms, much of the work being done on them is publishable in IEEE HPEC. The conference provides a convenient, rapid, and archival venue for innovations that span theory, systems, and applications. Topics include:

•High Performance Computing and Supercomputing
•Artificial Intelligence, Machine Learning, and Generative AI
•Large Language Models, CNNs, DNNs, and Edge Inference
•Big Data, Distributed Computing, and Graph Analytics
•General-Purpose GPUs and Quantum/Hybrid Architectures
•Cybersecurity, Secure Systems, and Fault Tolerance
•Embedded, Real-Time, and Mixed-Precision Computing
•Benchmarking, AI for Performance Optimization, and Multicore Software

Distinguished Speakers and Community-Led Sessions

HPEC attracts outstanding invited speakers each year, including luminaries from MIT, NVIDIA, Intel, Microsoft, Federal Laboratories, and abroad. Recent talks have covered safe autonomy, biodiversity AI, privacy-preserving analytics, and optimization for mobility and energy.

Dr. Albert Reuther

Equally compelling are the special topic sessions organized by the community. These have included:

•GenAI Opportunities and AI Challenges
•Bridging Quantum and High-Performance Computing

•Age of Mixed Precision
•MIT/Amazon/IEEE Graph Challenge
•BRAINS: Building Resilience through AI for Networked Systems
•GraphBLAS Forum
•Scaling Research Computing Education

A Boston Section Success Story

Although HPEC is globally attended, it is deeply rooted in the IEEE Boston Section. Launched over 25 years ago as an MIT Lincoln Laboratory workshop, it joined the Boston Section officially over a decade ago. That partnership has yielded a powerful blend of local continuity and global influence.

Boston Section members play vital roles as authors, reviewers, chairs, and attendees. You can take pride in HPEC's impact. Boston section members are encouraged to attend and support the conference by:

•Submitting work from your lab, startup, or university
•Encouraging students to attend and present
•Citing HPEC publications in your work
•Spreading the word to colleagues and collaborators

Looking Ahead

The next IEEE HPEC Conference will be held virtually from September 15–19, 2025. Information on registration, submissions, and special sessions is at https://ieee-hpec.org/. Paper submissions typically open in March and close in July, with reviews in August.

As AI, HPC, and embedded computing continue to converge, HPEC provides a forum that's timely, accessible, and impactful. It exemplifies what's possible when IEEE Sections embrace the future and invest in the long game.

Whether you're presenting new results, mentoring junior researchers, or exploring cutting-edge platforms, I invite you to engage with IEEE HPEC. Join us this September to discover where performance meets purpose at HPEC!

Dr. Joseph P. Campbell, an IEEE Life Fellow, is a Laboratory Fellow at MIT Lincoln Laboratory (MIT LL) specializing in artificial intelligence technologies for national security. Since joining MIT LL in 2001, he has led groups advancing human language technology, deep learning for cyber analytics, and operational evaluation methods, delivering significant mission impact for U.S. government applications. His leadership has extended to major programs in forensic speaker recognition, biometrics, big data analytics, and technologies for combating human trafficking, with innovations transitioned to operational use by the U.S. government.

An active IEEE volunteer, Dr. Campbell has served as a distinguished lecturer, editor, and officer in multiple IEEE roles, and currently co-chairs MIT LL's Professional Societies Committee. He has authored more than 120 publications with over 8,000 citations, holds a U.S. patent, and has led multiple U.S. Federal and NATO speech-coding standards. His technical leadership has been recognized with MIT LL's highest honor, the Technical Excellence Award, and numerous national awards in biometrics and speech processing.
Dr. Campbell earned his BS, MS, and PhD in electrical engineering from Rensselaer Polytechnic Institute, Johns Hopkins University, and Oklahoma State University, respectively.

Dr. Jeremy Kepner is an MIT Lincoln Laboratory Fellow. He founded the Lincoln Laboratory Supercomputing Center and pioneered the establishment of the Massachusetts Green High Performance Computing Center. He has developed novel big data and parallel computing software used by thousands of scientists and engineers worldwide. He has led several embedded computing efforts, which earned him a 2011 R&D 100 Award. Kepner has chaired the SIAM Data Mining conference, the IEEE Big Data conference, and the IEEE High Performance Extreme Computing conference. Kepner is the author of three books, Parallel MATLAB for Multicore and Multinode Computers, Graph Algorithms in the Language of Linear Algebra, and Mathematics of Big Data. His peer-reviewed publications include works on abstract algebra, astronomy, astrophysics, cloud computing, cybersecurity, data mining, databases, graph algorithms, health sciences, plasma physics, signal processing, and 3D visualization. In 2014, he received Lincoln Laboratory's Technical Excellence Award.
Kepner holds a BA degree in astrophysics from Pomona College and a PhD degree in astrophysics from Princeton University.

Dr. Albert Reuther is a senior staff member in the MIT Lincoln Laboratory Supercomputing Center (LLSC). He brought supercomputing to Lincoln Laboratory through the establishment of LLGrid, founded the LLSC, and leads the LLSC Computational Science and Engineering team. He developed the gridMatlab high-performance computing (HPC) cluster toolbox for pMatlab and is the computer system architect of the MIT Supercloud and numerous interactive supercomputing clusters based on Supercloud, including those in the LLSC.

As a computational engineer, he has worked with many teams within the Laboratory and beyond to develop efficient parallel and distributed algorithms to solve a wide array of computational problems. The Supercloud architecture earned him an Eaton Award for Design Excellence and his computational engineering work earned him a 2017 R&D 100 Award. He is the technical chair of the IEEE High Performance Extreme Computing Conference and has organized numerous workshops on interactive HPC, cloud HPC, economics of HPC, and HPC security. His areas of research include interactive HPC; computer architectures for machine learning, graph analytics, and parallel signal processing; and computational engineering.

Reuther earned BS, MS, and PhD degrees in computer and electrical engineering from Purdue University and an MBA degree from the Collège des Ingénieurs in Paris, France, and Stuttgart, Germany.

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IEEE Boston MTT/AP-S DML - 5:30PM, Thursday, September 11

Power Without Pain: High Power MMIC PA Design, the Pitfalls and how to Avoid Them

Time: 5:30 PM, Thursday, September 11

Location: MITLL, 3 Forbes Rd, Lexington, MA

Event Registration: https://events.vtools.ieee.org/m/469449

We will have a social period from 5:30-6pm, followed by the technical seminar from 6-7pm. Pizza and drinks will be provided. Please note if you have any dietary restrictions.

Please join the IEEE Boston MTT/AP-S Chapter for a free in-person DML seminar with Dr. Michael Roberg “Power Without Pain: High Power MMIC PA Design, the Pitfalls and how to Avoid Them”

This presentation discusses high power monolithic microwave integrated circuit (MMIC) power amplifier (PA) design in Gallium Arsenide (GaAs) and Gallium Nitride (GaN). At a high level, GaN versus GaAs semiconductor technology from the perspective of power amplifier design metrics is analyzed to help determine the relative advantages and disadvantages of each technology.

This is followed with an introduction of the most prevalent MMIC design topologies for the bulk of microwave applications which include reactively matched, non-uniform distributed, balanced, push-pull, Doherty and serially combined. Following introduction of the main topologies, the presentation focuses on the potential pitfalls the MMIC designer can encounter with detailed discussion on how to avoid them with the goal of first past design success.

The presentation relies on experience from the author’s career with over 20 years of experience in the defense and commercial industries as well as academia. MMIC designers will appreciate the candid explanation of the design topologies and pitfalls while non-designers will come away with a good working knowledge of what can be achieved and what to watch out for.shared.

Michael Roberg (pictured below) received the Ph.D. degree from the University of Colorado at Boulder in 2012. From 2003 to 2009, he was an engineer at Lockheed Martin-MS2 in Moorestown, NJ working on advanced phased array radar systems. From 2012 to 2022 he worked for Qorvo in the High Performance Analog business unit as a MMIC Design Engineering Fellow. In 2021, he received the Outstanding Young Engineer award from MTT-S and in 2022 he won the

industry paper competition at IMS in Denver. From 2022-2024 he was an Engineering Fellow at mmTron, Inc. where he focused on MMIC development for millimeter wave systems. Michael re-joined Qorvo as a member of the research organization in 2024 and continues to focus on advanced MMIC development.

IEEE Boston Photonics Chapter – 6:00PM, Thursday, September 11

Advances in Low-Loss Chip-to-Chip Couplers and BSU Opportunities for Photonic Education and Prototyping

Time: 6:00 PM, Thursday, September 11

Location: MIT Lincoln Laboratory, Forbes Rd. Cafeteria, 3 Forbes Rd., Lexington, MA

Speaker: Dr. Samuel Serna, Bridgewater State University in MA

Registration: https://events.vtools.ieee.org/m/497468

Light meals will be served (free, registration required).

6:00 pm Networking starts
6:15 pm Light meals served
7:00 pm Seminar starts

The exponential growth of global data traffic and the energy demands of data centers have accelerated the need for high-density, low-loss optical interconnects. Recent advances in co-packaged optics have demonstrated vertical silicon-to-silicon nitride chip-to-chip evanescent couplers with sub-dB loss and passive alignment tolerances suitable for scalable assembly using standard CMOS-compatible processes. These developments address one of the key bottlenecks in photonic integration—reducing cost and complexity in packaging while enabling terabit-to-petabit per second bandwidth scaling.

This presentation will highlight recent results on waveguide-to-waveguide couplers, including broadband vertical coupling strategies, graded-index concepts for efficient fan out, and the potential impact of such technologies on co-packaged optics and heterogeneous integration. Beyond research, this talk will also discuss workforce development and educational pathways in photonics. Bridgewater State University hasestablished the first undergraduate program in Photonics and Optical Engineering in New England, designed to train the next generation of engineers in integrated photonics, optical communications, and packaging. Furthermore, the Laboratory for Education and Application Prototyping (LEAP) at BSU provides unique opportunities for undergraduate students and industry partners to prototype, and test photonic devices in collaboration with MIT and many other players in the region. By bridging cutting-edge photonic packaging research with innovative education and accessible prototyping facilities, this work outlines both the technical advances and the ecosystem required to sustain U.S. leadership in integrated photonics and address the pressing challenges of data-driven innovation.

Samuel Serna (pictured left) **i**s an Associate Professor in the Department of Physics and Photonics and Optical Engineering at Bridgewater State University in Massachusetts, USA. He earned his Ph.D. in 2016 from the University of Paris-Sud / Paris-Saclay, where he
focused on the design and characterization of passive silicon photonic devices and developed techniques to probe their third-order nonlinear optical properties.

Following his doctoral work, he was a postdoctoral researcher at the Centre for Nanoscience and Nanotechnology (C2N) and later a postdoctoral associate at MIT,where he continues to collaborate as a visiting scientist to develop hybrid photonic devices for telecommunications and mid-infra**red** applications.

Dr. Serna leads initiatives to expand access to integrated photonics education andsustainable microchip manufacturing. He is an OPTICA Ambassador (2019) and a Senior Member (2022) and has served on the SPIE Editorial Board. His research interests include integrated photonics, nonlinear optics, photonic packaging, and scalable photonic systems.

IEEE Boston Section

IEEE Women in Engineering WIE

Senior Member Elevation Breakfast

Empowering Women in Engineering and Technology

Date: Saturday, September 13, 2025

Time: 9:30 AM—12:00 PM

Location: The Mill Café
14 Mill Street, Arlington, NZ76

Join us for a morning of networking, mentorship, and celebration as we encourage and support female IEEE members on the path to Senior Member elevation.

- Guidance on qualifications and application
- Peer support and shared success stories
- Complimentary breakfast and coffee
- A welcoming community of women in tech leadership

Who Should Attend:

- Female IEEE Members (any grade level)
- Those considering or eligible for Senior Member elevation
- Supporters and advocates for diversity in leadership

Space is limited — reserve your spot today!

IEEE Senior Member is the highest grade for which a member may apply Only 10 % of IEEE members achieve this distinction.

Let's make sure more women are represented among them.

IEEE Boston Blockchain – 10:00 AM, Saturday, September 13

DeSci Boston Conference -- Decentralized Science as the Operating System for Open Scholarship

IEEE Boston Blockchain is a knowledge partner for DeSci Boston.

Time: 10:00 AM, Saturday, September 13

Location: MIT Media Lab

Event Registration Information: here.

This event weaves knowledge sharing with collective workshops to explore how Decentralized Science (DeSci) enacts Open Science principles by enabling transparent and auditable research processes through blockchain technology. We'll explore how these tools can minimize the increasing review burden, fund peer reviewers, certify data integrity, and support FAIR data management across organizations.

Through this event we hope to gather researchers with tool builders and thought leaders so each new innovation is accountable to building a more modular, open, and collective research world.

Register ($10): https://lu.ma/wgv2box9

NOTE: For academic attendees, SOLBoston will provide a refund on the day of the event if you sign up with your academic email.

More about DeSci Boston:

DeSci Boston'25 is our third event uniting scientists, patients, pharma, funders, technologists, and other stakeholders to re-envision how science is done and shared.

A wide variety of innovative technological solutions have been demonstrated in the past, including permanent & transparent knowledge repositories, improved data storage & access systems, governance infrastructure tooling, novel funding pipelines, redesigned processes for scientific societies, open licensing solutions, and cloud lab frameworks for world-wide wet-lab access.

DeSci Boston provides a platform for these projects to showcase the work they have done, share problems they see in the space, and the milestones they plan to accomplish.

IEEE Boston CNET – 6:30 PM, Monday, September 15

Discussion about AI Training for Members

This is a CNET Board of Directors open meeting featuring a discussion about AI training for members

Time: 6:30 PM, Monday, September 15

Location: Great Wall Restaurant, 309 Great Rd, Bedford - free dinner included

Event Registration: www.bostonconsultants.org

The Board will introduce the topic of the AI impact on consultancy practice and will moderate the participants' conversation regarding the need and benefits of CNET members' AI training.

IEEE Boston Reliability Chapter – 5:00PM, Wednesday, September 17

Additive Manufacturing of Microelectronics including Passive and Active Components for 3D HI and Advanced Packaging

Time: 5:00 PM, Wednesday, September 17

Location: MIT Lincoln Laboratory
244 Wood Street, Lexington, MA -- Main Cafeteria

Event Registration: https://events.vtools.ieee.org/m/497579

We introduce a new sustainable and scalable technique to manufacture nano and microelectronics additively. The technique eliminates etching, vacuum deposition, and other chemically intensive processing by utilizing direct assembly of nanoscale particles or other nanomaterials at room temperature and atmospheric pressure onto an interposer, wafer, or board. The presented technology enables the printing of crystalline conductors and semiconductors. The technology enables the additive manufacturing of passive and active components including logic gates at the nano and microscale using a purely additive (directed assembly enabled) process utilizing inorganic semiconductors, metals, and dielectrics nanoparticles. The process demonstrates the manufacturing of transistors with an on/off ratio greater than 106. This new technology enables the fabrication of nanoelectronics and electronic components while reducing the cost by 10-100 times and can print 1000 faster and 1000 smaller (down to 25nm) structures than ink-jet-based printing. Results showing passive and active components will demonstrate high-throughput printing of interconnects and circuit components at a scale equal to or less than 2 microns. Fully additively manufactured capacitors printed on silicon and sapphire substrates will be presented. The results will show printed capacitors ranging down to 20 x 20 µm with capacitance of femto Farad to nano Farads. The results will show additively printed logic gates such as NAND and MOSFET with high on/off ratios. This new Fab-in-a-Box platform is designed to print electronics and products with minimum features down to 300 nm for several advanced packaging applications.

Ahmed A. Busnaina, Ph.D. (pictured below), is the founding Director of the National Science Foundation's Nanoscale Science and Engineering Center for High-rate Nanomanufacturing since 2004 and the NSF Center for Microcontamination Control at Northeastern University, Boston, MA, since 2002. He is also the founder and CTO of Nano OPS, Inc. since 2017. Prior to joining Northeastern University, he was a professor and a director of the Particulate Control Lab at Clarkson University from 1984-2000. Dr. Busnaina is internationally recognized for his work on semiconductor fabrication with an emphasis on yield. He also developed nano and microscale additive manufacturing for making interconnects, passive and active electronic components, LEDs, and sensors. He authored more than 600 papers in journals, proceedings, and conferences. He also has 25 granted and more than 45 pending patents. He was awarded the 2020 American Society of Mechanical Engineers (ASME) William T. Ennor Manufacturing Technology Award and Medal. He is a fellow of the National Academy of Inventors, a fellow of the American Society of Mechanical Engineers, and a Fulbright Senior Scholar. He is an editor of the Journal of Microelectronic Engineering. He also serves on many advisory boards, including Samsung Electronics, the Journal of Electronic Materials Letters, the Journal of Nanomaterials, and the Journal of Nanomanufacturing.

IEEE Electromagnetic Compatibility Society - 8:00AM, Wednesday, September 24

Annual EMI/EMC Summit

Time: 8:00 AM, Wednesday, September 24

Location: 1146 Massachusetts Avenue Boxborough, MA

Event Details & Registration here.

Dear members of the EMC community,

Please, mark your calendars for our annual EMI/EMC Summit, at the Element Materials Technology facility, in Boxborough, MA, 01719. The event is sponsored by IEEE EMC Society Boston Chapter. The attached PDF file provides abstracts of the upcoming presentations. This 2025 free EMI/EMC Summit is happening on Wednesday, September 24, 2025, starting at 8:00 AM.

Join us for a full-day symposium featuring four expert speakers presenting on the latest developments in EMI/EMC testing. This event will provide timely, industry-focused information to help you make informed decisions and stay ahead in the field.

Key Features:

5 expert speakers
All-day lab tours
Vendor exhibitions
Breakfast and lunch included
Topics Include:

MIL STD 461
PI Challenges
Lightning Protection
HIRF Methods

Don’t miss this opportunity to be a part of an insightful summit!

Regards,
Boris Shusterman
IEEE EMC Society Boston Chapter

IEEE Boston Section Life Members (cohosted by NH Life Members) – 2:00PM, Wednesday, September 24

Artificial Intelligence for Everyday

Time: 5:00 PM, Wednesday, September 17

Location: Morrison Theatre, Newbury Court, 100 Newbury Court, Concord, MA (see directions in the righthand column). Parking is limited at Newbury Court, so registration via vTools is important.

Speaker: Reshmi Ghosh, Microsoft

Event Registration: https://events.vtools.ieee.org/m/498144

Abstract:

Artificial Intelligence (AI) is no longer just a futuristic idea, it is already making daily life more productive. In this talk, we will explore how AI-powered assistants can support independence and improve quality of life in assisted living communities. From helping manage medications and appointments, to providing companionship through natural conversations, AI is becoming a gentle, reliable partner.

We will highlight real examples of how these technologies are opening new possibilities: people living with dementia are now able to create art simply by describing what they imagine in words; individuals with mobility challenges can control their environment—lights, music, reminders—just by speaking naturally; and caregivers are finding AI to be a valuable support in reducing stress while improving personalized care. Far from replacing human connection, these tools are designed to enhance it, giving people more opportunities for creativity, memory support, and meaningful engagement. The session will offer both a glimpse into today's AI applications and a hopeful vision of how these innovations can help us all live better, longer, and more connected lives.

We will also discuss a little about how such assistants are being made safer with policy discussions and company specific guardrails.

Reshmi Ghosh (pictured below) is a Senior Applied Scientist and researcher at Microsoft's Copilot and Search team, driving the effort to make AI agents safer. She has a breadth of experience of building products from scratch with conventional machine learning and Generative AI models. Most recently, she is also teaching Generative AI basics to college graduates and professional continuing education, and has been a advocate to help women break into STEM careers. Reshmi is an active member on the IEEE Boston Executive Committee and committees.

Directions:
Newbury Court has two entrances; one at 80 Deaconess Rd and the other at 100 Newbury Court. The 80 Deaconess Rd entrance is immediately after the Emerson Hospital driveway. Please ignore that entrance and continue on down the road ("Old Road to Nine Acre Corner") until you see the second Newbury Court entrance and take that one. Drive up to the little traffic circle at the entrance and immediately after that is visitor parking. If this area is full, please park along the right side of the driveway heading back to the road. If anyone runs into difficulty, park temporarily at the traffic circle , run in, and ask the concierge for guidance as to where to park.

Please check in at the Concierge desk, then proceed down the hall to the Morrison Theatre.

Boston, Guatemala, Panama, and Peru Chapters of the IEEE Computer Society, Boston IEEE Engineering in Medicine and Biology Society (EMBS), New Jersey Coast and North Florida Sections of IEEE and GBC/ACM - 7:00 PM, Thursday, September 25

Learning, Engineering, & Targeting Cell States in Cancer

Time: 7:00 PM, Thursday, September 25

Location: 32-G449 (Kiva) - MIT Stata Center, 32 Vassar Street, Cambridge,MA and online via Zoom
Speaker: Ava Amini, Microsoft Research

Event Registration here. *Please register in advance for this seminar even if you plan to attend in person. After registering, you will receive a confirmation email containing information about joining the webinar.*

Indicate on the registration form if you plan to attend in person. This will help us determine whether the room is close to reaching capacity. We plan to serve light refreshments (probably pizza) before the talk starting at around 6:30 pm. Letting us know you will come in person will help us determine how much pizza to order.

We may make some auxiliary material such as slides and access to the recording available after the seminar to people who have registered.

Cancer is often treated using a reductionist approach: distilled to an individual subtype, mutation, or phenotype. But fundamentally, cancers are complex ecosystems that necessitate systems-level understanding and intervention. Addressing this problem is equal parts biology and computer science. In Project Ex Vivo, a joint cancer research collaboration between Microsoft Research and the Broad Institute, we are envisioning a new, constructionist paradigm for precision oncology, one powered by the bottom-up integration of computation and experimentation to understand the complexity of cell state ecosystems in cancer. In this talk I will share our recent efforts to build AI models to better define, model, and therapeutically target cell states in cancer.

Ava Amini (pictured right) is a Principal Researcher at Microsoft Research in Cambridge, MA. Her research focuses on developing new AI methods to understand and design biology, with the ultimate aim of realizing precision biomedicines that improve human health. She is a co-lead of Ex Vivo , a collaborative effort between Microsoft and the Broad Institute, that is focused on defining, engineering, and targeting cell states in cancer.

In addition to research, Ava is passionate about AI education and outreach — she is a lead organizer and instructor for MIT Introduction to Deep Learning , an in-person and global course on the fundamentals of deep learning.

Ava completed her PhD in Biophysics at Harvard University and the Massachusetts Institute of Technology (MIT), where she was advised by Sangeeta Bhatia at the Koch Institute for Integrative Cancer Research and supported by the NSF Graduate Research Fellowship. Ava received her Bachelor of Science in Computer Science and Molecular Biology from MIT.

Directions: Please use the main entrance to the Stata Center at 32 Vassar Street (the entrance closest to Main Street) as those doors will be unlocked. Upon entering, proceed to the elevators which will be on the right after passing a large set of stairs and a MITAC kiosk. Take the elevator to the 4th floor and turn right, following the hall to an open area; 32-G449 will be on the left. Location of Stata on campus map.

Partner/Exhibitor Prospectus

2026 IEEE International Phased Array Symposium

ARRAY 2026

BOSTON MASSACHUSETTS

October 19 - 22, 2026

www.ieee-array.org

IEEE

Digital Signal Processing (DSP) for Software Radio

Dates & Times: **Live Workshops: 6 - 7:30PM EST; Thursdays, October 23, November 6, 13, 20, December 4 and 11; First Video Release and Orientation, 6 - 6:30PM October 23, 2025. Additional videos released weekly in advance of that week's live session!**

Speaker: **Dan Boschen**

Location: **Zoom**

Attendees will have access to the recorded session and exercises for two months (until February 11, 2026) after the last live session ends!

This is a hands-on course providing pre-recorded lectures that students can watch on their own schedule and an unlimited number of times prior to live Q&A/Workshop sessions with the instructor. Ten 1.5 hour videos released 2 per week while the course is in session will be available for up to two months after the conclusion of the course.

Course Summary This course builds on the IEEE course "DSP for Wireless Communications" also taught by Dan Boschen, further detailing digital signal processing most applicable to practical real-world problems and applications in radio communication systems. Students need not have taken the prior course if they are familiar with fundamental DSP concepts such as the Laplace and Z transform and basic digital filter design principles.

This course brings together core DSP concepts to address signal processing challenges encountered in radios and modems for modern wireless communications. Specific areas covered include carrier and timing recovery, equalization, automatic gain control, and considerations to mitigate the effects of RF and channel distortions such as multipath, phase noise and amplitude/phase offsets.

Dan builds an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real-world applications for mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges, rather than a tutorial on implementations with DSP processors.

Now with Jupyter Notebooks! This long-running IEEE Course has been updated to include Jupyter Notebooks which incorporates graphics together with Python simulation code to provide a "take-it-with-you" interactive user experience. No knowledge of Python is required but the notebooks will provide a basic framework for proceeding with further signal processing development using that tools for those that have interest in doing so.

This course will not be teaching Python, but using it for demonstration. A more detailed course on Python itself is covered in a separate IEEE Course routinely taught by Dan titled "Python Applications for Digital Design and Signal Processing".

All set-up information for installation of all tools used will be provided prior to the start of class.

Target Audience: All engineers involved in or interested in signal processing for wireless communications. Students should have either taken the earlier course "DSP for Wireless Communications" or have been sufficiently exposed to basic signal processing concepts such as Fourier, Laplace, and Z-transforms, Digital filter (FIR/IIR) structures, and representation of complex

digital and analog signals in the time and frequency domains. Please contact Dan at boschen@loglin.com if you are uncertain about your background or if you would like more information on the course.

Benefits of Attending/ Goals of Course:
Attendees will gain a strong intuitive understanding of the practical and common signal processing implementations found in modern radio and modem architectures and be able to apply these concepts directly to communications system design.

Topics / Schedule:
Class 1: DSP Review, Radio Architectures, Digital Mapping, Pulse Shaping, Eye Diagrams

Class 2: ADC Receiver, CORDIC Rotator, Digital Down Converters, Numerically Controlled Oscillators

Class 3: Digital Control Loops; Output Power Control, Automatic Gain Control

Class 4: Digital Control Loops; Carrier and Timing Recovery, Sigma Delta Converters

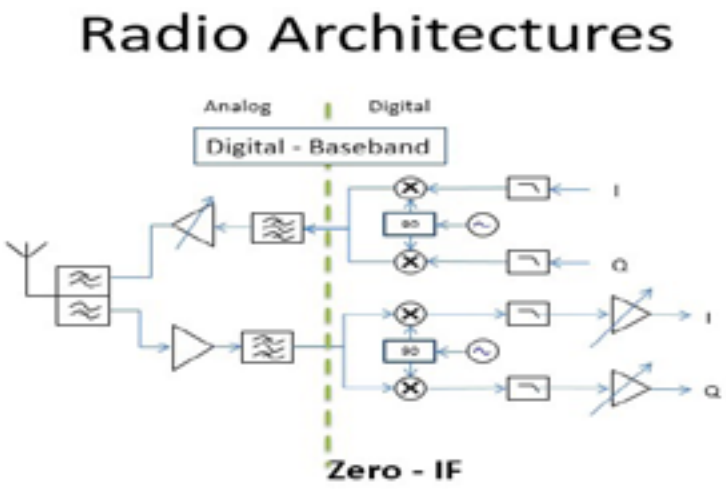
Class 5: RF Signal Impairments, Equalization and Compensation, Linear Feedback Shift Registers

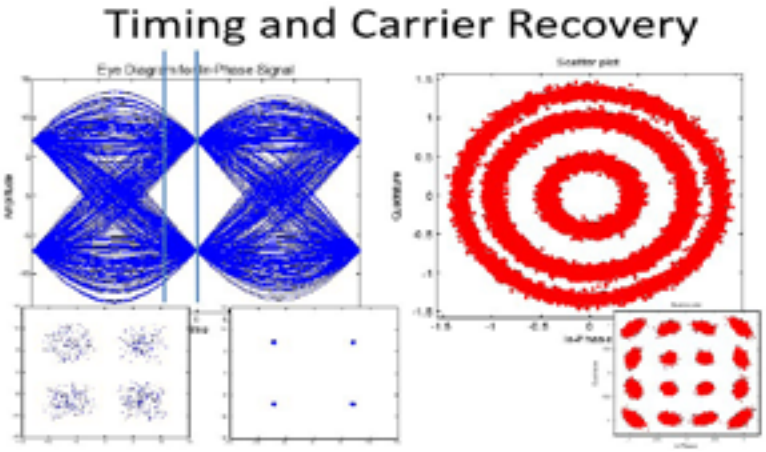
Speaker's Bio:
Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems and has taught courses on DSP to international audiences for over 15 years. Dan is a contributor to Signal Processing Stack Exchange https://dsp.stackexchange.com/, and is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

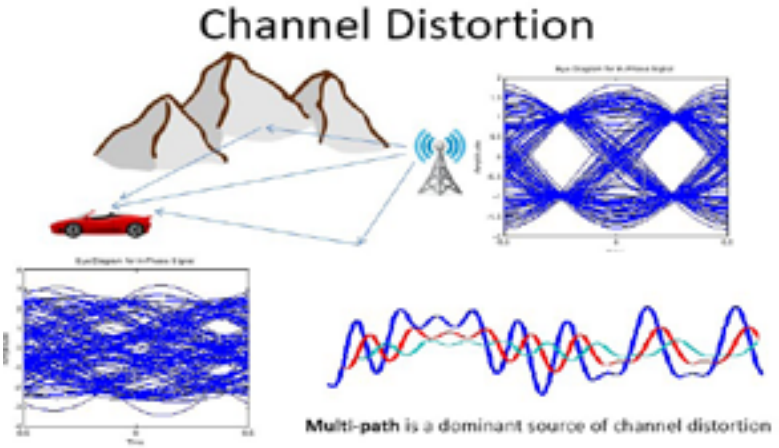
Decision (Run/Cancel) Date for this Course is Friday, October 17, 2025

Payment	By Oct 17	After Oct 17
IEEE Members	$190	$285
Non-members	$210	$315

For more background information, please view Dan's Linked-In page at: http://www.linkedin.com/in/dan-boschen







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May 12-14, 2026

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Notification of Acceptance: 2/12/26
Publication-Ready Submission: 4/21/26

More information and submissions:
IEEE-FASEH.org

Controlled fusion energy, inspired by the sun and stars, and space-based solar power (SBSP) represent two of the most promising clean and sustainable energy technologies of the future. The fast advancement in power electronics and microelectronics has sped up the development of laser and magnetic fusion; this has also led to reinvigorated interest in the large-scale solar energy harvesting via SBSP across the US, Europe, and Asia. Furthermore, growing energy-efficiency computing technologies and advanced innovations in AI tools accelerate the deployment of green energy systems.

The 2026 IEEE International Symposium on Fusion and Solar Energy Harvesting (FASEH) will bring together scientists, engineers, and practitioners from academia, industry, and government to share advances in fusion energy systems and large-scale solar energy collection in space, as well as the AI applications for energy. The symposium acronym, “FASEH” is pronounced “Phasor”, echoing the term commonly used in science and engineering, to represent the sinusoidal waveforms of physical quantities in steady-state systems.

FASEH Technical Tracks Include:

- Power Electronics for Energy Systems
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- Space-Based Solar Power Systems
- Fusion Power Engineering
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- Plasma Related Energy Technologies
- Environmental Impacts of Fusion and Solar Systems and AI Tools
- Social and Educational Implications of Energy Technologies

Submission Guidelines

Details will be posted on the symposium website at: https://ieee-faseh.org

Symposium and Technical Program Chair: Min-Chang Lee

Technical Program Co-Chair: Marcel Gaudreau

Local Symposium Co-Chair: Len Long
Local Symposium Co-Chair: Maira Marques Samary

https://ieee-faseh.org

2026 IEEE FASEH SYMPOSIUM

Deadline: 15 September

Every year, IEEE-USA Awards are given to recognize professionalism, technical achievement, and literary contributions to public awareness and understanding of the engineering profession in the United States.

PROFESSIONALISM AWARDS

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To honor members of the engineering profession for long-term dedicated effort and outstanding accomplishments in advancing the aims of IEEE professional activities in the United States.

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To honor individuals not currently in the practice of engineering for contributions to furthering the professional goals of IEEE in the United States.

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To honor members who have made exemplary contributions toward achieving the aims of professional activities in the United States.

The IEEE-USA John Meredith Professional Service Award

To recognize key individuals for outstanding IEEE-USA volunteer efforts and contributions. Maximum of one award presented per year.

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To honor pairs of K-12 educators and engineers that, through their joint collaboration, provide learning experiences to precollege students, support the education and curriculum requirements of their institution, promote and increase the math, science and engineering awareness of student participants, and/or support the educational goals of the IEEE and IEEE-USA.

IEEE-USA Entrepreneur Achievement Award for Leadership in Entrepreneurial Spirit

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IEEE-USA Jim Watson Student Professional Awareness Achievement Award

To recognize key individuals for their contributions to Student-Professional Awareness Activities in the United States.

LITERARY AWARD

Award for Distinguished Literary Contributions Furthering Public Understanding and Advancement of the Engineering Profession

To recognize outstanding journalistic or other efforts that contribute to the enhancement and expansion of the public understanding andthe advancement of the engineering profession in the United States.

TECHNICAL ACHIEVEMENT AWARD

Harry Diamond Memorial Award

To honor individuals for distinguished technical contributions in the field of electrotechnology while in U.S. Government Service.

ieeeusa.org/awards

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IEEE Boston Section

IEEE Strategic Plan

2025-2030

OUR MISSION

We foster technological innovation and excellence for the benefit of humanity.

OUR VISION

We will be essential to the global technical community and to technical professionals everywhere, and be universally recognized for the contributions of technology and of technical professionals in improving global conditions.

CORE VALUES

- Growth & Nurturing
- Trust
- Partnership
- Integrity in Action
- Global Community Building
- Service to Humanity

OUR GOALS

Advance science and technology as a leading trusted source of information for research, development, standards, and public policy

Drive technological innovation while promoting scientific integrity and the ethical development and use of technology

Provide opportunities for technology-related interdisciplinary collaboration, research, and knowledge sharing across industry, academia, and government

Inspire intellectual curiosity and support discovery and invention to engage the next generation of technology innovators

Expand public awareness of the significant role that engineering, science, and technology play across the globe

Empower technology professionals in their careers through ongoing education, mentoring, networking, and lifelong engagement

IEEE will foster a collaborative environment that is open, inclusive, and free of bias and will continue to sustain the strength, reach, and vitality of our organization for future generations.

www.ieee.org/strategic-plan

Approved by the IEEE Board of Directors, November 2024

IEEE

Advancing Technology for Humanity

IEEE Boston Section Volunteers Wanted!

Are you passionate about technology and eager to contribute to the advancement of your field? The IEEE Boston Section is excited to announce a call for volunteers to join our dynamic team of professionals and enthusiasts. By becoming a volunteer, you'll have the opportunity to collaborate with like-minded individuals, develop new skills, and make a meaningful impact on the local technology community.

About IEEE Boston Section:

The IEEE Boston Section is a thriving community of engineers, researchers, students, and industry professionals dedicated to promoting technological innovation and knowledge sharing. Our section hosts a variety of events, workshops, seminars, and conferences throughout the year, providing members with opportunities to learn, network, and stay updated on the latest developments in their fields.

Volunteer Opportunities:

We are currently seeking volunteers to help on the following committees:

The Fellow and Awards Committee - activities include recommending qualified members of the Section for advancement to Fellow grade and for receipt of the various IEEE (IEEE/Region/MGA/Section) awards. Identifying and building a database of the various IEEE awards available for nomination and searching out qualified candidates, for preparing the necessary written recommendations, and for assembling all required supporting documentation and submit its recommendations directly to the appropriate IEEE body.
Time Commitment: Meets 4 times a year for 1 – 2 hours per meeting (virtual or in person)

Local Conferences Committee - activities include identifying timely topical areas for conference development. Identify champions of these conferences to run the identified conference organizing committees. The section local conference committee is not charged with organizing and executing individual conferences.
Time Commitment: Meets 4 times per year 1 – 2 hours per meeting (virtual or in person)

Professional Development & Education Committee - activities include identifying topics, speakers, and/or organizers for appropriate technical lecture series or seminars. The subject matter should be timely, of interest to a large segment of the membership, and well organized with regard to speakers and written subject matter.
Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

The Membership Development Committee - activities include actively promoting membership in the IEEE and shall encourage members to advance to the highest grade of membership for which they are qualified. To these ends this committee shall include wide representation within the Section territory, shall maintain lists of prospects and members qualified for advancement, and shall provide information and assistance to preparing applications.
Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Student Activities Committee - activities include attracting a broad and diverse group of undergraduate and graduate students to IEEE and to engage them in activities that promote their own professional development as well as the ongoing growth of IEEE. The Student Activities Committee shall include among its members the IEEE Counselors at the universities, colleges, and technical institutes that lie within the Section territory. It shall be responsible for liaison with the Student Branches at these institutions and advise the Executive Committee on all other matters affecting the Student Members of the Section.
Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Young Professionals Affinity Group - activities include organizing programs, and initiatives aimed to address the needs of early-career professionals pursuing technology-related careers in engineering, business, management, marketing, and law. This committee is committed to helping young professionals evaluate their career goals, polish their professional image, and create the building blocks of a lifelong and diverse professional network.
Time Commitment: meets 4 times per year, 1 – 2 hours per meeting (virtual or in person)

Benefits of Volunteering:

Volunteering with IEEE Boston Section offers numerous benefits, including:

- Networking opportunities with professionals in your field.
- Skill development and enhancement through hands-on experience.
- Contribution to the local technology community and its growth.
- Access to cutting-edge information and discussions.

How to Get Involved:

If you're enthusiastic about technology and want to make a difference, we invite you to join us as a volunteer. To express your interest and learn more about specific roles, please visit our website and fill out the volunteer application form. Our team will get in touch with you to discuss opportunities that align with your interests and skills.

Thank you for considering this opportunity to contribute to the IEEE Boston Section. Your dedication and passion are what drive the success of our community and its impact on the world of technology.

Volunteer Here!