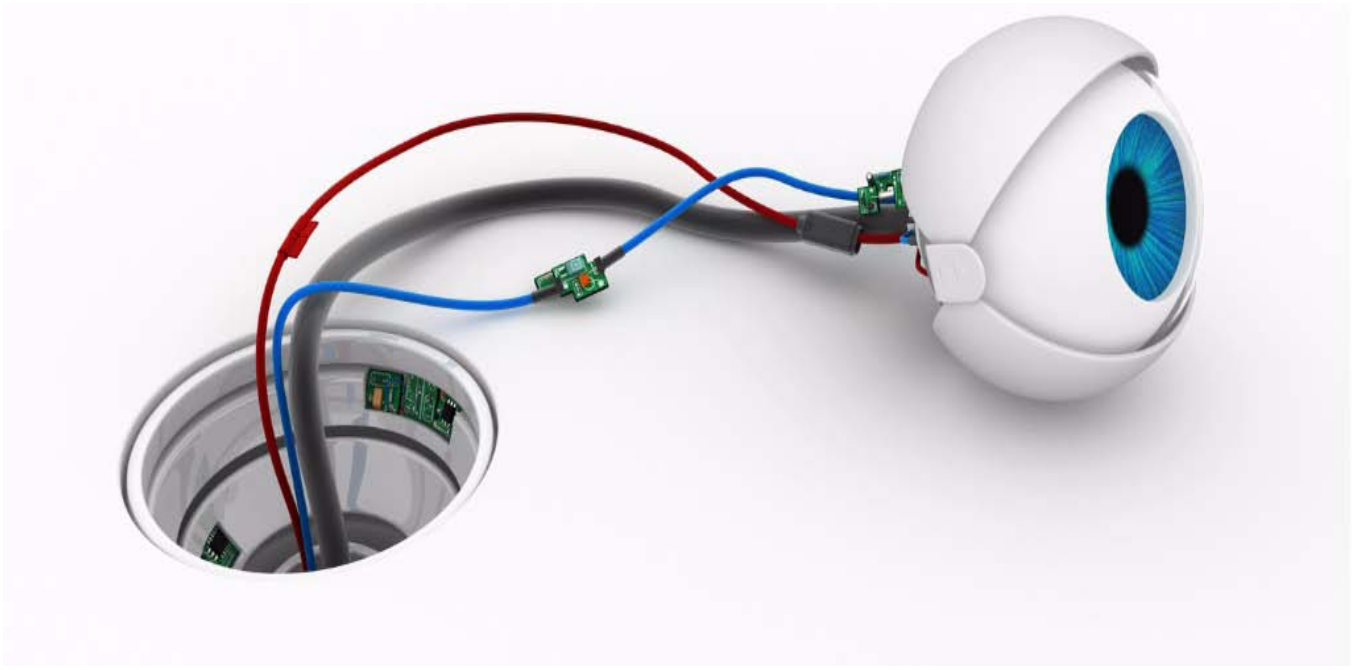
BOSTON

THE REFLECTOR

ISSUE #8
AUGUST 2021



IEEE
Advancing Technology for Humanity

TABLE OF CONTENTS

Human Assisted Artificial Intelligence

by Karen Panetta, Reflector Editor

While the country continues to struggle convincing people it is safe and smart to get vaccinated against Covid-19 despite emergency authorization and advocacy from the U.S. Federal Drug Administration (FDA), other growing numbers of people are willing to jump in with both feet in when it comes to trusting their lives to Artificial Intelligence (AI), which has no standards or organizational oversight. At this time, only "guidelines" from the U.S. Federal Trade Commission (FTC) exist for AI.

I will take you through an example of how even impactful applications of AI really still need a human assistant to ensure trustworthy, explainable, and unbiased decision making.

Using AI for automating manufacturing and improving our work streams, such as providing robust CMMS (computerized maintenance management systems) is an excellent application for AI. CMMS is a proactive methodology to keep systems running and to optimize maintenance operations. Alternatively, if businesses and institutions don't invest in being smart about maintenance and choose only to take action after a system fails, it ultimately impacts operations, and customer service. Especially, if the components needed for repair are not readily available.

CMMS systems utilize sensors and other Internet of Things (IoT) devices and leverage on cloud services and can track equipment assets, sense whether device performance is degrading, maintain the history of repair times and help us determine whether it is time to invest in replacing/upgrading versus investing in more repairs. AI can be used to look at this plethora of data and help make inferences that could save money, anticipate risk factors and build risk mitigation plans.

So far in this example, it appears that humans can't be personally adversely affected by the AI used in this kind of application, but consider a scenario when a relationship appears between the number of times a repair was done on a device that repeatedly failed and the person who performed that repair?

Perhaps this means the repair person needs more training or does it simply mean the device has too many faults and should be replaced? This is when the AI needs to ask a human for help and the human needs to be smart about interpreting what the data means.

Whenever AI makes a decision on a human's livelihood or is used to evaluate an individual's competency, we need to hit the big red STOP button and understand how the AI is making decisions and what it means. There have been many examples of companies using AI to evaluate human job performance, which resulted in the subsequent dismissal or poor evaluations of employees. Lending institutions using AI have encountered algorithms that have unfairly eliminated underrepresented groups of individuals from qualifying for loans.

This kind of blind faith in computer generated decisions gives me a flashback to high school when they gave us career assessment tests to match us to a future vocation. I was at the top of my class and my best friend, a male had scored slightly lower than I did in math and science. We were both expecting the outputs of our career assessments to be similar. How wrong I was!

His assessment said he could become an engineer, scientist, or politician. The results of my assessment, said I could be a cook, or sell cosmetics.

True fact: I stink at cooking. I never could cook and I still can't. Furthermore, it would be cruel and unjust for anyone to be subjected to eating my cooking.

When I complained to the guidance counselor, he reminded me that the results had to be correct, because this was a "computer generated" result and therefore it had to be accurate. Thankfully, I have always been a rebel and didn't care what any computer program output said, I ignored that assessment and went on to become an engineer.

AI has so much potential, but it has a long way to go before it can be considered a standalone replacement for human decision making that is trustworthy and unbiased. In a recent IEEE/IEEE-HKN webinar, Dr. Manuela M. Veloso, Head of J.P. Morgan AI Research discussed human assisted AI as the bridge in the quest to help create more robust trustworthy AI. Including the human in the loop while the AI is exploring the data and asking the human for help is a new paradigm that many have leaped over to expedite the use of AI. We need to demystify AI as a building block and have a way for the AI to declare it needs help from its human partner.

Finally, we need to question results and help lawmakers develop standards to prevent blind trust in computer generated outputs that could have disastrous impacts of turning aspiring engineers into horrible cooks.

IEEE Boston Section - 2020 Distinguished Service Award Recipient

The 2020 recipient of the IEEE Boston Section's "Distinguished Service Award" (DSA) is Dr. Albert Reuther. The DSA is awarded to an IEEE Boston Section volunteer who is active in our section, chapter, or conference efforts. Specifically, the DSA honors an IEEE Boston Section member who has made exceptional and distinguished contributions to the IEEE Boston Section. Dr. Reuther received the award for his extraordinary efforts on the section's High Performance Extreme Computing Conference (HPEC) Committee in 2020. His citation reads, "For Continuous and dedicated support of the section's HPEC Conference and extraordinary effort virtualizing HPEC 2020 in response to the global pandemic".

Dr. Albert Reuther is Senior Technical Staff Member in the MIT Lincoln Laboratory Supercomputing Center (LLSC). He brought supercomputing to Lincoln Laboratory through the establishment of LLGrid, founded the LLSC, and leads the LLSC Computational Science and Engineering team. He developed the gridMatlab high-performance computing (HPC) cluster toolbox for pMatlab and is the computer system architect of the MIT Supercloud and numerous interactive supercomputing clusters based on Supercloud, including those in the LLSC. He is the technical chair of the IEEE High Performance Extreme Computing Conference and has organized numerous workshops on interactive HPC, cloud HPC, economics of HPC, and HPC security. His areas of research include interactive HPC; computer architectures for machine learning, graph analytics, and parallel signal processing; and computational engineering. Dr. Reuther earned PhD degree in electrical and computer engineering in 2000 from Purdue University and an MBA degree from the Collège des Ingénieurs in Paris, France, and Stuttgart, Germany in 2001.

In addition to the DSA, the section has two other awards for which qualified section members can also be nominated. They are, "Student Achievement Award" - to recognize a college student who demonstrates the potential to become a distinguished leader and outstanding contributor in an IEEE field of interest, and the, "Distinguished Member Award" which recognizes outstanding long-term service (10-years or more) to the Boston Section of the IEEE and significant contributions in an IEEE field of interest.

See the IEEE Boston section website, ieeeboston.org for more details on the IEEE Boston Section awards.

IEEE Boston Section Online Courses:

(Students have 180 day access to all online, self-paced courses)

Electronic Reliability Tutorial Series - (Fall 2020) (NEW!!!)

Full course description and registration at ,
http://ieeeboston.org/electronic-reliability/

Verilog101:Verilog Foundations

Full course description and registration at ,
http://ieeeboston.org/verilog-101-verilog-foundations-online-course/

System Verilog 101: Design Constructs

Full course description and registration at ,
http://ieeeboston.org/systemverilog-101-sv101-design-constructs-online-course/

System Verilog 102: Verification Constructs

Full course description and registration at ,
http://ieeeboston.org/systemverilog-102-sv102-verification-constructs-online-course/

High Performance Project Management

Full course description and registration at ,
http://ieeeboston.org/high-performance-project-management-online-course/

Introduction to Embedded Linux Part I

Full course description and registration at ,
http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/

Embedded Linux Optimization - Tools and Techniques

Full course description and registration at ,
http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/

Embedded Linux Board Support Packages and Device Drivers

Full course description and registration at ,
http://ieeeboston.org/embedded-linux-bsps-device-drivers-line-course/

Software Development for Medical Device Manufacturers

Full course description and registration at ,
http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/

Fundamental Mathematics Concepts Relating to Electromagnetics

Full course description and registration at ,
http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/

Reliability Engineering for the Business World

Full course description and registration at ,
http://ieeeboston.org/reliability-engineering-business-world-line-course/

Design Thinking for Today's Technical Work

http://ieeeboston.org/design-thinking-technical-work-line-course/

Fundamentals of Real-Time Operating Systems

http://ieeeboston.org/fundamentals-of-real-time-operating-systems-rt201-on-line-course/

Summer 2021 IEEE Hackathon – On-Line

Applications of AI in Remote Sensing

Sponsored by:

IEEE GRSS Boston Chapter
IEEE GRSS Brazil Chapter
IEEE GRSS Italy Chapter
IEEE GRSS Spain Chapter

MIT LL

PROJECT OWL

WESTLIGHT.AI

Dates: Start: Saturday **July 31** at 11:00AM – End: Monday **August 9** at 11:00AM, 2021

Eligible students: undergraduate students from universities in the USA, Brazil, Italy and Spain

Team composition: 2-4 students. Majors required: computer science + geoscience or Remote Sensing or relevant.

Platforms: Registration: Eventbrite - Teams/Submission: DevPost Registration https://ieee-grss-boston-hackathon.devpost.com – Communications: Slack. Workshop and Q&A on Zoom on July 31 at 11:00AM EDT

Challenge: Use Geiger-Mode LiDAR data of an eastern region of Puerto Rico (after hurricane Maria in 2018) provided by MIT LL and write a code using AI to find and label on an image: a. Damaged roads and buildings, b. Areas with high risk of landslide; c. Areas that are isolated (with no roads connection available in/out); d. areas in need of communication networks; e. Crops and relevant damage to agriculture. Pre-hurricane data available by USGS at; https://www.usgs.gov/news/usgs-3dep-lidar-point-cloud-now-available-amazon-public-dataset

Scoring guidelines: Approach: +40%, Results: +30%, Teamwork +20%, Team Diversity +10%

Prizes: 1st place: $1,200. 2nd place: 1,000. 3rd place: $500

Call for Articles

Now that the Reflector is all electronic, we are expanding the content of the publication. One of the new features we will be adding are technical, professional development, and general interest articles to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development or general interest articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional/interest articles will be reviewed by the Publications Committee for suitability.The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to;
ieeebostonsection@gmail.com

IEEE Video Series

A collaborative discussion panel featuring esteemed members from the Institute of Electrical and Electronics Engineers has convened in 2021 to produce educational video presentations that embrace IEEE's mission of advancing technology for humanity.

Among the programs they've produced include "Electric Vehicles: Fun Saving Our Planet", "Greener Power For More Electric Vehicles", "Overcoming Nuclear Fears To Achieve Net Zero CO2 By 2050" and "Achieving a Net Zero Carbon Future", and "Green Energy's Economic Progress". Projects currently in production include the expansive topic of futurology, with a focus on increasing the efficiency and transformation of aging electrical power generating stations and infrastructure to accommodate nuclear power; reviewing the viability of alternative energy (such as geothermal, wind and solar); and focusing on 'cleaner' fossil fuels that are more environmentally-friendly to slow the rate of climate change.

These shows are produced and directed by Lennart E. Long, IEEE Senior Life Member from the Executive Committee and Past Chair of the Boston Section; Dr. Paul H Carr, BS, MS, MIT; PhD Brandeis U, IEEE Life Fellow; Dr. Ted Kochanski, SB (MIT), Ph.D (U.Texas, Austin), IEEE Global Education for Microelectronic Systems and former Boston Section Chair; and Dr. Ken Laker, B.E. (Manhattan College), M.S. and Ph.D. (New York University), IEEE Life Fellow and past President of IEEE.

The panel is moderated by five-time Boston/New England Emmy Award-winner and television personality and star of "The Folklorist," John Horrigan.

These video programs with presentations and discussions can be accessed at the IEEE Boston Section video portal at https://vimeo.com/user18608275.

We are looking for any IEEE members that would like to appear on the program in the role of presenter or discussion expert. Simply reach out to Robert Alongi at the Boston Section at, ieeebostonsection@gmail.com.

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.
If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- **Honoraria can be considered for course lecturers**
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

MIT URTC 2021 10/8 - 10/10, 2021

UNDERGRADUATE RESEARCH TECHNOLOGY CONFERENCE

IN PARTNERSHIP WITH IEEE MIT

Passionate about research in technology? Looking to share your work with peers and professionals?

Join us at MIT URTC 2021!

PAPERS

EARLY SUBMISSION DEADLINE	JULY 11, 2021
EARLY NOTIFICATION OF ACCEPTANCE	JULY 31, 2021
REGULAR SUBMISSION DEADLINE	JULY 31, 2021
REGULAR NOTIFICATION OF ACCEPTANCE	AUGUST 21, 2021

POSTERS & LIGHTNING TALKS

SUBMISSION DEADLINE	AUGUST 29, 2021
NOTIFICATION OF ACCEPTANCE	SEPTEMBER 5, 2021

CONFERENCE DATES

10/8 - 10/10, 2021

Technical Tracks

1. **Biological and Biomedical Engineering (BioEECS)**
2. **Circuits, Materials, and Nanotechnologies**
3. **Computer Systems, Theoretical Computer Science and Mathematics**
4. **Machine Learning / Artificial Intelligence (AI)**
5. **Robotics and Controls**
6. **Security and Communications**
7. **Space Application and Technologies**
8. **Innovation Research**

Submission Site:
https://cmt3.research.microsoft.com/URTC2021

5G The Best Channel Codes:

Polar Codes with MATLAB Applications

Web-based Course with live Instructor!

Times & Dates: 10 – 11AM ET, September 14, 16, 21, 23, 28, 30, October 5, 7, 12, 14
Speaker: Orhan Gazi, Cankaya University, Ankara-Turkey
Course Format: Live Webinar, 10, one hour, sessions

Introduction: Forward error correction is a vital process in communication systems. The last channel codes discovered in the research world are the "polar codes" which are adapted to be used in 5G standard. The construction and decoding of polar codes are quite different from the construction and decoding of classical channel nodes. Polar codes are the only codes constructed in a non-trivial manner. The discovery of polar codes can be considered as a breakthrough in coding society. It is clear that future channel codes will follow the logic of polar codes. For this reason, it is critical to learn the encoding and decoding philosophy of the polar codes which is the state of art of the coding world.

Outline of the topics to be covered:

- Entropy and Mutual Information
- Philosophy of Polar Codes
- Generator Matrices of Polar Codes
- Polar Encoder Structures
- Recursive Structures for Polar Encoders
- Channel Splitting and Concept of Channel Polarization
- Split Channels
- Calculation of Split Channel Capacities
- Polar Decoding
- Polar Decoding for Noiseless Transmission
- Polar Decoding Formulas for Kernel Structure for noisy Transmission
- Successive Cancelation Decoding of Polar Codes
- Belief Propagation Decoding of Polar Codes
- Polar Encoders and Decoders in 5G New Radio (NR) and Future Channel Codes

Target Audience: Electronic and Communication Engineers, electronic engineers, computer engineers, engineers working in communication industry

Benefits of Attending Course:
1) The participant will have an idea about the state of art polar codes.
2) Polar codes are used in 5G standard; the participant can comprehend the polar code used in 5G standard.
3) The participant will learn successive cancelation decoding of polar codes.

Speaker Bio: Prof. Orhan Gazi is the author of the book "Polar Codes. A Non-Trivial Approach to Channel Coding" which can be reached from https://www.springer.com/gp/book/9789811307362

The book is selected by IEEE COMSOC as one of the best readings in polar codes, https://www.comsoc.org/publications/best-readings/polar-coding

Prof. Orhan Gazi is the sole author of 10 books written in electrical engineering subjects. Apart from the polar code book, he is the single author of the books "Information Theory for Electrical Engineers" https://www.springer.com/gp/book/9789811084317 and "Forward Error Correction via Channel Coding" https://www.springer.com/gp/book/9783030333799. The research area of Prof. Orhan Gazi involves "channel coding", and "digital communication subjects". Recently, he focuses on over capacity data transmission using polar codes. He is also interested in practical applications of communication systems involving FPGA devices. He is delivering courses with titles "VHDL circuit design", "interface design using VHDL for FPGA devices" and "system on chip design".

Materials to be included: Lecture slides will be provided.

Decision (Run/Cancel) Date for this Course is Wednesday, September 8, 2021

IEEE Members	**$250**
Non-members	**$300**

https://ieeeboston.org/event/5g-the-best-channel-codes/?instance_id=3068

Electronic Reliability Tutorial Series -

Fall 2021 Edition - Electronic Reliability Series 3:

How to use Simulation and Modeling techniques to Improve Reliability

Three new, LIVE WEBINAR courses!

Times & Dates: **Each session is two hours and starts at 11:00AM ET, Oct 7, 14, 21**

Speakers: Dr. Nathan Blattau, Michael Blattau, Nick Kirsch, Dr. Gil Sharon & Tyler Ferris, Ansys

Electronics perform critical functions in every major industry vertical, whether in automotive, aerospace, consumer, medical or industrial segments. With the advent of newer technologies (both at the component and material levels), shrinkage of feature sizes, more stringent environments and sophisticated power requirements, electronics face increasing reliability risks. Supply chain trends have changed over the years from a vertically integrated model to a more geographically diverse supply chain. All these trends have increased reliability risks for companies. However, the cost of reliability assurance activities is often a fraction of the cost of failure, with compounding benefits from conducting these activities early in the design process.

This set of three tutorials will highlight how simulation and modeling can be used to optimize the design, gain assurance of passing qualification tests, and mitigate reliability issues early in the design process.

Session 1) Solder Alloys and Modeling Solder Reliability for Electronic Assemblies

Abstract: Solder provides the structural and electrical connection between a printed wiring board (PWB) and electrical components. Solder is the most common material used for assembling electronics. However, while most materials only experience elastic deformation during use, solder is also one of the few structural materials that is expected to also undergo significant inelastic deformation during its lifetime.

Both elastic and inelastic deformation damages solder, causing the solder joints to fail, and consequentially the printed circuit assembly to fail. Predicting when the solder joint fails is critical when using solder in harsh use environments. These harsh environments have loads that can come in several forms (i.e., drop/shock, vibration, temperature cycling).

While vibration causes high cycle fatigue of solder, most solder fatigue failures in electronics are thermo-mechanically driven due to temperature cycling which causes significant deformations and stresses due to coefficient of thermal expansion (CTE) mismatches between the PWB and components. To predict solder failure, a damage model must be used that relates deformation of the solder to cycles to printed circuit board assembly failure.

In this tutorial, we will discuss material characterization of various solder alloys, predictive solder fatigue damage models using a physics-of-failure approach (PoF) for printed circuit board assemblies and how to develop damage models using simulation and test***ing.***

Target audience: Engineers involved in the design, simulation and modeling, manufacturing and/or reliability of complex printed circuit board assemblies.

Benefits of attending

- Learn about different solder alloys and their failure mechanisms
- Characterizing solder material properties for simulation and modeling
- Methods for predicting reliability of electronic assemblies

Dr. Nathan Blattau, Distinguished Engineer at Ansys, has been involved in the simulation and reliability of electronic equipment for over twenty years. Prior to joining Ansys, Dr. Blattau was the Vice President and Chief Scientist of DfR Solutions. He holds two patents and has authored over 20 papers and has presented on a wide variety of reliability issues within the electronics industry. His specialties include best practices in design for reliability, robustness of Pb-free, failure analysis, accelerated test plan development, nonlinear finite element analysis, and solder joint reliability. Dr. Blattau holds a Ph.D. in Mechanical Engineering, an M.S. in Mechanical Engineering, and a B.S. in Civil Engineering from the University of Maryland

Session 2) Printed Circuit Board Level Reliability Testing – Leveraging Testing, Failure Analysis, and Simulation to Improve Reliability

Abstract: Board Level Reliability Testing (BLRT) encompasses a range of environmental stress tests that evaluate the robustness of a semiconductor package once soldered to a printed circuit board (PCB). Solder joint reliability under thermal and mechanical loads has been the focus of BLRT programs, though increasingly other failure modes have also been identified for testing under these programs. While standards from organizations, such as JEDEC JEP150 and AEC Q104 (for automotive), provide guidance for BLRT testing, there is often ambiguity around test coupon design, test conditions, test duration, and failure criteria. This ambiguity can cause confusion, delay, and dissatisfaction up and down the supply chain.

Additionally, finite element modeling (FEM) is often underutilized in BLRT programs. Proactive simulation can be a helpful tool to design for reliability and improve overall BLRT robustness. This tutorial will cover tips for designing an appropriate BLRT program. This includes best practices in BLRT risk assessment, test coupon design, and experimental procedures. It will also review how to leverage simulation to improve BLRT design and performance.

Target audience: Engineers involved in the design, prototyping, qualification, or end use of new electronic package designs

Benefits of attending

- Learn about common failure modes and mechanisms of electronic package assemblies experienced and tested for in Printed Circuit Board Reliability Testing
- Learn about best practices for designing and conducting a board level reliability test program (BLRT)
- Learn how to use simulation to predict qualification test performance and reduce design cycles

Michael Blattau is a Senior Consulting Engineer at Ansys with expertise in mechanical packaging of electronics. Prior to working for Ansys he was a Design Engineering Supervisor for over a decade with an embedded computer manufacturer. Michael brings significant expertise in electronics enclosure design, PCB layout, and FEA simulation and has a M.S., Electronic Packaging.

Nick Kirsch (MBA, PMP) leads the modeling and simulation team for ANSYS Reliability Engineering Services. He has a 9-year background as a project manager and engineer working with US Government and private sector clients to improve product performance, resolve manufacturing problems, manage complex testing programs, and provide expert analysis and guidance at all stages of the product development process. At ANSYS, his work focuses on validating and improving the mechanical performance of electronics systems through testing and FEA reliability simulations.

Session 3) Simulation Techniques to Evaluate ELK Stress During Chip Attach Process and Mitigate Failures

Abstract: Electronic component manufacturing requires a technology to connect a silicon die to a circuit. A popular method to do so is to flip the die and solder it using C4 bumps to a substrate. The substrate is then finished into a component. A major concern for flip chip technology nsion of the silicon die (2-3 ppm/°C) and the substrate (8-15 ppm/°C). The stress in the extreme low-k layers (ELK Stress) causes a brittle fracture).

This workshop is a hands-on tutorial on completing a simulation for this failure mode. The tutorial includes example files, analysis settings and best-known methods. The workshop will rely on the use of Ansys Sherlock, Ansys Mechanical and Ansys SpaceClaim inside the Ansys Workbench environment.

Target audience: Flip chip component designers and integrators, assembly bumping designers and manufacturers, chip attach, packaging and assembly engineers

Benefits of attending

- How to prevent flip Chip packaging and assembly issues
- Prevent ELK cracking problems before design
- Using simulation techniques to drive design for manufacturing (DfM)

Dr. Sharon is a diverse industry expert with research specialties including mechanical reliability of electronic systems and characterization; embedded components failure analysis and particle beam accelerator mechanical fatigue; multidisciplinary reliability of complex electromechanical systems; characterization and modeling of material behavior; mechanical performance of flip chip packages; and Physics of Failure of electromechanical and MEMS systems. In addition to his responsibilities at ANSYS - DfR, Dr. Sharon serves as an adjunct faculty member at the University of Maryland.

Tyler Ferris is a Senior Consulting Engineer at Ansys and is an expert in the use of reliability physics, finite element analysis and hands-on laboratory failure analysis. Tyler has consulted with customers in the aerospace, automotive, industrial controls, data center industries and more, to evaluate system, PCBA and component-level failure risks and mitigation strategies.

- Benefits of attending
- How to prevent flip Chip packaging and assembly issues
- Prevent ELK cracking problems before design
- Using simulation techniques to drive design for manufacturing (DfM)

Decision (Run/Cancel) Date for this Course is One week prior to session

Each session is a separate registration

IEEE Members - $80

Non-members - $100

IEEE Boston Section Social Media Links:

Twitter: https://twitter.com/ieeeboston

Facebook: https://www.facebook.com/IEEEBoston

YouTube: https://www.youtube.com/user/IEEEBostonSection

LinkedIn: https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about

Introduction to Practical Neural Networks and Deep Learning (Part I)

Web-based Course with live Instructor!

Times & Dates: 9AM - 12:30PM ET, Saturday, September 18

Speaker: CL Kim

Course Format: Live Webinar, 3 hours of instruction!

Series Overview: From the book introduction: "Neural networks and deep learning currently provides the best solutions to many problems in image recognition, speech recognition, and natural language processing."

This Part 1 and the planned Part 2 (winter or spring 2022, to be confirmed) series of courses will teach many of the core concepts behind neural networks and deep learning.

More from the book introduction: Reference book: "Neural Networks and Deep Learning" by Michael Nielsen, http://neuralnetworks and deeplearning.com "We'll learn the core principles behind neural networks and deep learning by attacking a concrete problem: the problem of teaching a computer to recognize handwritten digits. …it can be solved pretty well using a simple neural network, with just a few tens of lines of code, and no special libraries."

"But you don't need to be a professional programmer."

The code provided is in Python, which even if you don't program in Python, should be easy to understand with just a little effort.

Benefits of attending the series:
* Learn the core principles behind neural networks and deep learning.
* See a simple Python program that solves a concrete problem: teaching a computer to recognize a handwritten digit.
* Improve the result through incorporating more and more core ideas about neural networks and deep learning.
* Understand the theory, with worked-out proofs of fundamental equations of backpropagation for those interested.
* Run straightforward Python demo code example.

The demo Python program (updated from version provided in the book) can be downloaded from the speaker's GitHub account. The demo program is run in a Docker container that runs on your Mac, Windows, or Linux personal computer; we plan to provide instructions on doing that in advance of the class.

(That would be one good reason to register early if you plan to attend, in order that you can receive the straightforward instructions and leave yourself with plenty of time to prepare the Git and Docker software that are widely used among software professionals.)

Course Background and Content: This is a live instructor-led introductory course on Neural Networks and Deep Learning. It is planned to be a two-part series of courses. The first course is complete by itself and covers a feedforward neural network (but not convolutional neural network in Part 1). It will be a pre-requisite for the planned Part 2 second course. The class material is mostly from the highly-regarded and free online book "Neural Networks and Deep Learning" by Michael Nielsen, plus additional material such as some proofs of fundamental equations not provided in the book.

Outline:
Introduction to Practical Neural Networks and Deep Learning (Part 1)
Feedforward Neural Networks.
* Simple (Python) Network to classify a handwritten digit
* Learning with Gradient Descent
* How the backpropagation algorithm works

* Improving the way neural networks learn:
** Cross-entropy cost function
** Softmax activation function and log-likelihood cost function
** Rectified Linear Unit
** Overfitting and Regularization:
*** L2 regularization
*** Dropout
*** Artificially expanding data set
*** Hyper-parameters

Pre-requisites: There is some heavier mathematics in learning the four fundamental equations behind backpropagation, so a basic familiarity with multivariable calculus and matrix algebra is expected, but nothing advanced is required. (The backpropagation equations can be also just accepted without bothering with the proofs since the provided Python code for the simple network just make use of the equations.) Basic familiarity with Python or similar computer language.

Speaker Background: CL Kim works in Software Engineering at CarGurus, Inc. He has graduate degrees in Business Administration and in Computer and Information Science from the University of Pennsylvania. He had previously taught for a few years the well-rated IEEE Boston Section class on introduction to the Android platform and API.

Decision (Run/Cancel) Date for this Course is Tuesday, September 14, 2021

IEEE Members	**$110**
Non-members	**$130**

https://ieeeboston.org/event/neuralnetworks/?instance_id=3049

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.
If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- **Honoraria can be considered for course lecturers**
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

Python Applications for Digital Design and Signal Processing

Dates & Times: **Thursday, November 11, 2021, videos released weekly 2x1.5 hours**
Live Workshops: 7:00 - 8:00PM ET; Tuesdays, November 16, 23, 30, December 7

Speaker: **Dan Boschen**

Location: **Zoom**

This is a hands-on course combining pre-recorded lectures with live Q&A and workshop sessions in the popular and powerful open-source Python programming language.

New Format with Pre-Recorded Videos: The course format has been updated to release pre-recorded video lectures that students can watch on their own schedule, and an unlimited number of times, prior to live Q&A workshop sessions on Zoom with the instructor. The videos will also be available to the students for viewing for up to two months after the conclusion of the course.

Overview: Dan provides simple, straight-forward navigation through the multiple configurations and options, providing a best-practices approach for quickly getting up to speed using Python for modelling and analysis for applications in signal processing and digital design verification. Students will be using the Anaconda distribution, which combines Python with the most popular data science applications, and Jupyter Notebooks for a rich, interactive experience.

The course begins with basic Python data structures and constructs, including key “Pythonic” concepts, followed by an overview and use of popular packages for scientific computing enabling rapid prototyping for system design.

During the course students will create example designs including a sigma delta converter and direct digital synthesizer both in floating point and fixed point. This will include considerations for cycle and bit accurate models useful for digital design verification (FPGA/ASIC), while bringing forward the signal processing tools for frequency and time domain analysis.

Jupyter Notebooks: This course makes extensive use of Jupyter Notebooks which combines running Python code with interactive plots and graphics for a rich user experience. Jupyter Notebooks is an open-source web-based application (that can be run locally) that allows users to create and share visually appealing documents containing code, graphics, visualizations and interactive plots. Students will be able to interact with the notebook contents and use “take-it-with-you” results for future applications in signal processing.

Target Audience: This course is targeted toward users with little to no prior experience in Python, however familiarity with other modern programming languages and an exposure to object-oriented constructs is very helpful. Students should be comfortable with basic signal processing concepts in the frequency and time domain. Familiarity with Matlab or Octave is not required, but the equivalent operations in Python using the NumPy package will be provided for those students that do currently use Matlab and/or Octave for signal processing applications.
Benefits of Attending / Goals of Course: Attendees will gain an overall appreciation of using Python and quickly get up to speed in best practice use of Python and related tools specific to modeling and simulation for signal processing analysis and design.

All set-up information for the installation of all tools will be provided before the start of class.

Topics / Schedule:

Pre-recorded lectures (3 hours each) will be distributed Friday prior to all Workshop dates. Workshop/ Q&A Sessions are 7pm-8pm on the dates listed below:

Tuesday, November 16

Topic 1: Intro to Jupyter Notebooks, the Spyder IDE and the course design examples. Core Python constructs.

Tuesday, November 23

Topic 2: Core Python constructs; iterators, functions, reading writing data files.

Tuesday, November 30

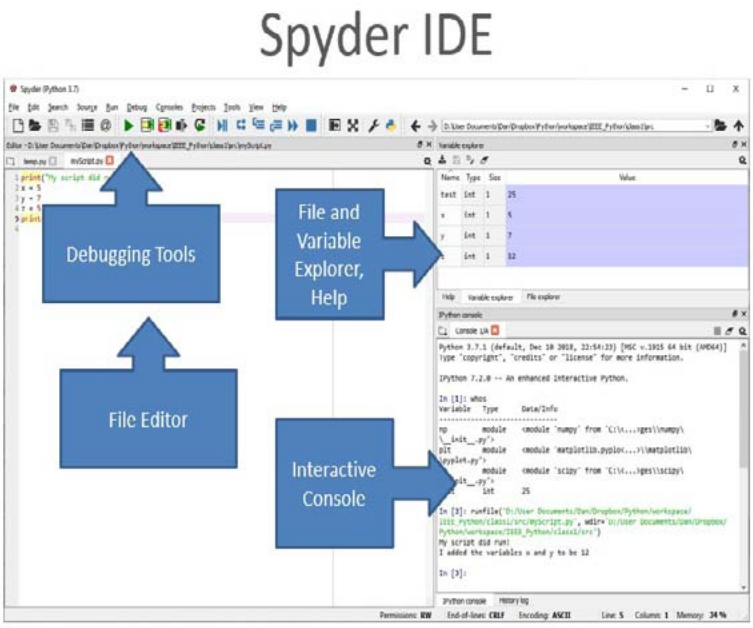
Topic 3: Signal processing simulation with popular packages including NumPy, SciPy, and Matplotlib.

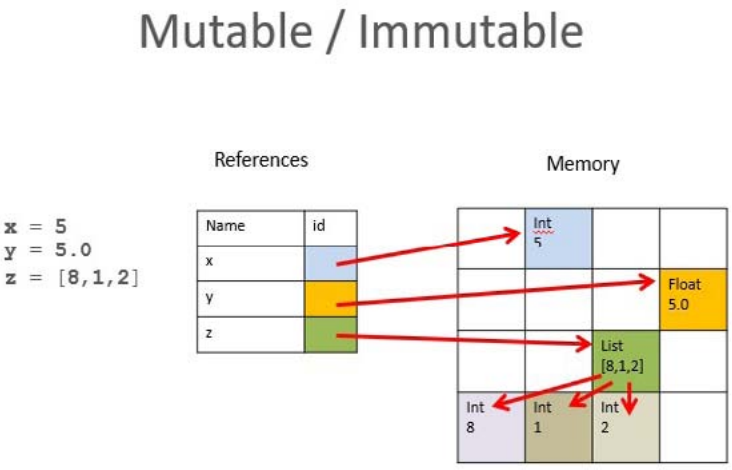
Tuesday, December 7

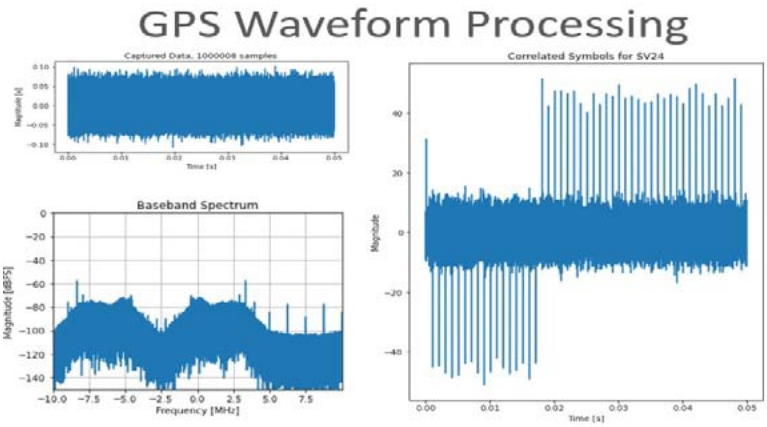
Topic 4: Bit/cycle accurate modelling and analysis using the design examples and simulation packages

Speaker's Bio: Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems and has taught courses on DSP to international audiences for over 15 years. Dan is a contributor to Signal Processing Stack Exchange https://dsp.stackexchange.com/, and is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page (https://www.linkedin.com/in/dan-boschen/)







Decision (Run/Cancel) Date for this Course is Thursday, November 4, 2021

IEEE Members	**$190**
Non-members	**$210**

https://ieeeboston.org/event/pythonapplications/?instance_id=3109

Digital Signal Processing (DSP) for Software Radio

Dates & Times: **Thursday, October 7, 2021, Videos released weekly 2x1.5 hours**
Live Workshops: 7:00 - 8:00PM ET; Tuesdays, October 12, 19, 26, November 2, 9

Speaker: **Dan Boschen**

Location: **Zoom**

New Format Combining Live Workshops with Pre-recorded Video

This is a hands-on course providing pre-recorded lectures that students can watch on their own schedule and an unlimited number of times prior to live Q&A/Workshop sessions with the instructor. Ten 1.5 hour videos released 2 per week while the course is in session will be available for up to two months after the conclusion of the course.

Course Summary This course builds on the IEEE course "DSP for Wireless Communications" also taught by Dan Boschen, further detailing digital signal processing most applicable to practical real-world problems and applications in radio communication systems. Students need not have taken the prior course if they are familiar with fundamental DSP concepts such as the Laplace and Z transform and basic digital filter design principles.

This course brings together core DSP concepts to address signal processing challenges encountered in radios and modems for modern wireless communications. Specific areas covered include carrier and timing recovery, equalization, automatic gain control, and considerations to mitigate the effects of RF and channel distortions such as multipath, phase noise and amplitude/phase offsets.

Dan builds an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real-world applications for mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges, rather than a tutorial on implementations with DSP processors.

Now with Jupyter Notebooks! This long-running IEEE Course has been updated to include Jupyter Notebooks which incorporates graphics together with Python simulation code to provide a "take-it-with-you" interactive user experience. No knowledge of Python is required but the notebooks will provide a basic framework for proceeding with further signal processing development using that tools for those that have interest in doing so.

This course will not be teaching Python, but using it for demonstration. A more detailed course on Python itself is covered in a separate IEEE Course routinely taught by Dan titled "Python Applications for Digital Design and Signal Processing".

All set-up information for installation of all tools used will be provided prior to the start of class.

Target Audience: All engineers involved in or interested in signal processing for wireless communications. Students should have either taken the earlier course "DSP for Wireless Communications" or have been sufficiently exposed to basic signal processing concepts such as Fourier, Laplace, and Z-transforms, Digital filter (FIR/IIR) structures, and representation of complex digital and analog signals in the time and frequency domains. Please contact Dan at boschen@loglin.com

if you are uncertain about your background or if you would like more information on the course.

Benefits of Attending/ Goals of Course:
Attendees will gain a strong intuitive understanding of the practical and common signal processing implementations found in modern radio and modem architectures and be able to apply these concepts directly to communications system design.

Topics / Schedule:
Class 1: DSP Review, Radio Architectures, Digital Mapping, Pulse Shaping, Eye Diagrams

Class 2: ADC Receiver, CORDIC Rotator, Digital Down Converters, Numerically Controlled Oscillators

Class 3: Digital Control Loops; Output Power Control, Automatic Gain Control

Class 4: Digital Control Loops; Carrier and Timing Recovery, Sigma Delta Converters

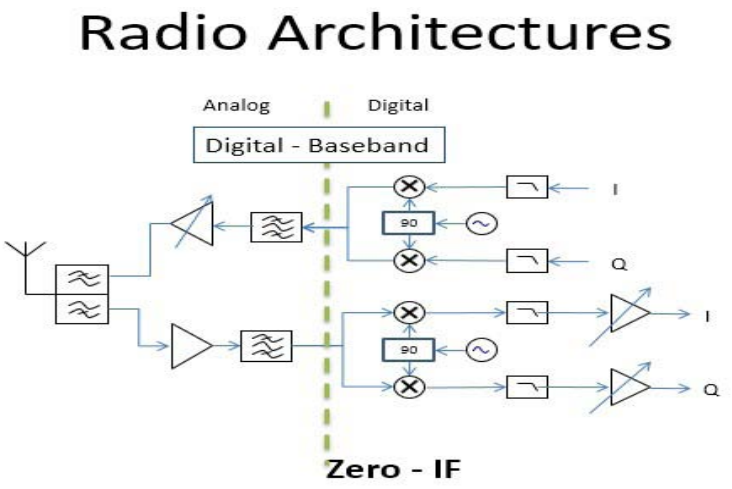
Class 5: RF Signal Impairments, Equalization and Compensation, Linear Feedback Shift Registers

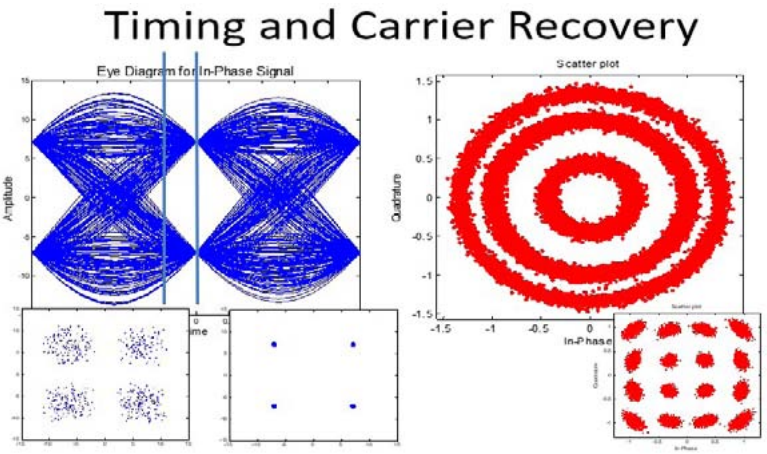
Speaker's Bio:
Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems and has taught courses on DSP to international audiences for over 15 years. Dan is a contributor to Signal Processing Stack Exchange https://dsp.stackexchange.com/, and is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

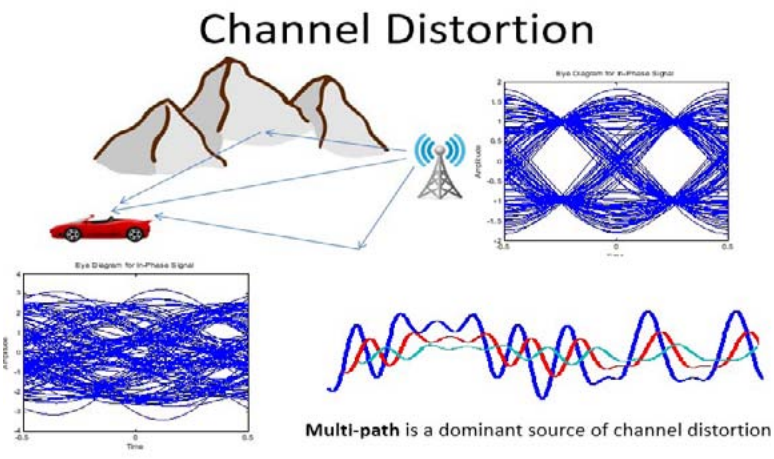
Decision (Run/Cancel) Date for this Course is Thursday, September 30, 2021

IEEE Members	**$190**
Non-members	**$210**

For more background information, please view Dan's Linked-In page at: http://www.linkedin.com/in/dan-boschen







https://ieeeboston.org/event/dspswradio/?instance_id=3098

CALL FOR PAPERS

2022 IEEE International Symposium on Phased Array Systems and Technology

Revolutionary Developments in Phased Arrays

IEEE BOSTON SECTION

11–14 October 2022
The Westin Waltham Boston
Waltham, Massachusetts, USA
www.array2022.org

Sponsors

Platinum

MITRE

Technical Co-sponsors

MTT-S

AESS

APS

About the Symposium

Phased array systems continue to be a rapidly evolving technology with steady advances motivated by the challenges presented to modern military and commercial applications. This symposium will present the most recent advances in phased array technology and present a unique opportunity for members of the international community to interact with colleagues in the field of Phased Array Systems and Technology.

Suggested Topics

- Array Design
- Array Measurements
- Beamforming & Calibration
- T/R Modules
- Radar Systems
- Communications Arrays
- Metamaterial Phased Arrays
- Array Signal Processing
- mmWave and Terahertz
- Wideband Arrays
- Dual Polarized Arrays
- Weather Radar Arrays
- Automotive
- MIMO

See webpage for more details

Special Session Proposals

Please provide suggestions for special sessions to the Technical Program Chair at info@array2022.org

Publication Information

All paper submissions must be in IEEE dual-column format and must be 2 pages (minimum) to 8 pages (maximum) in length including figures, and must be submitted in PDF format via the symposium website (www.array2022.org/call-for-papers). Additional instructions are on the website. All papers will be peer reviewed. Authors of papers presented at ARRAY 2022 conference will be invited to submit an expanded version to the IEEE T-MTT Mini-Special Issue.

Important Dates

• Full paper submission (2-8 pages including figures)	12 March 2022
• Author notification	30 April 2022
• Conference registration deadline for accepted authors	01 Sept 2022

BOSTON 2022

Conference Committee

Conference Chair:
Sean Duffy, MIT LL

Vice Chair:
Wajih Elsallal, MITRE

Technical Program Chair:
David Mooradd, MIT LL

Technical Program Vice Chair:
Glenn Hopkins, GTRI

Special Sessions Chairs:
Matt Facchine, NGC
Kenneth E. Kolodziej, MIT LL

Plenary Session Chairs:
Dan Culkin, NGC
Ellen Ferraro, Raytheon

Tutorials Chairs:
TBD
Will Moulder, MIT LL

Student Program Chairs:
Justin Kasemodel, Raytheon
Matilda Livradaru, STR

Sponsorship/ Exhibits Chairs:
Mark McClure, STR
Marc Angelucci, Lockheed Martin

Publicity Chairs:
Bradley T. Perry, MIT LL
Cara Yang Kataria, MIT LL

Social Media Chair:
Elizabeth Kowalski, MIT LL

Publications Chairs:
Raoul Ouedraogo, MIT LL
Steve Best, MegaWave Corp.

Poster Sessions Chair:
Honglei Chen, The MathWorks

Local Arrangements/Finance:
Robert Alongi, IEEE Boston

Website:
Pierre Dufilie, MIT LL
Kathleen Ballos, Ballos Associates

Advisors:
Alan J. Fenn, MIT LL
Jeffrey S. Herd, MIT LL
Eli Brookner, Raytheon (retired)
William Weedon, Applied Radar
Glenn Meurer, MITRE

Primary Sponsor:
IEEE Boston Section

Modern Applications of RISC-V CPU Design

Last Notice Before Course Begins, Please Register Now!!!

Access Period: September 1 - 30, 2021

Speaker: Steve Hoover, Redwood, EDA

Type of Course: Self-paced, on-demand Course. Lab format

Course Overview: CPUs are a fundamental building block of complex SoCs, and RISC-V is taking hold as the ISA of choice. In this workshop, you will create a Verilog RISC-V CPU from scratch, and you will modify this CPU to be suitable for different applications.

You will learn and use modern techniques, using Transaction-Level Verilog to generate and modify your Verilog code more reliably, in far less time. You will discover how concepts like pipelining and hazards can be incorporated easily using timing-abstract design principles. All labs will be completed online in the Makerchip.com IDE for open-source circuit design. The skills you learn will be applicable far beyond CPU design.

Outline of Topics to be Covered:
Digital logic using TL-Verilog and Makerchip
– combinational logic
– sequential logic
– pipelined logic
– validity
– a calculator circuit
Basic RISC-V CPU microarchitecture
– single-cycle CPU microarchitecture
– testbench, test program, and lab setup for your CPU
– fetch, decode, and execute logic for RISC-V subset
– control flow logic
Pipelined RISC-V subset CPU microarchitecture
– simple pipelining of the CPU
– hazards and PC redirects
Completing the RISC-V CPU
– data memory and load/store
– remaining RISC-V (RV32I) instructions

Course Format:
– self paced, on demand course, providing attendees a flexible schedule
– access to content for 30 days
– pre-scheduled live Zoom and chat sessions with the instructors during the 30 day access period
– offline chat available with instructors during the entire 30 day access period (reply within 24 hours).

Target Audience: Engineers interested in a career in digital logic design or adjacent disciplines, including experienced engineers looking to modernize their skill set.

Prerequisites: An engineering education and basic understanding of digital logic. (Verilog knowledge is not a prerequisite.)

Benefits of Attending:
– Develop a solidified understanding of pipelined CPU design through hands-on labs.
– Acquire knowledge of advanced digital circuit design methodology.
– Gain exposure to an open-source design ecosystem.

Speaker Bio: Steve Hoover is the founder of Redwood EDA, an early-stage startup focused on advanced silicon design methodology and tools. Steve is a former logic design lead for DEC, Compaq, and Intel and has extensive experience designing high-performance server CPUs and network switches.

System Requirements: All resources are free and online; no download or installation required. We will use Slack, Zoom, GitHub Classroom, and Makerchip.com.

Decision (Run/Cancel) Date for this Course is Wednesday, August, 25, 2021

	Before August 15	August 15 or later
IEEE Members	$275	$350
Non-members	$320	$395

http://ieeeboston.org/event/modern-applications-of-risc-v-cpu-design-course/?instance_id=2955

Software Development for Medical Device Manufacturers

Web-based Course with live Instructor!

(11 hours of instructions!)

Times & Dates: 9AM - 4PM ET, Tuesday & Wednesday, November 9 & 10
Speaker: Steve Rakitin, Software Qualtiy Consulting
Course Format: Live Webinar

COURSE SUMMARY: Developing software in compliance with the FDA Design Control regulation, changing FDA guidance documents and latest international standards is challenging. This intensive course provides practical solutions and suggestions for developing software in a manner that meets applicable FDA regulations, guidance documents and international standards, such as IEC-62304:2015. The focus is on interpreting Design Controls for software. Each section of the Design Controls regulation (820.30) is discussed from the perspective of software development. Discussions on key topics such as Software Requirements, Traceability, Design Reviews, Software Verification & Validation and Risk Management (including recently updated standards ISO-14971:2019 and EN-14971:2019) are included. Also discussed are FDA requirements for validation of software development tools and software used in Manufacturing and Quality Systems. Also discussed are recent FDA Guidance Documents on Cybersecurity, Mobile Apps, and Usability.

THIS COURSE IS INTENDED FOR: Software engineers, project managers, quality managers, software quality professionals, RA/QA staff, and anyone who needs to develop cost-effective processes and procedures that will enable their organizations to deliver high quality software-based medical devices that comply with FDA regulations and international standards. This course is also appropriate for people who are new to the medical device industry. Course notes, access to an extensive collection of reference documents and a training certificate are provided.

COURSE OUTLINE: This course will be presented with a live instructor using web-meeting software. The course content will be covered in 4 sessions as described below.

SESSION 1 – Regulatory Context
Duration ~3 hours with one 15 min break
This session will cover key regulatory requirements for medical device software in the US and EU.

Regulations and Guidance:
• FDA Medical Device Regulation (21 CFR Part 820 – specifically, design controls)
• EU Medical Device Regulation
• FDA Guidance Documents:
• Guidance for Content of Pre-market Submissions for Medical Devices Containing Software
• Off-the-Shelf Software Use in Medical Devices
• General Principles of Software Validation
• Content of Premarket Submissions for Management of Cybersecurity in Medical Devices
• Policy for Software Device Functions and Mobile Medical Applications
• Applying Human Factors and Usability Engineering to Medical Devices

International Standards:
• ISO 13485:2016 Medical Devices – Quality Management Systems
• IEC 62304: 2015 Medical Device Software – Software Lifecycle Processes
• ISO 14971: 2019 Application of Risk Management to Medical Devices

• EN 14971: 2019 Application of Risk Management to Medical Devices
• Off-the-Shelf (OTS) Software and Open Source software (SOUP)
• Discussion: All Software Is Defective…

SESSION 2 – FDA Design Controls and IEC 62304 – Part 1
Duration ~2.5 hours with one 15 min break
This session will cover FDA Design Controls and IEC 62304 requirements for medical device software.

• Design and Development Planning
    • How does Agile Development fit?
    • Medical Device Software Lifecycle Processes
• Risk Management
    • FDA Levels of Concern
    • IEC 62304 Software Safety Classification
• Software Requirements
    • Techniques for Removing Ambiguity from Requirements
• Software Architecture and Design
• Software Design Changes

SESSION 3 – FDA Design Controls and IEC 62304 – Part 2
Duration ~2.5 hours with one 15 min break
This session will cover Software Verification and Validation requirements.

• Software Implementation
• Software Verification
    • Technical Reviews
    • Static Analysis
    • Unit and Integration Testing
• System Testing
• Software Validation Testing

SESSION 4 – Software Tool Validation and Risk Management
Duration ~2.5 hours with one 15 min break
This session will cover Software Tool Validation and Risk Management requirements.
• Software Tool Validation
    • Deciding which tools need to be validated
    • Validation approach for software tools
• Validation of Manufacturing Software and Quality System Software
• Risk Management Using Fault Tree Analysis (FTA)
    • Review of ISO/EN 14971:2019 Requirements
    • Example of Fault Tree Analysis and Failure Modes Effect Criticality Analysis (FMECA)

About the instructor: Steven R. Rakitin has over 45 years experience as a software engineer. He has over 30 years of experience in the medical device industry and has been a medical device consultant for over 20 years. He has worked with over 100 medical device manufacturers and biotech companies worldwide, from startups to Fortune 100 corporations. He has published papers on medical device software risk management as well as a book titled: Software Verification & Validation for Practitioners and Managers.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE.

Steve works collaboratively with medical device companies to help them comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

Decision (Run/Cancel) Date for this Course is Wednesday, November 3, 2021

IEEE Members	**$285**
Non-members	**$345**

http://ieeeboston.org/event/live-course-software-development-for-medical-device-manufacturers/

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.
If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- **Honoraria can be considered for course lecturers**
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

REGISTER NOW FOR FREE!

Every Wednesday in August

August 4: 5G/WiFi/IoT

August 11: PCB/Interconnect

August 18: Radar/Automotive/SATCOM

August 25: Signal Integrity/Power Integrity

www.edicononline.com

Earn IEEE CEU/PDH credits! Win a book from Artech House!

Platinum Sponsors: KEYSIGHT TECHNOLOGIES, samtec, ALTAIR

PCB Keynote Sponsor: Averatek

IEEE BOSTON SECTION

25th Annual

2021 IEEE High Performance Extreme Computing Virtual Conference

21 - 23 September 2021

IEEE-HPEC.ORG

IEEE HPEC High Performance Extreme Computing

DELL Technologies | Hewlett Packard Enterprise | Lenovo | NVIDIA | MITRE | MIT Lincoln Laboratory | siam

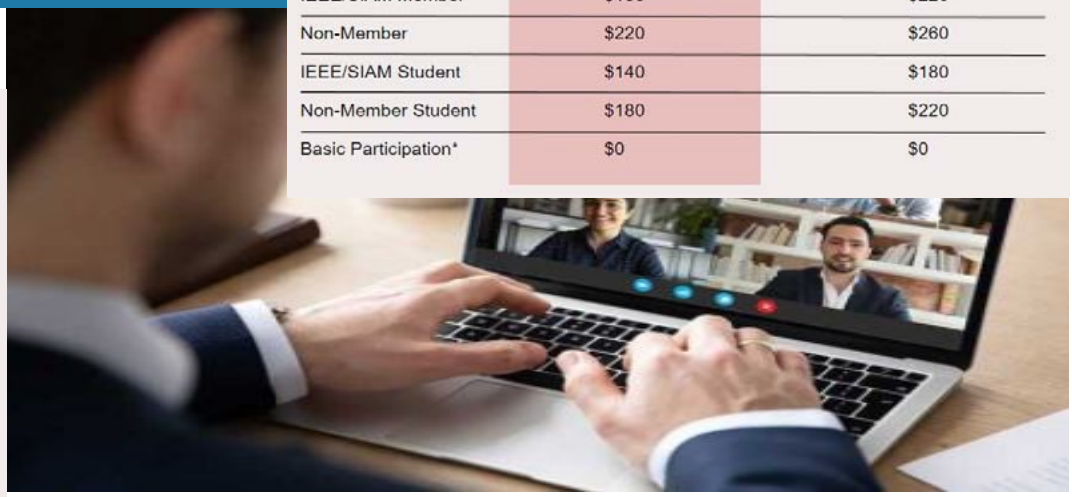
Early-bird registration ends on September 1, 2021

REGISTER NOW!

	EARLY Registration (ends September 1, 2021)	Standard Registration (ends September 23, 2021)
IEEE/SIAM Member	$180	$220
Non-Member	$220	$260
IEEE/SIAM Student	$140	$180
Non-Member Student	$180	$220
Basic Participation*	$0	$0

Special Events!

- ⇒ **MIT/Amazon/IEEE Graph Challenge**
- ⇒ **GraphBLAS**
- ⇒ **Remote Sensing for Humanitarian Assistance & Disaster Relief**
- ⇒ **HPSEC: High Performance Secure Extreme Computing**
- ⇒ **BRAIDS**
- ⇒ **Bridging Quantum and High Performance Computing**
- ⇒ **Scaling HPC Education**
- ⇒ **AI Challenges**



Distinguished Speakers!

info@IEEE-HPEC.org