BOSTON

THE REFLECTOR

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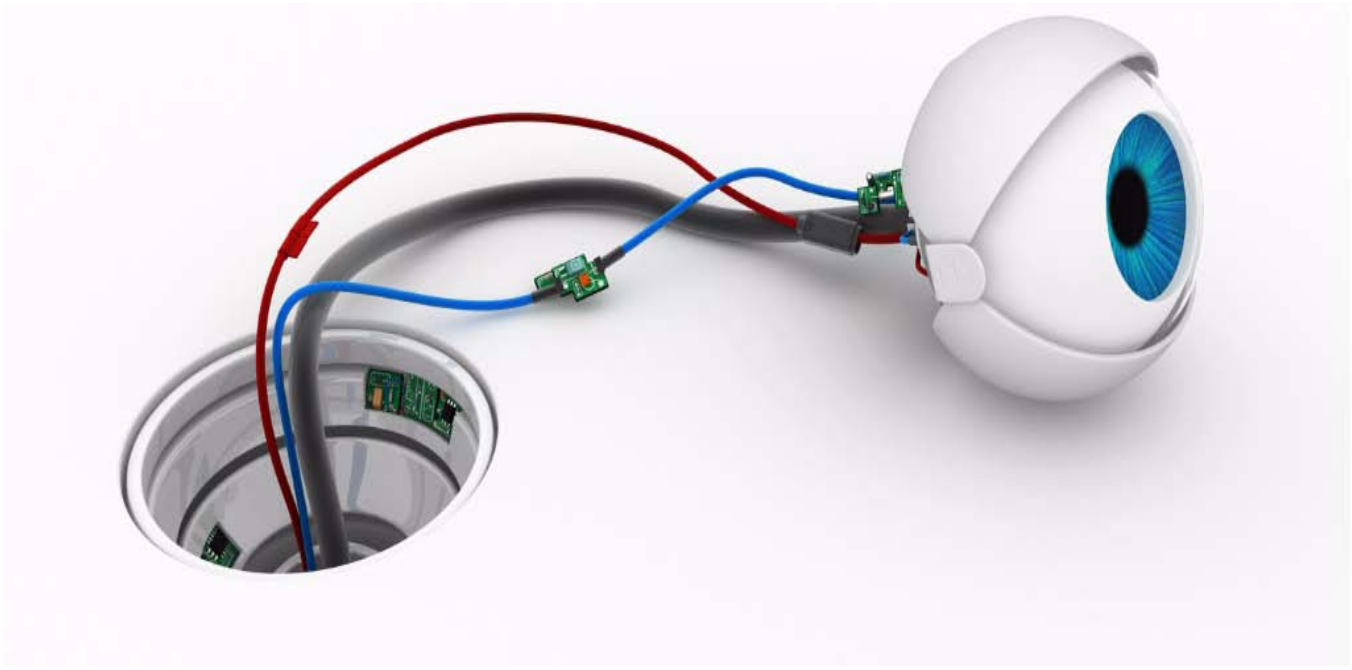

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A Lifetime of Learning Provided by IEEE- Boston!

By Lennart E. Long, IEEE Boston Section Excom

My introduction to IEEE-Boston was in 1956 when the Northeastern University Student Chapter decided to run a paper contest. As a consummate geek I never expected to win but I did. Then, when I moved here after an Army tour of duty, I thought it might be good to pay back IEEE-Boston by joining the EMC Society Chapter. I was invited to be the Chair of that Chapter and held that office for a couple of years. At that time I was invited to join the IEEE-Boston Executive Committee where I have served ever since. IEEE has made a significant contribution to my career. It has helped me cultivate ideas for my multiple patents, helped me manage a group of engineers and scientists, and helped me train myself in multiple disciplines.

Even as an ageing engineer as the Chair of the Life Members Affinity Group, I have learned a lot about how older engineers spend their time and energy. I am still working today using the knowledge and skill obtained from IEEE. I learned that the technical offerings provided by the IEEE Boston Section are key to technical success and the meetings provide the social interaction which allows me to network with people of all management and technical levels. This interaction provides Chapter and Society members with inside information for engineers trying to solve similar problems and issues. Members of the Chapters also provided me with technical, management and government contacts who I could ask to be speakers for Section Conferences and IEEE-Boston training courses. All this is made possible by the highly effective and professional personnel that staff the IEEE Boston Section Office, Bob Alongi, the Business Manager and Karen Safina the Administrative Assistant.

How does the IEEE-Boston offerings differ from University offerings? The main difference is that University offerings are mainly academic whereas the IEEE-Boston are practical, applications oriented and are designed to enhance working engineers' career. We focus our courses, both online and in-person as well as our conferences by attending the University of New Hampshire's Industry Advisory Board. In addition, we poll our members for subjects that the working engineers are concerned about at the present time. I encourage you to participate in your IEEE-Boston Society Chapter of interest. It could pay many dividends to you.

IEEE Boston Section Social Media Links:

Twitter: https://twitter.com/ieeeboston

Facebook: https://www.facebook.com/IEEEBoston

YouTube: https://www.youtube.com/user/IEEEBostonSection

LinkedIn: https://www.linkedin.com/groups/3763694

IEEE Boston Section Online Courses:

(Students have 180 day access to all online, self-paced courses)

Electronic Reliability Tutorial Series (NEW!!!)
Full course description and registration at ,
http://ieeeboston.org/electronic-reliability/

Verilog101:Verilog Foundations
Full course description and registration at ,
http://ieeeboston.org/verilog-101-verilog-foundations-online-course/

System Verilog 101: Design Constructs
Full course description and registration at ,
http://ieeeboston.org/systemverilog-101-sv101-design-constructs-online-course/

System Verilog 102: Verification Constructs
Full course description and registration at ,
http://ieeeboston.org/systemverilog-102-sv102-verification-constructs-online-course/

High Performance Project Management
Full course description and registration at ,
http://ieeeboston.org/high-performance-project-management-online-course/

Introduction to Embedded Linux Part I
Full course description and registration at ,
http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/

Embedded Linux Optimization - Tools and Techniques
Full course description and registration at ,
http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/

Embedded Linux Board Support Packages and Device Drivers
Full course description and registration at ,
http://ieeeboston.org/embedded-linux-bsps-device-drivers-line-course/

Software Development for Medical Device Manufacturers
Full course description and registration at ,
http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/

Fundamental Mathematics Concepts Relating to Electromagnetics
Full course description and registration at ,
http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/

Reliability Engineering for the Business World
Full course description and registration at ,
http://ieeeboston.org/reliability-engineering-business-world-line-course/

Design Thinking for Today's Technical Work
http://ieeeboston.org/design-thinking-technical-work-line-course/

Fundamentals of Real-Time Operating Systems
http://ieeeboston.org/fundamentals-of-real-time-operating-systems-rt201-on-line-course/

Geoscience & Remote Sensing Society – 6:00PM, Tuesday, July 20

Simulating the Performance of Ocean-Observing Imaging Payloads for Nanosatellites

Location: Zoom

Speaker: Candence Brea Payne

Earth's oceans are the largest defining feature of our planet and arguably an invaluable resource. Consequences of climate change threaten to have substantial and irreversible negative effects on our oceans, making it crucial to quickly understand and quantify behavioral changes resulting from increased human impact. Near-continuous, large-scale monitoring from space is revolutionizing methods for monitoring and forecasting ocean behavior. Nanosatellite platforms offer a potential solution for large-scale deployment of ocean-sensing instruments that provide detailed measurements of critical characteristics. Monitoring these key features provides valuable insight to behavioral changes within the context of our shifting climate.

Constellations of nanosatellites that target key ocean characteristics could provide continuous ocean monitoring with high spatiotemporal resolution. Compared with current state-of-the-art ocean-observing spacecraft, such as NASA's Moderate Resolution Imaging Spectroradiometer (MODIS) with a repeat cycle of 16 days, nanosatellites in Low-Earth Orbit (LEO) can observe the same ground scene roughly once every five days. While spacecraft such as NASA's Geostationary Operational. Environmental Satellite (GOES) achieves high temporal resolution, imaging the same scene every 30 seconds to 15 minutes depending on target region size, they are limited to imaging a single ground scene due to their stationary placement. Constellations of nanosatellites offer opportunities for measurement improvement including reducing revisit rates down from several days to hours, as well as increasing surface coverage through placement in orbital planes of varying inclinations. Informative, emergent information such as sea surface salinity, front location, and fauna concentrations (namely phytoplankton) are derived from measuring key characteristics such as ocean color and Sea Surface Temperature (SST). Existing nanosatellite constellations such as Planet's Flock-3p, composed of 88 3U (10 x 10 x 30 cm) CubeSats, provide daily coverage of Earth's land mass; however, they do not yet target oceans and coastal regions, nor tailor their imaging bands for these specific measurement needs. We present a concise set of ocean measurement band centers for an imaging payload targeting ocean color, a key behavioral feature. We assume narrow-band (10 - 15 nm bandwidth) ocean color measurements (390 nm - 865 nm) and constrain the payload to within the volume of a U-class (3U / 6U / 12U) nanosatellite located in LEO (~ 450 km altitude). A radiometric link approach is used to develop a tool that compares the performance of multiple different available Commercial

Off-the-Shelf (COTS) detectors, as well as different detector and optical front-end combinations. As detector sensitivity performance is driven primarily by aperture size and focal length, the imaging payload is assumed to have a scalable aperture (e.g.,diameter, focal length) and tunable sensor parameters (e.g., pixel pitch, number of pixels, sensor format). We simulate the sensor's performance primarily by scaling the aperture from 0.5 cm to 20 cm diameter, suitable for 0.5U - 12U CubeSat volumes. Simulation results determine key "cut-off" regions where collected data no longer achieve the desired measured sensitivity of the target feature. A discussion of the radiometric approach, including definition of the measurement and detector parameter trade-space, is provided, along with preliminarily results of the simulated performance.

Cadence Payne is a 4th year PhD student in the department of Aeronautics and Astronautics in the Space Telecommunications, Astronomy, and Radiation Laboratory advised by Dr. Kerri Cahoy. Her research at MIT focuses on technology development for small, Earth-observing spacecraft called CubeSats. She is currently the lead Systems Engineer for the Auroral Emission Radio Observer (AERO), a 3U CubeSat that uses a 4-meter vector sensor antenna to probe low-frequency emission from the Earth's aurora. She is also supporting AEROS, a joint mission with MIT Portugal that collects data for climate and weather monitoring via ocean observations. She graduated from Morehead State University in 2017 with a BS in Space Science and a minor in astronomy.

Celebrating L. Dennis Shapiro

A pioneer in the personal emergency response systems industry, L. Dennis Shapiro was dedicated in all he did, including helping people live more safely, building companies that made a difference and patenting new inventions. His patents included innovations in motion detector technology (Aritech Corp), and the premier emergency response alert (Lifeline Systems), that has saved countless lives and to this day enables elderly people and others with medical needs to live independently. Shapiro was also a philanthropist and avid collector.

Shapiro, an IEEE Life Fellow elevated in 2013 for development and commercialization of personal emergency response systems, was a very active IEEE volunteer. He was a member of IEEE Communications and Consumer Technologies Societies, and served on the boards of both. He founded the Boston chapter of Consumer Technology Society and spearheaded an effort to reinvigorate the society, which included a rebranding effort.

He served on the IEEE Foundation (https://www.ieeefoundation.org/Home) Board of Directors from 2019 until this year and was a member of the IEEE Heritage Circle (https://www.ieeefoundation.org/donors/heritage-circle) at the Alexander Graham Bell level. The donor-recognition program acknowledges members who have pledged more than US$10,000 to support IEEE programs (https://www.ieeefoundation.org/what-to-support).

Through his giving, Shapiro sought to bring the history of technology to a wider audience and lead by example. As a devoted reader of “Scanning Our Past” a feature in Proceedings of the IEEE, one of his donations allowed six of the features to be available via open access. In 2019, he also donated three historical documents featuring Edwin H. Armstrong and Thomas Edison from his personal collection to the IEEE History Center.

In Shapiro’s memory, the IEEE Foundation established the IEEE L. Dennis Shapiro Collection Fund (https://www.ieeefoundation.org/Shapiro) and will match the first $10,000 in giving to the Shapiro Fund to support the work of the IEEE History Center. The fund celebrates and advances his passion for collecting artifacts and promoting the heritage of electrical engineering. Donations to the fund (https://www.ieeefoundation.org/Shapiro) support acquisitions to enhance and complement the Center’s holdings. The artifacts and other objects collected thanks to fund donations will be noted as part of the Shapiro Collection when referenced in exhibits and publications.

Donate today to honor Dennis’ passion for collecting and commitment to advancing the preservation and promulgation of the history of technology through objects and artifacts.

Read more about Shapiro’s life and accomplishments (https://spectrum.ieee.org/the-institute/ieee-member-news/a-tribute-to-l-dennis-shapiro-who-helped-develop-the-life-alert-personal-emergencyresponse-system)

Boston MTT-S Chapter Receives the 2020 Outstanding Chapter Award!

MTT-S
IEEE MICROWAVE THEORY & TECHNIQUES SOCIETY

The Boston Chapter of the IEEE Microwave Theory and Techniques Society (MTT-S) has won the 2020 Outstanding Chapter Award! This award is given annually based on the quantity and quality of the activities and programs implemented by the chapters during the year.

The Boston Chapter (Vice-Chaired by Lincoln Laboratory’s Youngho Suh) will be featured in an upcoming MTT-S Magazine to describe its activities.

IEEE Video Series

A collaborative discussion panel featuring esteemed members from the Institute of Electrical and Electronics Engineers has convened in 2021 to produce educational video presentations that embrace IEEE's mission of advancing technology for humanity.

Among the programs they've produced include "Electric Vehicles: Fun Saving Our Planet", "Greener Power For More Electric Vehicles", "Overcoming Nuclear Fears To Achieve Net Zero CO2 By 2050" and "Achieving a Net Zero Carbon Future". Projects currently in production include the expansive topic of futurology, with a focus on increasing the efficiency and transformation of aging electrical power generating stations and infrastructure to accommodate nuclear power; reviewing the viability of alternative energy (such as geothermal, wind and solar); and focusing on 'cleaner' fossil fuels that are more environmentally-friendly to slow the rate of climate change.

These shows are produced and directed by Lennart E. Long, IEEE Senior Life Member from the Executive Committee and Past Chair of the Boston Section; Dr. Paul H Carr, BS, MS, MIT; PhD Brandeis U, IEEE Life Fellow; Dr. Ted Kochanski, SB (MIT), Ph.D (U.Texas, Austin), IEEE Global Education for Microelectronic Systems and former Boston Section Chair; and Dr. Ken Laker, B.E. (Manhattan College), M.S. and Ph.D. (New York University), IEEE Life Fellow and past President of IEEE.

The panel is moderated by five-time Boston/New England Emmy Award-winner and television personality and star of "The Folklorist," John Horrigan.

These video programs with presentations and discussions can be accessed at the IEEE Boston Section video portal at https://vimeo.com/user18608275.

We are looking for any IEEE members that would like to appear on the program in the role of presenter or discussion expert. Simply reach out to Robert Alongi at the Boston Section at, ieeebostonsection@gmail.com.

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.
If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- **Honoraria can be considered for course lecturers**
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

MIT URTC 2021 10/8 - 10/10, 2021

UNDERGRADUATE RESEARCH TECHNOLOGY CONFERENCE

IN PARTNERSHIP WITH IEEE MIT

Passionate about research in technology? Looking to share your work with peers and professionals?

Join us at MIT URTC 2021!

PAPERS

EARLY SUBMISSION DEADLINE	JULY 11, 2021
EARLY NOTIFICATION OF ACCEPTANCE	JULY 31, 2021
REGULAR SUBMISSION DEADLINE	JULY 31, 2021
REGULAR NOTIFICATION OF ACCEPTANCE	AUGUST 21, 2021

POSTERS & LIGHTNING TALKS

SUBMISSION DEADLINE	AUGUST 29, 2021
NOTIFICATION OF ACCEPTANCE	SEPTEMBER 5, 2021

CONFERENCE DATES

10/8 - 10/10, 2021

Technical Tracks

1. **Biological and Biomedical Engineering (BioEECS)**
2. **Circuits, Materials, and Nanotechnologies**
3. **Computer Systems, Theoretical Computer Science and Mathematics**
4. **Machine Learning / Artificial Intelligence (AI)**
5. **Robotics and Controls**
6. **Security and Communications**
7. **Space Application and Technologies**
8. **Innovation Research**

Submission Site:
https://cmt3.research.microsoft.com/URTC2021

5G The Best Channel Codes:

Polar Codes with MATLAB Applications

Web-based Course with live Instructor!

Times & Dates: 10 – 11AM ET, September 14, 16, 21, 23, 28, 30, October 5, 7, 12, 14
Speaker: Orhan Gazi, Cankaya University, Ankara-Turkey
Course Format: Live Webinar, 10, one hour, sessions

Introduction: Forward error correction is a vital process in communication systems. The last channel codes discovered in the research world are the "polar codes" which are adapted to be used in 5G standard. The construction and decoding of polar codes are quite different from the construction and decoding of classical channel nodes. Polar codes are the only codes constructed in a non-trivial manner. The discovery of polar codes can be considered as a breakthrough in coding society. It is clear that future channel codes will follow the logic of polar codes. For this reason, it is critical to learn the encoding and decoding philosophy of the polar codes which is the state of art of the coding world.

Outline of the topics to be covered:

- Entropy and Mutual Information
- Philosophy of Polar Codes
- Generator Matrices of Polar Codes
- Polar Encoder Structures
- Recursive Structures for Polar Encoders
- Channel Splitting and Concept of Channel Polarization
- Split Channels
- Calculation of Split Channel Capacities
- Polar Decoding
- Polar Decoding for Noiseless Transmission
- Polar Decoding Formulas for Kernel Structure for noisy Transmission
- Successive Cancelation Decoding of Polar Codes
- Belief Propagation Decoding of Polar Codes
- Polar Encoders and Decoders in 5G New Radio (NR) and Future Channel Codes

Target Audience: Electronic and Communication Engineers, electronic engineers, computer engineers, engineers working in communication industry

Benefits of Attending Course:
1) The participant will have an idea about the state of art polar codes.
2) Polar codes are used in 5G standard; the participant can comprehend the polar code used in 5G standard.
3) The participant will learn successive cancelation decoding of polar codes.

Speaker Bio: Prof. Orhan Gazi is the author of the book "Polar Codes. A Non-Trivial Approach to Channel Coding" which can be reached from https://www.springer.com/gp/book/9789811307362

The book is selected by IEEE COMSOC as one of the best readings in polar codes, https://www.comsoc.org/publications/best-readings/polar-coding

Prof. Orhan Gazi is the sole author of 10 books written in electrical engineering subjects. Apart from the polar code book, he is the single author of the books "Information Theory for Electrical Engineers" https://www.springer.com/gp/book/9789811084317 and "Forward Error Correction via Channel Coding" https://www.springer.com/gp/book/9783030333799. The research area of Prof. Orhan Gazi involves "channel coding", and "digital communication subjects". Recently, he focuses on over capacity data transmission using polar codes. He is also interested in practical applications of communication systems involving FPGA devices. He is delivering courses with titles "VHDL circuit design", "interface design using VHDL for FPGA devices" and "system on chip design".

Materials to be included: Lecture slides will be provided.

Decision (Run/Cancel) Date for this Course is Wednesday, September 8, 2021

IEEE Members	**$250**
Non-members	**$300**

https://ieeeboston.org/event/5g-the-best-channel-codes/?instance_id=3068

Information Theory for Electronic Communication with MATLAB Applications

(12 hours of instruction!)

Web-based Course with live Instructor!

Times & Dates: 10 AM - 11:30 AM ET - July 20, 22, 27, 29, August 3, 5, 10, 12

Speaker: Orhan Gazi, Cankaya University, Ankara-Turkey

Course Format: Live Webinar, 8, 90 minute sessions

Introduction: Information theory was born with the publication of Shannon's paper, a mathematical theory of communication, in 1948. In his paper, Shannon defined the terms entropy, mutual information, and channel capacity which is the maximum reliable transmission speed for a given signal-to-noise ratio. Shannon also stated 'channel coding theorem' in his paper, which opened another research area, design of channel codes, in communication field. The concept of data compression aroused after Shannon's paper. Any engineer working in the communication industry must have some knowledge about information theory. Especially knowledge of capacity is very critical to compare the performance of communication systems with each other. In this course, we will provide information about basic concept of information theory. We will also provide some practical applications using MATLAB platform.

Prerequisite: The one who is interested in taking this course should have basic knowledge of probability and random variables. He or She should be familiar with the terms probability mass function, probability density function, random variable, expected value, variance, etc.

- Discrete Entropy, Mutual Information for Discrete Channels, Information Channels
- MATLAB Applications for Entropy and Mutual Information
- Entropy for Continuous Random Variables, Discrete and Continuous Channel Capacities
- Bounds and Limiting Cases for AWGN Channel Capacity
- MATLAB Applications for Channel Capacities
- Typical Sequences and Data Compression
- MATLAB Applications for Data Compressions
- Channel Coding Theorem

Target Audience: Electronic and Communication Engineers, electronic engineers, computer engineers, engineers working in communication industry

Benefits of Attending Course:

1) The participant will have an idea about Shannon's information theory.
2) The participant will have an idea about transmission channel capacity.
3) The participant will learn the logic behind the data compression concept.
4) The participant will be able to compare the performances of two different communication systems.
5) The participant will have an idea about the factors affecting maximum transmission speed.

Speaker Bio: Prof. Orhan Gazi is the author of the book "Information Theory for Electrical Engineers" https://www.springer.com/gp/book/9789811084317 Prof. Orhan Gazi is the sole author of 10 books written in electrical engineering subjects.

He is also the author of the book "Polar Codes. A Non-Trivial Approach to Channel Coding" which can be reached from https://www.springer.com/gp/book/9789811307362

The book is selected by IEEE COMSOC as one of the best readings in polar codes, https://www.comsoc.org/publications/best-readings/polar-coding

He is also the single author of the book "Forward Error Correction via Channel Coding" https://www.springer.com/gp/book/9783030333799

The research area of Prof. Orhan Gazi involves "channel coding", and "digital communication subjects". Recently, he focuses on over capacity data transmission using polar codes. He is also interested in practical applications of communication systems involving FPGA devices. He is delivering courses with titles "VHDL circuit design", "interface design using VHDL for FPGA devices" and "system on chip design".

Materials to be included: Lecture slides will be provided.

Decision (Run/Cancel) Date for this Course is Wednesday, July 14, 2021

IEEE Members	**$250**
Non-members	**$300**

https://ieeeboston.org/event/information-theory-for-electronic-communication/?instance_id=3060

Call for Articles

Now that the Reflector is all electronic, we are expanding the content of the publication. One of the new features we will be adding are technical, professional development, and general interest articles to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development or general interest articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional/interest articles will be reviewed by the Publications Committee for suitability.The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!
Submissions should be sent to;
ieeebostonsection@gmail.com

Python Applications for Digital Design and Signal Processing

Dates & Times: **Thursday, November 11, 2021, videos released weekly 2x1.5 hours**
Live Workshops: 7:00 - 8:00PM ET; Tuesdays, November 16, 23, 30, December 7

Speaker: **Dan Boschen**

Location: **Zoom**

This is a hands-on course combining pre-recorded lectures with live Q&A and workshop sessions in the popular and powerful open-source Python programming language.

New Format with Pre-Recorded Videos: The course format has been updated to release pre-recorded video lectures that students can watch on their own schedule, and an unlimited number of times, prior to live Q&A workshop sessions on Zoom with the instructor. The videos will also be available to the students for viewing for up to two months after the conclusion of the course.

Overview: Dan provides simple, straight-forward navigation through the multiple configurations and options, providing a best-practices approach for quickly getting up to speed using Python for modelling and analysis for applications in signal processing and digital design verification. Students will be using the Anaconda distribution, which combines Python with the most popular data science applications, and Jupyter Notebooks for a rich, interactive experience.

The course begins with basic Python data structures and constructs, including key “Pythonic” concepts, followed by an overview and use of popular packages for scientific computing enabling rapid prototyping for system design.

During the course students will create example designs including a sigma delta converter and direct digital synthesizer both in floating point and fixed point. This will include considerations for cycle and bit accurate models useful for digital design verification (FPGA/ASIC), while bringing forward the signal processing tools for frequency and time domain analysis.

Jupyter Notebooks: This course makes extensive use of Jupyter Notebooks which combines running Python code with interactive plots and graphics for a rich user experience. Jupyter Notebooks is an open-source web-based application (that can be run locally) that allows users to create and share visually appealing documents containing code, graphics, visualizations and interactive plots. Students will be able to interact with the notebook contents and use “take-it-with-you” results for future applications in signal processing.

Target Audience: This course is targeted toward users with little to no prior experience in Python, however familiarity with other modern programming languages and an exposure to object-oriented constructs is very helpful. Students should be comfortable with basic signal processing concepts in the frequency and time domain. Familiarity with Matlab or Octave is not required, but the equivalent operations in Python using the NumPy package will be provided for those students that do currently use Matlab and/or Octave for signal processing applications.
Benefits of Attending / Goals of Course: Attendees will gain an overall appreciation of using Python and quickly get up to speed in best practice use of Python and related tools specific to modeling and simulation for signal processing analysis and design.

All set-up information for the installation of all tools will be provided before the start of class.

Topics / Schedule:

Pre-recorded lectures (3 hours each) will be distributed Friday prior to all Workshop dates. Workshop/ Q&A Sessions are 7pm-8pm on the dates listed below:

Tuesday, November 16

Topic 1: Intro to Jupyter Notebooks, the Spyder IDE and the course design examples. Core Python constructs.

Tuesday, November 23

Topic 2: Core Python constructs; iterators, functions, reading writing data files.

Tuesday, November 30

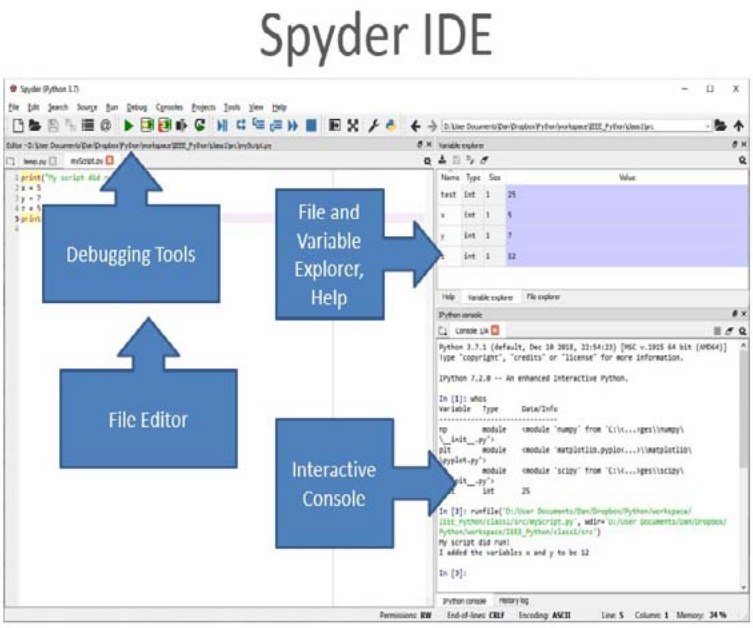
Topic 3: Signal processing simulation with popular packages including NumPy, SciPy, and Matplotlib.

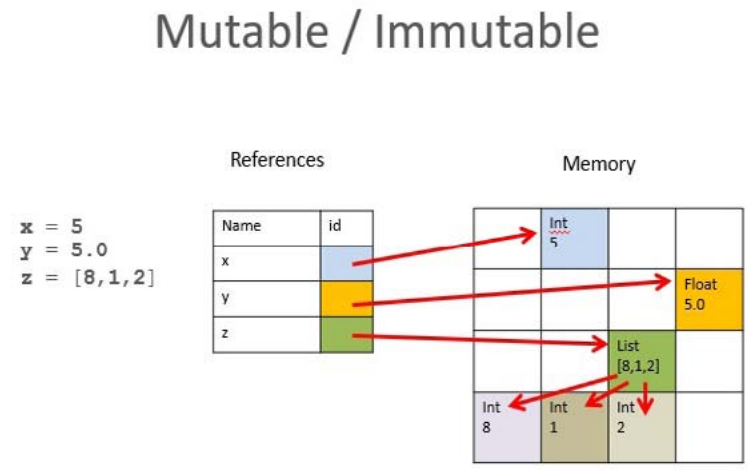
Tuesday, December 7

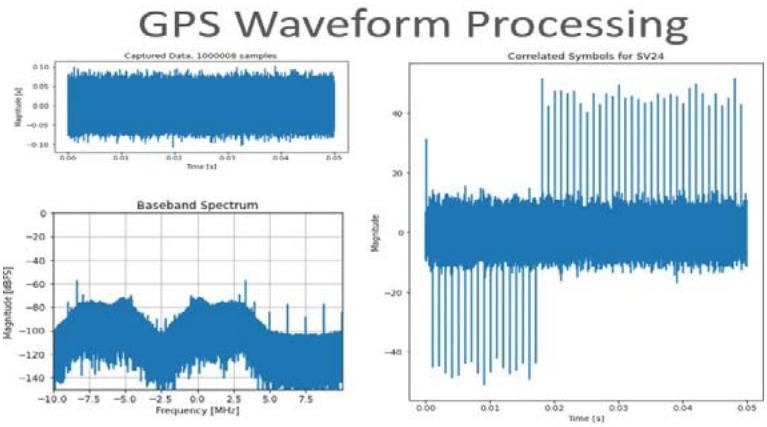
Topic 4: Bit/cycle accurate modelling and analysis using the design examples and simulation packages

Speaker's Bio: Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems and has taught courses on DSP to international audiences for over 15 years. Dan is a contributor to Signal Processing Stack Exchange https://dsp.stackexchange.com/, and is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page (https://www.linkedin.com/in/dan-boschen/)







Decision (Run/Cancel) Date for this Course is Thursday, November 4, 2021

IEEE Members	**$190**
Non-members	**$210**

https://ieeeboston.org/event/pythonapplications/?instance_id=3109

Digital Signal Processing (DSP) for Software Radio

Dates & Times: **Thursday, October 7, 2021, Videos released weekly 2x1.5 hours**
Live Workshops: 7:00 - 8:00PM ET; Tuesdays, October 12, 19, 26, November 2, 9

Speaker: **Dan Boschen**

Location: **Zoom**

New Format Combining Live Workshops with Pre-recorded Video

This is a hands-on course providing pre-recorded lectures that students can watch on their own schedule and an unlimited number of times prior to live Q&A/Workshop sessions with the instructor. Ten 1.5 hour videos released 2 per week while the course is in session will be available for up to two months after the conclusion of the course.

Course Summary This course builds on the IEEE course "DSP for Wireless Communications" also taught by Dan Boschen, further detailing digital signal processing most applicable to practical real-world problems and applications in radio communication systems. Students need not have taken the prior course if they are familiar with fundamental DSP concepts such as the Laplace and Z transform and basic digital filter design principles.

This course brings together core DSP concepts to address signal processing challenges encountered in radios and modems for modern wireless communications. Specific areas covered include carrier and timing recovery, equalization, automatic gain control, and considerations to mitigate the effects of RF and channel distortions such as multipath, phase noise and amplitude/phase offsets.

Dan builds an intuitive understanding of the underlying mathematics through the use of graphics, visual demonstrations, and real-world applications for mixed signal (analog/digital) modern transceivers. This course is applicable to DSP algorithm development with a focus on meeting practical hardware development challenges, rather than a tutorial on implementations with DSP processors.

Now with Jupyter Notebooks! This long-running IEEE Course has been updated to include Jupyter Notebooks which incorporates graphics together with Python simulation code to provide a "take-it-with-you" interactive user experience. No knowledge of Python is required but the notebooks will provide a basic framework for proceeding with further signal processing development using that tools for those that have interest in doing so.

This course will not be teaching Python, but using it for demonstration. A more detailed course on Python itself is covered in a separate IEEE Course routinely taught by Dan titled "Python Applications for Digital Design and Signal Processing".

All set-up information for installation of all tools used will be provided prior to the start of class.

Target Audience: All engineers involved in or interested in signal processing for wireless communications. Students should have either taken the earlier course "DSP for Wireless Communications" or have been sufficiently exposed to basic signal processing concepts such as Fourier, Laplace, and Z-transforms, Digital filter (FIR/IIR) structures, and representation of complex digital and analog signals in the time and frequency domains. Please contact Dan at boschen@loglin.com

if you are uncertain about your background or if you would like more information on the course.

Benefits of Attending/ Goals of Course:
Attendees will gain a strong intuitive understanding of the practical and common signal processing implementations found in modern radio and modem architectures and be able to apply these concepts directly to communications system design.

Topics / Schedule:
Class 1: DSP Review, Radio Architectures, Digital Mapping, Pulse Shaping, Eye Diagrams

Class 2: ADC Receiver, CORDIC Rotator, Digital Down Converters, Numerically Controlled Oscillators

Class 3: Digital Control Loops; Output Power Control, Automatic Gain Control

Class 4: Digital Control Loops; Carrier and Timing Recovery, Sigma Delta Converters

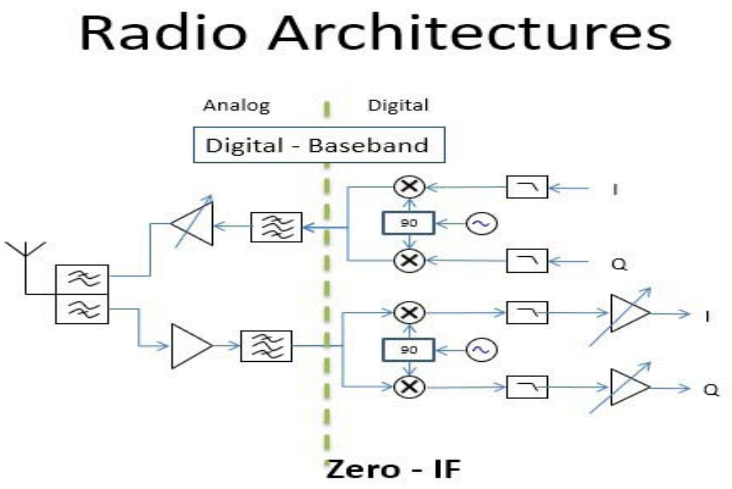
Class 5: RF Signal Impairments, Equalization and Compensation, Linear Feedback Shift Registers

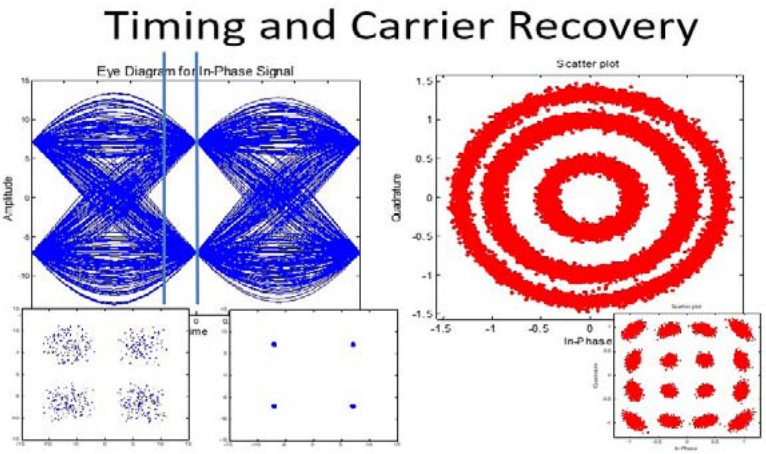
Speaker's Bio:
Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems and has taught courses on DSP to international audiences for over 15 years. Dan is a contributor to Signal Processing Stack Exchange https://dsp.stackexchange.com/, and is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

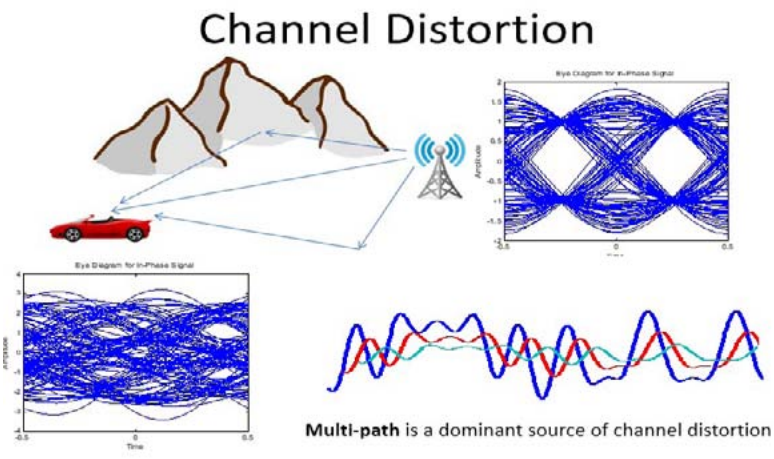
Decision (Run/Cancel) Date for this Course is Thursday, September 30, 2021

IEEE Members	**$190**
Non-members	**$210**

For more background information, please view Dan's Linked-In page at: http://www.linkedin.com/in/dan-boschen







https://ieeeboston.org/event/dspswradio/?instance_id=3098

Announcing the 2022 IEEE International Symposium on Phased Array Systems and Technology October 11-14, 2022 Greater Boston, Massachusetts, USA

Greetings from the Conference Committee as we assemble an exciting program and hope you will consider joining us at this milestone event in the Greater Boston area. We look forward to the return to in-person networking and collaboration that these events provide.

Phased array technology is evolving at a rapid pace, finding its way into a growing set of commercial and military applications. The 2022 Symposium will highlight the wide spectrum of work going on across the international community and emphasize new developments in the field. While an official call for papers is in the works, the committee wanted to share a preview of the topics we are considering and some important logistical information for this gathering.

Preliminary Technical Program Schedule:

12 March 2022 – full paper submission deadline

30 April 2022 – author notification

01 Sept 2022 – conference registration deadline for accepted authors

Venue: Westin Waltham, Greater Boston, Massachusetts, USA

Suggested Topics:

- Array Design
- Array Measurements
- Beamforming and Calibration
- T/R Modules
- Radar Systems
- Communications Arrays
- Metamaterial Phased Arrays
- Signal Processing and Architectures
- Millimeter Wave and Terahertz
- Wideband Arrays
- Dual polarized arrays
- Weather radar arrays
- Automotive
- MIMO

ARRAY2022.ORG

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Modern Applications of RISC-V CPU Design

Access Period: **September 1 - 30, 2021 (originally scheduled for March '21)**

Speaker: **Steve Hoover, Redwood, EDA**

Type of Course: Self-paced, on-demand Course. Lab format

Course Overview: CPUs are a fundamental building block of complex SoCs, and RISC-V is taking hold as the ISA of choice. In this workshop, you will create a Verilog RISC-V CPU from scratch, and you will modify this CPU to be suitable for different applications.

You will learn and use modern techniques, using Transaction-Level Verilog to generate and modify your Verilog code more reliably, in far less time. You will discover how concepts like pipelining and hazards can be incorporated easily using timing-abstract design principles. All labs will be completed online in the Makerchip.com IDE for open-source circuit design. The skills you learn will be applicable far beyond CPU design.

Outline of Topics to be Covered:
Digital logic using TL-Verilog and Makerchip
– combinational logic
– sequential logic
– pipelined logic
– validity
– a calculator circuit
Basic RISC-V CPU microarchitecture
– single-cycle CPU microarchitecture
– testbench, test program, and lab setup for your CPU
– fetch, decode, and execute logic for RISC-V subset
– control flow logic
Pipelined RISC-V subset CPU microarchitecture
– simple pipelining of the CPU
– hazards and PC redirects
Completing the RISC-V CPU
– data memory and load/store
– remaining RISC-V (RV32I) instructions

Course Format:
– self paced, on demand course, providing attendees a flexible schedule
– access to content for 30 days
– pre-scheduled live Zoom and chat sessions with the instructors during the 30 day access period
– offline chat available with instructors during the entire 30 day access period (reply within 24 hours).

Target Audience: Engineers interested in a career in digital logic design or adjacent disciplines, including experienced engineers looking to modernize their skill set.

Prerequisites: An engineering education and basic understanding of digital logic. (Verilog knowledge is not a prerequisite.)

Benefits of Attending:
– Develop a solidified understanding of pipelined CPU design through hands-on labs.
– Acquire knowledge of advanced digital circuit design methodology.
– Gain exposure to an open-source design ecosystem.

Speaker Bio: Steve Hoover is the founder of Redwood EDA, an early-stage startup focused on advanced silicon design methodology and tools. Steve is a former logic design lead for DEC, Compaq, and Intel and has extensive experience designing high-performance server CPUs and network switches.

System Requirements: All resources are free and online; no download or installation required. We will use Slack, Zoom, GitHub Classroom, and Makerchip.com.

Decision (Run/Cancel) Date for this Course is Wednesday, August, 25, 2021

IEEE Members	**$350**
Non-members	**$395**

http://ieeeboston.org/event/modern-applications-of-risc-v-cpu-design-course/?instance_id=2955

Software Development for Medical Device Manufacturers

Web-based Course with live Instructor!

(11 hours of instructions!)

Times & Dates: **Postponed until the fall 2021; Exact dates and times TBD**
Speaker: **Steve Rakitin, Software Qualtiy Consulting**
Course Format: Live Webinar, four, 3 hour sessions

COURSE SUMMARY: Developing software in compliance with the FDA Design Control regulation, changing FDA guidance documents and latest international standards is challenging. This intensive course provides practical solutions and suggestions for developing software in a manner that meets applicable FDA regulations, guidance documents and international standards, such as IEC-62304:2015. The focus is on interpreting Design Controls for software. Each section of the Design Controls regulation (820.30) is discussed from the perspective of software development. Discussions on key topics such as Software Requirements, Traceability, Design Reviews, Software Verification & Validation and Risk Management (including recently updated standards ISO-14971:2019 and EN-14971:2019) are included. Also discussed are FDA requirements for validation of software development tools and software used in Manufacturing and Quality Systems. Also discussed are recent FDA Guidance Documents on Cybersecurity, Mobile Apps, and Usability.

THIS COURSE IS INTENDED FOR: Software engineers, project managers, quality managers, software quality professionals, RA/QA staff, and anyone who needs to develop cost-effective processes and procedures that will enable their organizations to deliver high quality software-based medical devices that comply with FDA regulations and international standards. This course is also appropriate for people who are new to the medical device industry. Course notes, access to an extensive collection of reference documents and a training certificate are provided.

COURSE OUTLINE: This course will be presented with a live instructor using web-meeting software. The course content will be covered in 4 sessions as described below.

SESSION 1 – Regulatory Context
Duration ~3 hours with one 15 min break
This session will cover key regulatory requirements for medical device software in the US and EU.

Regulations and Guidance:
• FDA Medical Device Regulation (21 CFR Part 820 – specifically, design controls)
• EU Medical Device Regulation
• FDA Guidance Documents:
• Guidance for Content of Pre-market Submissions for Medical Devices Containing Software
• Off-the-Shelf Software Use in Medical Devices
• General Principles of Software Validation
• Content of Premarket Submissions for Management of Cybersecurity in Medical Devices
• Policy for Software Device Functions and Mobile Medical Applications
• Applying Human Factors and Usability Engineering to Medical Devices

International Standards:
• ISO 13485:2016 Medical Devices – Quality Management Systems
• IEC 62304: 2015 Medical Device Software – Software Lifecycle Processes
• ISO 14971: 2019 Application of Risk Management to Medical Devices

• EN 14971: 2019 Application of Risk Management to Medical Devices
• Off-the-Shelf (OTS) Software and Open Source software (SOUP)
• Discussion: All Software Is Defective…

SESSION 2 – FDA Design Controls and IEC 62304 – Part 1
Duration ~2.5 hours with one 15 min break
This session will cover FDA Design Controls and IEC 62304 requirements for medical device software.

• Design and Development Planning
    • How does Agile Development fit?
    • Medical Device Software Lifecycle Processes
• Risk Management
    • FDA Levels of Concern
    • IEC 62304 Software Safety Classification
• Software Requirements
    • Techniques for Removing Ambiguity from Requirements
• Software Architecture and Design
• Software Design Changes

SESSION 3 – FDA Design Controls and IEC 62304 – Part 2
Duration ~2.5 hours with one 15 min break
This session will cover Software Verification and Validation requirements.

• Software Implementation
• Software Verification
    • Technical Reviews
    • Static Analysis
    • Unit and Integration Testing
• System Testing
• Software Validation Testing

SESSION 4 – Software Tool Validation and Risk Management
Duration ~2.5 hours with one 15 min break
This session will cover Software Tool Validation and Risk Management requirements.
• Software Tool Validation
    • Deciding which tools need to be validated
    • Validation approach for software tools
• Validation of Manufacturing Software and Quality System Software
• Risk Management Using Fault Tree Analysis (FTA)
    • Review of ISO/EN 14971:2019 Requirements
    • Example of Fault Tree Analysis and Failure Modes Effect Criticality Analysis (FMECA)

About the instructor: Steven R. Rakitin has over 45 years experience as a software engineer. He has over 30 years of experience in the medical device industry and has been a medical device consultant for over 20 years. He has worked with over 100 medical device manufacturers and biotech companies worldwide, from startups to Fortune 100 corporations. He has published papers on medical device software risk management as well as a book titled: Software Verification & Validation for Practitioners and Managers.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE.

Steve works collaboratively with medical device companies to help them comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

Decision (Run/Cancel) Date for this Course is TBD

IEEE Members	**$285**
Non-members	**$345**

http://ieeeboston.org/event/live-course-software-development-for-medical-device-manufacturers/

Call for Course Speakers/Organizers

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity. The IEEE Boston Section, its dedicated volunteers, and over 8,500 members are committed to fulfilling this core purpose to the local technology community through chapter meetings, conferences, continuing education short courses, and professional and educational activities.

Twice each year a committee of local IEEE volunteers meet to consider course topics for its continuing education program. This committee is comprised of practicing engineers in various technical disciplines. In an effort to expand these course topics for our members and the local technical community at large, the committee is publicizing this CALL FOR COURSE SPEAKERS AND ORGANIZERS.

The Boston Section is one of the largest and most technically divers sections of the IEEE. We have over 20 active chapters and affinity groups.
If you have an expertise that you feel might be of interest to our members, please submit that to our online course proposal form on the section's website (www.ieeeboston.org) and click on the course proposal link (direct course proposal form link is **http://ieeeboston.org/course-proposals/** . Alternatively, you may contact the IEEE Boston Section office at ieeebostonsection@gmail.com or 781 245 5405.

- **Honoraria can be considered for course lecturers**
- Applications oriented, practical focused courses are best (all courses should help attendees expand their knowledge based and help them do their job better after completing a course
- Courses should be no more than 2 full days, or 18 hours for a multi-evening course
- Your course will be publicized to over 10,000 local engineers
- You will be providing a valuable service to your profession
- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

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IEEE Boston Section is the largest, most active, and technically diverse section in the U.S.
Comprised of Engineers, scientists and professionals in the electrical and computer sciences and engineering industry

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- **August 18:** Radar/Automotive/SATCOM
- **August 25:** Signal Integrity/Power Integrity

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A Note from the HPEC Committee:
IEEE HPEC 2021 will be presented as a virtual conference that will allow safe participation and full publication in IEEE Xplore.

The IEEE High Performance Extreme Computing Conference (HPEC '21) will be held in the Greater Boston Area, Massachusetts, USA on 21 – 23 September 2021. The HPEC charter is to be the premier conference in the world on the confluence of HPC and Embedded Computing.

The technical committee seeks new presentations that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- AI / Machine Learning
- Graph Analytics & Network Science
- Advanced Multicore Software Technologies
- Advanced Processor Architectures
- Automated Design Tools
- Big Data & Distributed Computing
- Big Data Meets Big Compute
- Case Studies & Benchmarking of Applications
- Cloud HPEC
- Computing Technologies for Challenging Form Factors
- ASIC & FPGA Advances
- Quantum and Non-Deterministic Computing
- Data Intensive Computing
- Digital Front Ends
- Fault-Tolerant Computing
- Embedded Cloud Computing
- General Purpose GPU Computing
- High Performance Data Analysis
- Interactive and Real-Time Supercomputing
- Mapping & Scheduling of Parallel & Real-Time Applications
- New Application Frontiers
- Open System Architectures
- Cyber Analysis and Secure Computing

HPEC accepts two types of submissions:	**IMPORTANT DATES**:
1. Full papers (up to 6 pages, references not included; additional pages can be purchased for $200/page). 2. Extended abstracts (up to 2 pages, references included).	Submission Deadline: **JUL 9, 2021** Notification of Acceptance: **AUG 13, 2021** Camera Ready Deadline: **AUG 31, 2021**

Preference will be given to papers with strong, quantitative results, demonstrating novel approaches or describing high quality prototypes. Authors of full papers can mark their preference for a poster display or an oral presentation. Presenters who wish to have hardware demonstrations are encouraged to mark their preference for a poster display. Accepted extended abstracts will be displayed as posters. Papers can be declared "student paper" if the first author was a student when doing the presented work, and will be eligible for the "IEEE HPEC Best Student Paper Award." Papers should not be anonymized. All paper and extended abstract submissions need to use the approved IEEE templates. Full paper submissions with the highest peer review ratings will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions and extended abstracts are published on ieee-hpec.org.

Vendors are encouraged to sign up for vendor booths. This will allow vendors to present their HPEC technologies in an interactive atmosphere suitable for product demonstration and promotion. We welcome input (hpec@ieee-hpec.org) on tutorials, invited talks, special sessions, peer reviewed presentations, and vendor demos. Instructions for submitting will be posted on the conference web site shortly.

HPEC 2021