# **BOSTON**

# THE REFLECTOR





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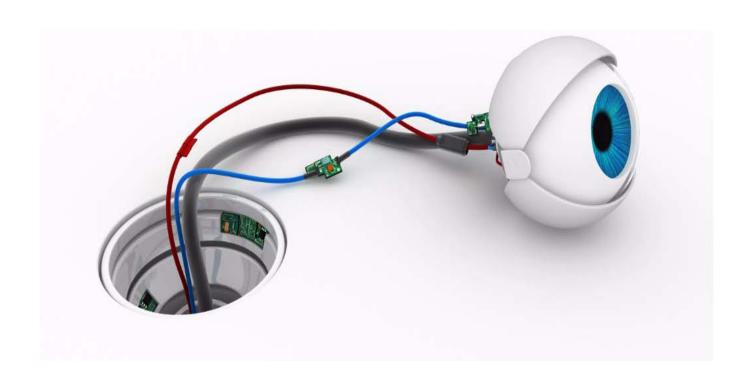
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# IEEE Senior Member Grade Elevation: Your New Year's Resolution

By Marie Tupaj, 2021 Chair, IEEE Boston Section

The first time I thought about Senior Membership was in 2013 at an IEEE WIE Boston planning committee meeting at the Fresh Pond Panera Bread in Cambridge. That evening, the committee started discussing the application process and which Senior Members they could ask for a reference (more about references later). As I thought about the application process and started counting my years of experience that are needed in the profession to become a Senior Member, I thought, I really don't have the required ten years of engineering work experience; I spent time out of the industry, changed my engineering field of work, and pursued a graduate degree, so I am not going to apply now. Despite the WIE Committee trying to convince me, I put off applying.

Years of local IEEE senior member grade elevation meetings passed, more colleagues pursued Senior Membership and I still did not apply. I was just fine with my professional member status. I continued to volunteer in IEEE, spending a year as WIE Boston chair, two years as an IEEE Boston Excom member-at-large, and I was inducted as a professional member into IEEE's international honor society, Eta-Kappa-Nu. In late 2018, I was approached to serve as the IEEE Boston treasurer. By agreeing to serve as IEEE Boston treasurer, it is presumed that you will serve as the section's vice-chair the following year, and will be nominated for the chair position the following year. As I started thinking about my past and future commitment to IEEE, I thought about elevating my membership grade to Senior Member. This would demonstrate a commitment to IEEE and present as a career honor on my CV and resume. Furthermore, how can I advocate and promote others to Senior Membership if I did not apply myself? Yet, I dragged my feet on the application somehow thinking I will have more free time the following year to work on it. Sigh, another excuse. When I was approached in the fall of 2020 and asked if I would serve as the 2021 IEEE Boston chair, I said, yes. Two days later, I remembered that I still hadn't applied for Senior Membership.

By now, you may be thinking, what are the requirements for Senior Membership? The general answer is that Senior Members have worked in an IEEE designated field for at least ten years and they have demonstrated significant work performance for at least five of those years. At this point, I had moved on from counting my years in the profession to trying to figure out what I could use as five years of significant work performance.

Yet, thinking about those answers didn't matter much anymore. I had put off the senior membership elevation application for so long that at this point they were either going to accept me or not. So, I started by clearing my schedule and ordering food out. Applications never get far on an empty stomach. Next, I began looking into the process and reading the requirements for Senior Membership that were located on the IEEE Boston website (http://ieeeboston.org/membership-development/ member-grade-elevation/). This is the IEEE Boston's Senior Member Guide. As I started to read, I began to feel better when I learned that significant work performance could be as simple as leading a work team or contributing to a patent or publication. In addition, the professional positions that are approved as IEEE designated fields, which qualify towards work experience for Senior Members, are broad and include many different types of work. Finally, years of work experience does not need to be consecutive and graduate school

counts towards these years. I finished the meal, turned on music, and opened up my workspace. I thought, well at least I have the time now - there aren't many places that I want to go during a pandemic. After working a few hours each day over the next couple of days updating my CV, contacting references, and talking with other Senior Members about member grade elevation, I learned some tips about the process.

- 1. First Identify Three IEEE Senior Members for References. Select your references carefully as changing references once your application is submitted is a hassle. To identify references, the IEEE Boston holds senior member grade elevation clinics each year where Senior Members are present and willing to write references (They will also provide overall guidance on the process). Alternatively you can search for Senior Members on IEEE Collabratec (https://ieee-collabratec.ieee.org). Emailing our local chapter can also help assist you with leads.
- 2. Use the CV template provided in the IEEE Boston Senior Member Guide. Using the CV template will make your qualifications for Senior Member clear to the reviewers. Also, with examples provided in each section of the template, you won't forget to include something when putting your CV together. Overall, it prevents your application from accidently heading into the "maybe" pile.
- **3. Track your application status online**. Once your application is submitted, your references will be contacted. You will receive notification after each reference

is submitted. To ensure your application was received and to find out the next review date, IEEE has a Senior Member Application Status Website (https://mga.ieee.org/membership-development/senior-member-program-volunteer-resources/status-of-senior-member-applications). Notice of your elevation grade will come shortly afterwards.

Within three weeks after submitting my application, I received an email in my inbox that my Senior Membership was approved. I couldn't believe it was that easy. I thought why didn't I do this earlier? The benefits for a Senior Member include peer recognition, society leadership eligibility, a letter of commendation sent to your employer (if requested), and a voucher to join a new IEEE society. Also, having the ability to add IEEE Senior Member on your resume is helpful. At my last job interview, a search committee member noticed on my resume that I was an IEEE member. He told me he was an IEEE Life Member. I was able to talk to him about the recent Life Members Meeting. Listing an IEEE professional membership on my resume was a way of connecting with someone that was hiring that I didn't know previously. I think it helped - I received a job offer.

If you are thinking of applying for a senior member grade elevation and have questions, send us an email at (ieeebostonsection@gmail.com). You can also go straight to the website at <a href="https://www.ieee.org/membership/senior/">https://www.ieee.org/membership/senior/</a>. We are here for you. While at home waiting for the pandemic's end, now is the time. Make it a New Year's resolution!

# **IEEE Boston Section Social Media Links:**

Twitter: https://twitter.com/ieeeboston

Facebook: https://www.facebook.com/IEEEBoston

YouTube: https://www.youtube.com/user/IEEEBostonSection

LinkedIn: https://www.linkedin.com/groups/IEEE-Boston-Section-3763694/about

# **IEEE Boston Section Online Courses:**

(Students have 90 day access to all online, self-paced courses)

# **Verilog101:Verilog Foundations**

Full course description and registration at , http://ieeeboston.org/verilog-101-verilog-foundations-online-course/

# **System Verilog 101: Design Constructs**

Full course description and registration at , http://ieeeboston.org/systemverilog-101-sv101-design-constructs-online-course/

# **System Verilog 102: Verification Constructs**

Full course description and registration at , http://ieeeboston.org/systemverilog-102-sv102-verification-constructs-online-course/

# **High Performance Project Management**

Full course description and registration at , http://ieeeboston.org/high-performance-project-management-online-course/

# Introduction to Embedded Linux Part I

Full course description and registration at , http://ieeeboston.org/introduction-to-embedded-linux-part-i-el201-online-course/

# **Embedded Linux Optimization - Tools and Techniques**

Full course description and registration at , http://ieeeboston.org/embedded-linux-optimization-tools-techniques-line-course/

# Embedded Linux Board Support Packages and Device Drivers

Full course description and registration at , http://ieeeboston.org/embedded-linux-bsps-device-drivers-line-course/

# **Software Development for Medical Device Manufacturers**

Full course description and registration at , http://ieeeboston.org/software-development-medical-device-manufacturers-line-course/

# **Fundamental Mathematics Concepts Relating to Electromagnetics**

Full course description and registration at , http://ieeeboston.org/fundamental-mathematics-concepts-relating-electromagnetics-line-course/

# Reliability Engineering for the Business World

Full course description and registration at , http://ieeeboston.org/reliability-engineering-business-world-line-course/

# **Design Thinking for Today's Technical Work**

http://ieeeboston.org/design-thinking-technical-work-line-course/

# **Fundamentals of Real-Time Operating Systems**

http://ieeeboston.org/fundamentals-of-real-time-operating-systems-rt201-on-line-course/



The goal of this monthly webinar series is to provide a pulpit to experts in the Artificial Intelligence field to present their expertise and knowledge to other technologists, engineers and scientists.

# **Confirmed Speakers Include:**



Vinton G. Cerf President & Chief Internet Evangelist of Google



Manuela M. Veloso, Head of J.P. Morgan Al Research



Alton D. Romig, Jr. Executive Officer of the National Academy of Engineering



Steve Wozniack, Co-Founder, Apple Computer



David Cox, IBM Director of the MIT-IBM Watson Al Lab



Helen Greiner, Co-Founder, iRobot

# Dates:

Monthly Webinar Series beginning January 21, 2021 with Session 1:

Does AI Mean Artificial Intelligence or Artificial Idiocy?

and

Birds vs. Drones: Real vs. Artificial Intelligence

# Time:

12:00PM - 1:30PM (ET)

# Cost:

IEEE Members: \$25. Non-members: \$35. Entrepreneurs' Network – 5:30PM, Tuesday, January 5

# How to Build your Product on Time and in Budget

Location: Webinar

(Please note capacity is limited, so pre-registration is necessary)

## Register:

https://boston-enet.org/event-3892659/Registration

You have validated your idea, built a team, and have funding. This session will focus on expeditiously bringing your product to market cost-effectively. Core topics will include; User Experience, Design Segmentation, Quality Assurance, and Performance and Scalability Testing. Whatever product you are building, the User Experience defines its acceptance. Customers expect the product's technology to work and count on the interface to make it easy to use and delight their employees. The panel will discuss converting UX requirements into exceptional product experiences.

Design Segmentation will review what parts of the system perform different functions, the trade-off between hardware and software solutions. Does the solution contain IP which must be developed in-house, or could the IP be purchased or subcontracted? The panel will discuss these topics and what are the best of class design methodologies today?

Quality is job 1, closely followed by scalability and performance. It is one thing to produce Proof Of Concept and Prototype quantities. It is entirely different to build mass production quantities or support tens of thousands of Users. The panel will discuss creating and testing quality early in the product development cycle. The importance of regression testing and revision control to enable quick problem resolution and product quality.

### Agenda:

5:30 – 6:45 – Networking on Grapevine.today 7:00 - 7:10 PM - ENET Chairperson's announcements 7:10 - 7:25 PM – <u>eMinute Pitch</u> - Up to 3 Startup

companies' presentations

7:25 - 8:10 PM - 3 expert speakers on the night's topic 8:10 - 8:30 PM – Moderator and Audience Q & A with the speakers

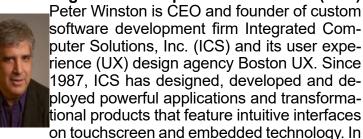
8:30 – 9:00 PM - Networking on Grapevine.today (all times are USA Eastern Daylight time)
A question and answer session will follow the panel

discussion, and panelists will be available afterward for responses to individual questions.

### **Panel Members**

### **Peter Winston**

CEO - Integrated Computer Solutions (ICS)



the past five years, Winston has evolved the company to encompass other leading-edge technologies, including machine learning and robotics, and voice and gesture recognition to fuel growth. Today, the global company excels in the areas of embedded, desktop, mobile, and IoT development and UX design, and has developed everything from regulated medical devices to commercial restaurant equipment. Customers include Fortune 1000 companies like Boeing and Intel, as well as small and midsize firms looking to disrupt their industries.

https://www.linkedin.com/in/peterwinston/

# Anupam Koul, Board President Envisage, Inc. Envisage, Inc...caring delivery of superior solutions (TM)



Anupam is an entrepreneur, investor, adviser, mentor and hands-on business operator. His background includes an interesting mix of product development and professional services. He has helped build and deploy many successful global products and technologies, as well as built more than one best-in-class

global professional services and engineering businesses from the ground-up. Currently, Anupam is a board member at Cultivate Care Farms, and is President of the Board at Envisage where he is tasked with being a strategic advisor to the CEO.

Envisage is a trusted partner to many clients for delivering on complex technology solutions. Our resources provide hands on expertise and strategic consultation that enable firms to complete projects efficiently and more effectively. For more than a decade now, we have demonstrated our expertise and proven our capability through a passion for delivering quality solutions, outcome certainty and transparency to our partners. Specialties: Information Technology, Enterprise Software, Implementations, Integration, Data, Business Intelligence, Cloud Modernization, Product Development, Embedded Systems & Hardware. Values: Quality, Integrity, Transparency, Consistency, Hard Work & Service

https://www.linkedin.com/in/anupamkoul/

# Laura Tenney, Director of Software Engineering Dell Technologies |Storage Products

Laura is an experienced engineering leader who enjoys developing and leading high-performing organizations, with a focus on strategic process improvements and on-going team development. With 30 years of experience in the industry, Laura has been a leader in software companies that range from startups to

multinational businesses such as Xerox and McKesson, and worked in markets that include networking, workforce management, optical character recognition, and health care. Laura enjoys driving positive change, solving challenging problems, and building products that meet or

exceed customer expectations. Currently Laura is helping lead the development of the first hardware independent containerized UFS64 File System at Dell Technologies where she has been working for the past 6 years. <a href="https://www.linkedin.com/in/laura-tenney-1bb1a61/">https://www.linkedin.com/in/laura-tenney-1bb1a61/</a>

# Organizer and Moderator:

Dan Skiba, Managing Director Skiba Advisory Associates, VP Printed Electronics Chasm Advanced Materials, Vice-Chair Meetings Boston ENET



As a Product Development Company Executive, I provide strategic leadership in product innovation and managing global teams, delivering award-winning products to the international market. My ability to problem solve, direct the entire product development lifecycle, and gain commitment to a common

goal have driven faster release of products and market penetration. By building synergies across all Product Life Cycle disciplines, we have delivered products that result in 100% product utilization and seamless integration into customer environments. My skills in optimizing international resources have significantly reduced costs and streamlined production, delivering product excellence. <a href="https://www.linkedin.com/in/dtskiba/">https://www.linkedin.com/in/dtskiba/</a>

# **IEEE Boston Section Excom Member Recipient of IEEE-USA Award**



Karen Panetta IEEE Boston Section Reflector Editor, is the 2020 recipient of the IEEE-USA Award for Distinguished Literary Contributions Furthering Public Understanding and the Advancement of the Engineering Profession "For co-authorship of the book, "Count Girls In", which serves as an inspiration for youth to pursue tech-

nology careers, and for lifelong commitment to STEM Literacy." You have honored IEEE with your contributions and services in the area of professional activities, and the IEEE-USA Board of Directors is very pleased to recognize your efforts.

Karen Panetta received a B.S. in Computer Engineering from Boston University, and a M.S. and Ph.D. in Electrical Engineering from Northeastern University. As the first female electrical engineer to be given tenure in the Electrical and Computer Engineering department, Panetta continues to promote the interests of women

in her field. From 2007 to 2009, she was the worldwide director for IEEE Women in Engineering, the largest international professional organization dedicated to promoting women engineers and scientists, and she served as editor-in-chief of the IEEE Women in Engineering magazine. She is the faculty adviser to the Tufts student chapters of both the Society of Women Engineers and the IEEE, and is founder of the nationally acclaimed Nerd Girls program, which promotes engineering disciplines to young students.

She is a fellow of the Institute of Electrical and Electronics Engineers (IEEE) and was awarded the 2013 IEEE Award for Distinguished Ethical Practices for exemplary contributions and leadership in developing ethics and social responsibility in students. She has received several NASA and National Science Foundation research grants, including the NSF CAREER Award. In 2011, President Barack Obama awarded Panetta the Presidential Award for Science and Engineering Education and Mentoring.

Robotics and Automation Society - 6:00 PM ET, Wednesday, January 13

# **Enabling Complexity in Soft Robotics: Manufacturing and Control of Multi-Scale Systems**

Speaker: Prof. Tommaso Ranzani, Boston University

**Meeting Location:** Zoom Meeting (online)

**Register here:** <a href="https://www.eventbrite.com/e/en-abling-complexity-in-soft-robotics-tickets-132968872477">https://www.eventbrite.com/e/en-abling-complexity-in-soft-robotics-tickets-132968872477</a>

The talk will be followed by the **2021 Chapter Elections**.



Soft robots are constructed from compliant materials, resulting in machines that can safely interact with natural environments. Given their inherent compliance, they are particularly suitable for exploring and interacting with unstructured environments, and manipulating soft, delicate, and irregular ob-

jects. These properties make soft robots promising for biomedical applications, such as wearable and medical devices. While they can be low cost and easy to manufacture, soft robots can also be difficult to control due to their typical reliance on external pressure sources that can become bulky as more degrees of freedom are introduced to the robot.

During this talk, I will describe progress in soft robotics and its potential for revolutionizing biomedical devices. I will introduce a soft manipulator inspired by the structure and the manipulation capabilities of the octopus tentacle, which is able to selectively tune its stiffness. I will introduce the potential of soft robotics at the millimeter and micrometer scales, addressing the challenge of

manufacturing complex mesoscale three-dimensional soft structures using two-dimensional processes involving laser machining, lamination, and soft lithography. These manufacturing processes could pave the way for soft microrobots as well as a new class of deployable, small, and safe medical devices. Ultimately, I will discuss challenges and opportunities in controlling soft multi-DOF robots focusing on the integration of onboard flow-control components.

Tommaso Ranzani is an Assistant Professor in the Department of Mechanical Engineering, Biomedical Engineering, and in the Division of Materials Science and Engineering at Boston University. He received a Bachelor's and Master's degree in Biomedical Engineering from the University of Pisa, Italy. He did his Ph.D. at the BioRobotics Institute of the Sant'Anna School of Advanced Studies and he joined the Wyss Institute for Biologically Inspired Engineering at the Harvard John A. Paulson School of Engineering and Applied Sciences as a postdoctoral fellow in 2014.

At Boston University, he founded the Morphable Biorobotics Lab. The lab focuses on expanding the potential of soft robots across different scales to develop novel reconfigurable soft-bodied systems with applications ranging from environmental exploration to assistive and surgical soft robots.

Computer Society and GBC/ACM, 7:00PM, Thursday, January 14

# SARS-CoV-2 Gene Content and COVID-19 Mutation Impact by Comparing 44 Sarbecovirus Genomes

Where: On-Line

Irwin Jungreis and Manolis Kellis

Register in advance for this webinar at <a href="https://acm-org.zoom.us/webinar/register/4616072161581/WN\_y8w-vok4XTM62W0Q3mji2-w">https://acm-org.zoom.us/webinar/register/4616072161581/WN\_y8w-vok4XTM62W0Q3mji2-w</a>

After registering, you will receive a confirmation email containing information about joining the webinar.

Despite its overwhelming clinical importance, the SARS-CoV-2 gene set remains unresolved, hindering dissection of COVID-19 biology. Here, we use comparative genomics to provide a high-confidence protein-coding gene set, characterize protein-level and nucleotide-level evolutionary constraint, and prioritize functional mutations from the ongoing COVID-19 pandemic. We select 44 complete Sarbecovirus genomes at evolutionary distances ideally-suited for protein-coding and non-coding element identification, create whole-genome alignments, and quantify protein-coding evolutionary signatures and overlapping constraint. We find strong protein-coding signatures for all named genes and for 3a, 6, 7a, 7b, 8, 9b, and also ORF3c, a novel alternate-frame gene. By contrast, ORF10 and overlapping-ORFs 9c lack protein-coding signatures.

Furthermore, we show no other conserved protein-coding genes remain to be discovered. Cross-strain and within-strain evolutionary pressures largely agree at the gene, amino-acid, and nucleotide levels, with some notable exceptions, including fewer-than-expected mutations in nsp3 and Spike subunit S1, and more-than-expected mutations in Nucleocapsid. The latter also shows a cluster of aminoacid-changing variants in otherwise-conserved residues in a predicted B-cell epitope, which may indicate positive selection for immune avoidance. Several Spike-protein mutations, including D614G, which has been associated with increased transmission, disrupt otherwise-perfectlyconserved amino acids, and could be novel adaptations to human hosts. The resulting high-confidence gene set and evolutionary-history annotations provide valuable resources and insights on COVID-19 biology, mutations, and evolution.

After obtaining a PhD in pure math from Harvard University, Irwin Jungreis embarked on a 17-year career as a

software engineer, manager, executive, and entrepreneur in the Computer Aided Design software industry. Inspired by Darwin's "On the Origin of Species", he decided to leave the software industry behind and become a biologist. While filling the gaps in his biological education, he encountered Manolis Kellis's

computational biology class at MIT, where he fell in love with the idea of using the imprint of evolution to reveal the secrets of molecular biology. He joined the Kellis lab as a Research Scientist, where he has worked for the last eleven years, with a focus on using evolutionary signatures to detect novel protein-coding genes and unusual cases of protein translation, including stop codon readthrough.

Manolis Kellis is a Professor of Computer Science at MIT, an Institute Member of the Broad Institute of MIT and Harvard, and a member of the Computer Science and Artificial Intelligence Lab at MIT where he directs the MIT Computational Biology Group (compbio.mit.edu). He has helped direct several large-scale

genomics projects, including the NIH Roadmap Epigenomics project, the comparative analysis of 29 mammals, the Encyclopedia of DNA Elements (ENCODE) project, and the Genotype Tissue-Expression (GTEx) project. He received the US Presidential Early Career Award in Science and Engineering (PECASE), the NSF CAREER award, the Alfred P. Sloan Fellowship. He obtained his Ph.D. from MIT, where he received the Sprowls award for the best doctorate thesis in computer science. He lived in Greece and France before moving to the US.

This joint meeting of the Boston Chapter of the IEEE Computer Society and GBC/ACM will be online only due to the COVID-19 lockdown.

Up-to-date information about this and other talks is available online at https://ewh.ieee.org/r1/boston/computer/.

You can sign up to receive updated status information about this talk and informational emails about future talks at <a href="https://mailman.mit.edu/mailman/listinfo/ieee-cs">https://mailman.mit.edu/mailman/listinfo/ieee-cs</a>, our self-administered mailing list.

Entrepreneurs' Network - 5:30PM, Tuesday, January 19

# How to successfully Sell in a Pandemic Economy

Location: Webinar

Register: https://boston-enet.org/event-3892675 (Please note capacity is limited, so pre-registration is necessary)

The COVID-19 pandemic has changed the business world in 2020 and likely continue well into 2021. We know that sales organizations have on the top of their minds, especially entrepreneurs, how do I sell more. In a world without Tradeshows, without face-to-face meetings; how do you generate leads, convert these leads to opportunities, and ultimately to Purchase Orders.

We are featuring Jack Derby, Mass High Tech All-Star, co-founder of 9 companies, an investor in 54 companies, and Professor of Entrepreneurship. Bring your questions, your startup challenges, and learn the steps required to drive your startup success.

## Agenda:

5:30 – 6:45 – Networking on Grapevine.today

7:00 - 7:10 PM - ENET Chairperson's announcements 7:10 - 7:25 PM - <u>eMinute Pitch</u> - Up to 3 Startup companies' presentations

7:25 - 8:10 PM - Jack Derby

8:10 - 8:30 PM - Moderator and Audience Q & A with the Jack Derby

8:30 – 9:00 PM - Networking on Grapevine.today (all times are USA Eastern Daylight time)

A question and answer session will follow the panel discussion, and panelists will be available afterward for responses to individual questions.

# Jack Derby, Director, Tufts Entrepreneurship Center, Cummings Family Professor of Entrepreneurship



Jack is responsible for the Tufts University Entrepreneurship Center. He teaches two courses and manages a highly engaged and active center of professors and students, constituting the largest minor on campus. The Center hosts 20+ entrepreneurship events each year, culminating in the \$100K New Ven-

tures Competition ranked by Forbes as one of the leading

university competitions in the U.S. Jack is passionate about Tufts and its students and has received the <u>Henry and Madeline Fisher Award</u> voted by the students as the most highly ranked teacher on campus.

Prior to forming a management consulting firm, Jack served as CEO of Mayer Electronics, President of CB Sports, President of Litton Industries Medical Systems, CEO of Datamedix, and President of Becton Dickinson Medical Systems. For his work as an entrepreneur, cofounding nine companies, Jack was named to Mass High Tech's All-Star Team. He received the Pro Bono Publico award from the Smaller Business Association of New England, the Meritorious Service Award from the Association for Corporate Growth, and the Vincent Fulmer Distinguished Service Award from the MIT Enterprise Forum where he served as Chairman.

He's an active board member in several companies and with a long investing history as an early-stage investor as General Partner at Kestrel Ventures, Chairman of Common Angels, and a General Partner at Converge Ventures. <a href="https://www.linkedin.com/in/jackderby/">https://www.linkedin.com/in/jackderby/</a>

# Organizer:

Dan Skiba, Managing Director Skiba Advisory Associates, VP Printed Electronics Chasm Advanced Materials, Vice-Chair Meetings Boston ENET



As a Product Development Company Executive, I provide strategic leadership in product innovation, and managing global teams, delivering award-winning products to the international market. My ability to problem solve, direct the entire product development lifecycle, and gain

commitment to a common goal have driven faster release of products and market penetration. By building synergies across all Product Life Cycle disciplines, we have delivered products that result in 100% product utilization and seamless integration into customer environments. My skills in optimizing international resources have significantly reduced costs and streamlined production, delivering product excellence.

https://www.linkedin.com/in/dtskiba/

Computer Society, GBC/ACM and BostonCHI, 7:00PM, Thursday, January 21

# The UX Leaders' Secret Guide to Innovative, UX-Driven Product Roadmaps

Jared M. Spool, Maker of Awesomeness at Center Centre - UIE

Where: Online only this year via Zoom

Informal networking via virtual whiteboard and Zoom coordinated by BostonCHI at 6:30 pm

[Admission is free, but you must register at <a href="https://jared-spooljan2021.eventbrite.com/?aff=ieeeboston">https://jared-spooljan2021.eventbrite.com/?aff=ieeeboston</a>]

Most UX professionals feel that they're at the mercy of their organization's product roadmaps. They're on the receiving end of decisions about what the team is building and when they're building it. These decisions are often not informed by their products' users' true needs. Instead, the decisions are driven by the stakeholders' beliefs that they must match competitive offerings.

The result is that UX teams are constrained to researching and designing in far too short a time period, where the problem isn't identified and the nature of the solution isn't well understood. They subsequently struggle to deliver what they believe to be the best possible product or service, feeling like they've busted their butts to only achieve mediocre results.

In this presentation, Jared will share the secrets that successful UX leaders have employed to take control of their product roadmap. You'll see what it takes to escape the misery of reactive UX practices by integrating key user research and design efforts directly into the roadmap planning process. You'll discover how UX leaders can work closely with their partners in product management to increase their organization's delivery of innovative products and services.

Jared M. Spool is a Maker of Awesomeness at Center Centre - UIE.



If you've ever seen Jared speak about user experience (UX) design, you know that he's probably the most effective and knowledgeable communicator on the subject today. He started working in the field of usability and user experience in 1978, before the terms "usability" and "UX" were ever associated with computers.

While he led UIE, the industry research firm he started in 1988, the field of UX design emerged and Jared helped define what makes UX designers successful all over the world. UIE's world-class research organization produces conferences and workshops all over the world and for companies in every industry.

In 2016, with Dr. Leslie Jensen-Inman, he opened Center Centre, a new school in Chattanooga, TN to create the next generation of industry-ready UX Designers. They created a revolutionary approach to vocational training, infusing Jared's decades of UX experience with Leslie's mastery of experience-based learning methodologies. UIE joined forces with Center Centre and now delivers the best professional development workshops, masterclasses, and conference in the UX Design industry.

For 23 years, he was the conference chair and keynote speaker at the now retired annual UI Conferences and UX Immersion Conferences, and he manages to squeeze in a fair amount of writing time. He is a co-author of Web Usability: A Designer's Guide and Web Anatomy: Interaction Design Frameworks that Work.

You'll find his writing at <u>uie.com</u>. You can also follow his adventures on the Twitters at @jmspool, where he tweets daily about UX design, design strategy, design education, and the wondrous customer service habits of the airline industry.

This meeting will be held online only due to the ongoing pandemic. Up-to-date information about this and other talks is available online at

https://ewh.ieee.org/r1/boston/computer/. You can sign up to receive updated status information about this talk and informational emails about future talks at

https://mailman.mit.edu/mailman/listinfo/ieee-cs, our self-administered mailing list.

For more information contact Peter Mager (p.mager at computer.org)

Microwave Theory and Techniques Society - 6:30PM, Tuesday, January 26

# Design of Wideband, On-board THz Interconnects, Circuits and Sensors Using Additive Manufacturing

Speaker: Dr. Jennifer Byford, MIT Lincoln Laboratory

Where: Webinar

Current trends in data consumption are driving a need to further increase the rate and bandwidth at which common electrical devices transmit data. Many solutions have been proposed using optical and electrical interconnects to address this problem but an ideal solution has yet to be realized. This is primarily due to optical interconnects inherent latency in needing to convert between electrical and optical signals, and because electrical solutions either suffer from metal losses, crosstalk, or narrow bandwidth. In this work an ultra-wideband waveguide design is proposed as a possible solution to address this need that combines the design of a traditional metal waveguide and that of a dielectric ribbon waveguide. This new design is enabled by advances in additive manufacturing.

Theoretical analysis, simulations, fabrication, and measured results are presented for waveguides of both a circular and rectangular cross-section. Theoretical expressions have been derived by hand and results found numerically using Python. Simulations were performed using finite element tool ANSYS Electronics Desktop HFSS to create and simulate waveguide models. Fabrication processes used here have utilized 3D printed

plastics to quickly and inexpensively create prototypes, and a frequency domain THz system was used to measure devices. Results show low-loss transmission up to 0.5 THz. This work has implications for future integrated circuits ability in meeting the data transmission needs of the future and applications for passive THz components, sensors, antennas and transmission line circuits are explored.

Jennifer is a member of the Technical Staff at MIT Lincoln Laboratory in the Advanced SATCOM Systems and Operations group. She earned her Ph.D. in Electrical Engineering in 2018 from Michigan State University under Dr. Premjeet Chahal in the Terahertz Systems Laboratory (TeSLa) and her Bachelor's degree in Electrical Engineering from Michigan State University in 2013. Her research interests include metamaterials, millimeter/terahertz active and passive devices, adaptive antennas and sensors, biomedical applications for terahertz, and engineering education.

Registration and webinar link: https://events.vtools.ieee.org/m/250951

# Introduction to Practical Neural Networks and Deep Learning (Part I)

Times and Dates: 9:00AM - 12:15PM, Saturday, March 20, 2021

(3 hours of instructions!)

Speaker: CL Kim

Location: A live, interactive webinar

### **Overview:**

From the book introduction: "Neural networks and deep learning currently provides the best solutions to many problems in image recognition, speech recognition, and natural language processing."

This Part 1 and the planned Part 2 (late spring/early summer 2021, to be confirmed) series of courses will teach many of the core concepts behind neural networks and deep learning.

### Reference book:

"Neural Networks and Deep Learning" by Michael Nielsen, http://neuralnetworksanddeeplearning.com More from the book introduction: "We'll learn the core principles behind neural networks and deep learning by attacking a concrete problem: the problem of teaching a computer to recognize handwritten digits. ...it can be solved pretty well using a simple neural network, with just a few tens of lines of code, and no special libraries." "But you don't need to be a professional programmer." The code provided is in Python, which even if you don't program in Python, should be easy to understand with just a little effort.

## Benefits of attending the series:

- \* Learn the core principles behind neural networks and deep learning.
- \* See a simple python program that solves a concrete problem: teaching a computer to recognize a handwritten digit.

- \* Improve the result through incorporating more and more of core ideas about neural networks and deep learning.
- \* Principle-oriented, with worked-out proofs of fundamental equations of backpropagation for those interested.
- \* Yet hands-on practical, with simple code examples.

# **Course Background and Content:**

This is a live instructor-led introductory course on Neural Networks and Deep Learning. It is planned to be a two-part series of courses. The first course is complete by itself. It will be a pre-requisite for the planned second course. The class material is mostly from the highly-regarded and free online book "Neural Networks and Deep Learning" by Michael Nielsen, plus additional material such as some proofs of fundamental equations not provided in the book, and (in planned Part 2) touching on more recent neural network types such as ResNet

### **Agenda**

Introduction to Practical Neural Networks and Deep Learning (Part 1)

Feedforward Neural Networks.

- \* Simple (Python) Network to classify a handwritten digit
- \* Learning with Gradient Descent
- \* How the backpropagation algorithm works
- \* Improving the way neural networks learn:
- \*\* Cross-entropy cost function

- \*\* Softmax activation function and log-likelihood cost function
- \*\* Rectified Linear Unit
- \*\* Overfitting and Regularization:
- \*\*\* L2 regularization
- \*\*\* Dropout
- \*\*\* Artificially expanding data set
- \*\*\* Hyper-parameters

Introduction to Practical Neural Networks and Deep Learning (planned Part 2, to be confirmed) Convolutional Neural Networks.

\* Local receptive field, Feature map. \* Pooling layer. \* Simple (Python) Convolutional Neural Network to classify a handwritten digit. \* Improving the network, Regularization. \* Touch on more recent progress in image recognition, such as Residual Network (ResNet).

# **Pre-requisites:**

There is some heavier mathematics in proving the four fundamental equations behind backprogation, so a basic familiarity with multivariable calculus and linear algebra is expected, but nothing advanced is required. (The backpropagation equations can be also just accepted without bothering with the proofs since the provided python code for the simple network just makes use of the equations.)

# Speaker Background:

CL Kim works in Software Engineering at CarGurus, Inc. He has graduate degrees in Business Administration and in Computer and Information Science from the University of Pennsylvania. He has previously taught for a few years the well-rated IEEE Boston Section class on introduction to the Android platform and API.

Decision (Run/Cancel) Date for this Course is Monday, March 15

IEEE Members \$110 Non-members \$130

http://ieeeboston.org/event/neuralnetworks/?instance\_id=2987

# **Call for Course Speakers/Organizers**

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- Previous lecturers include: Dr. Eli Brookner, Dr. Steven Best, Colin Brench, to name a few.

# Python Applications for Digital Design and Signal Processing

Times and Dates (for live Q&A sessions): 7 - 8PM ET, February 4, 11, 18, 25, 2021

Speaker: Dan Boschen

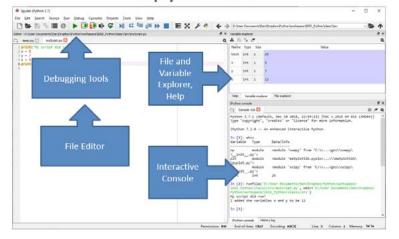
(Last Notice before Course Begins, Please Register Now!!!)

This is a hands-on course combining pre-recorded lectures with live Q&A and workshop sessions in the popular and powerful open source Python programming language.

New Format with Pre-Recorded Videos: The course format has been updated to release pre-recorded video lectures that students can watch on their own schedule, and an unlimited number of times, prior to live Q&A workshop sessions on Zoom with the instructor. The videos will also be available to the students for viewing for up to two months after the conclusion of the course.

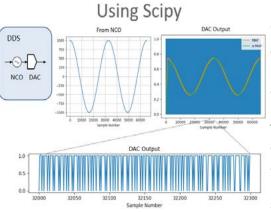
Overview: Dan provides simple, straight-forward navigation through the multiple configurations and options, providing a best-practices approach for quickly getting up to speed using Python for modelling and analysis for applications in signal processing and digital design verification. Students will be using the Anaconda distri-

Spyder IDE



bution, which combines Python with the most popular data science applications, and Jupyter Notebooks for a rich, interactive experience.

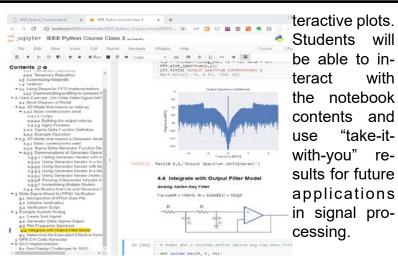
The course begins with basic Python data structures



and constructs, including key "Pythonic" concepts, followed by an overview and use of popular packages for scientific computing enabling rapid prototyping for system design.

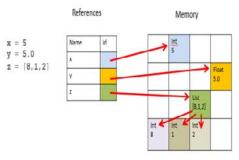
During the course students will create example designs including a sigma delta converter and direct digital synthesizer both in floating point and fixed point. This will include considerations for cycle and bit accurate models useful for digital design verification (FPGA/ASIC), while bringing forward the signal processing tools for frequency and time domain analysis.

Jupyter Notebooks: This course makes extensive use of Jupyter Notebooks which combines running Python code with interactive plots and graphics for a rich user experience. Jupyter Notebooks is an open-source webbased application (that can be run locally) that allows users to create and share visually appealing documents containing code, graphics, visualizations and in-



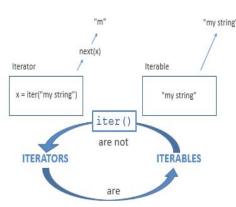
Target Audience: This course is targeted toward users with little to no prior experience in Python, however familiarity with other modern programming languages and an exposure to object-oriented constructs is very helpful. Students should be comfortable with basic signal processing concepts in the frequency and time

# Mutable / Immutable



domain. Familiarity with Matlab or Octave is not required, but the equivalent operations in Python using the NumPy package will be provided for those students that do currently use Matlab and/or Octave for signal processing applications.

# Iterable and Iterator



Benefits of
Attending / Goals
of Course: Attend"my string" ees will gain an
overall appreciation
of using Python and
quickly get up to
speed in best practice use of Python
and related tools
specific to modeling
and simulation for
signal processing

analysis and design.

A laptop (Mac or PC) preconfigured with Anaconda is required; the specific installation instructions will be emailed to students prior to the start of class.

Pre-recorded lectures (3 hours each) will be distributed Friday prior to all Workshop dates. Workshop/Q&A Sessions are 7pm-8pm on the dates listed below:

# **OUTLINE**

# Thursday, February 4

Topic 1: Intro to Jupyter Notebooks, the Spyder IDE and the course design examples. Core Python constructs.

# Thursday, February 11

Topic 2: Core Python constructs; iterators, functions, reading writing data files.

# Thursday, February 18

Topic 3: Signal processing simulation with popular packages including NumPy, SciPy, and Matplotlib.

# Thursday, February 25

Topic 4: Bit/cycle accurate modelling and analysis using the design examples and simulation packages

## **Biography:**

Dan Boschen has a MS in Communications and Signal Processing from Northeastern University, with over 25 years of experience in system and hardware design for radio transceivers and modems. He has held various positions at Signal Technologies, MITRE, Airvana and Hittite Microwave designing and developing transceiver hardware from baseband to antenna for wireless communications systems. Dan is currently at Microchip (formerly Microsemi and Symmetricom) leading design efforts for advanced frequency and time solutions.

For more background information, please view Dan's Linked-In page

Decision (Run/Cancel) Date for this Course is Thursday, January 28, 2021

IEEE Members \$190 Non-members \$210

# Modern Applications of RISC-C CPU Design

Access Period: March 1 - 31, 2021

Speaker: Steve Hoover, Redwood, EDA

<u>Type of Course: Self-paced, on-demand Course.</u>
Lab format

Course Overview: CPUs are a fundamental building block of complex SoCs, and RISC-V is taking hold as the ISA of choice. In this workshop, you will create a Verilog RISC-V CPU from scratch, and you will modify this CPU to be suitable for different applications.

You will learn and use modern techniques, using Transaction-Level Verilog to generate and modify your Verilog code more reliably, in far less time. You will discover how concepts like pipelining and hazards can be incorporated easily using timing-abstract design principles. All labs will be completed online in the Makerchip.com IDE for open-source circuit design. The skills you learn will be applicable far beyond CPU design.

# **Outline of Topics to be Covered:**

Digital logic using TL-Verilog and Makerchip

- combinational logic
- sequential logic
- pipelined logic
- validity
- a calculator circuit

Basic RISC-V CPU microarchitecture

- single-cycle CPU microarchitecture
- testbench, test program, and lab setup for your CPU
- fetch, decode, and execute logic for RISC-V subset
- control flow logic

Pipelined RISC-V subset CPU microarchitecture

- simple pipelining of the CPU
- hazards and PC redirects

Completing the RISC-V CPU

- data memory and load/store
- remaining RISC-V (RV32I) instructions

### **Course Format:**

 self paced, on demand course, providing attendees a flexible schedule

- access to content for 30 days
- pre-scheduled live Zoom and chat sessions with the instructors during the 30 day access period
- offline chat available with instructors during the entire 30 day access period (reply within 24 hours).

Target Audience: Engineers interested in a career in digital logic design or adjacent disciplines, including experienced engineers looking to modernize their skill set.

**Prerequisites:** An engineering education and basic understanding of digital logic. (Verilog knowledge is not a prerequisite.)

# **Benefits of Attending:**

- Develop a solidified understanding of pipelined CPU design through hands-on labs.
- Acquire knowledge of advanced digital circuit design methodology.
- Gain exposure to an open-source design ecosystem.

**Speaker Bio:** Steve Hoover is the founder of Redwood EDA, an early-stage startup focused on advanced silicon design methodology and tools. Steve is a former logic design lead for DEC, Compaq, and Intel and has extensive experience designing high-performance server CPUs and network switches.

**System Requirements:** All resources are free and online; no download or installation required. We will use Slack, Zoom, GitHub Classroom, and Makerchip.com.

Decision (Run/Cancel) Date for this Course is Thursday, February, 25, 2021

IEEE Members \$350 Non-members \$395

# **Call for Articles**

Now that the Reflector is all electronic, we are expanding the content of the publication. One of the new features we will be adding are technical, professional development, and general interest articles to our members and the local technology community. These will supplement the existing material already in our publication.

Technical submissions should be of reasonable technical depth and include graphics and, if needed, any supporting files. The length is flexible; however, a four to five page limit should be used as a guide. An appropriate guide may be a technical paper in a conference proceeding rather than one in an IEEE journal or transaction.

Professional development or general interest articles should have broad applicability to the engineering community and should not explicitly promote services for which a fee or payment is required. A maximum length of two to three pages would be best.

To ensure quality, technical submissions will be reviewed by the appropriate technical area(s). Professional/interest articles will be reviewed by the Publications Committee for suitability. The author will be notified of the reviewers' decision.

The Reflector is published the first of each month. The target submission deadline for the articles should be five weeks before the issue date (e.g., June 1st issue date; article submission is April 27). This will allow sufficient time for a thorough review and notification to the author.

We are excited about this new feature and hope you are eager to participate!

Submissions should be sent to; ieeebostonsection@gmail.com

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# Polar Codes - Encoding and Decoding Aspects

# Web-based Course with live Instructor!

Times & Dates: 10AM ET, Tuesdays, March 2, 9, 16, 23, Thursdays, March 4, 11, 18, 25, 2021

Speaker: Orhan Gazi, Cankaya University, Ankara-Turkey

Course Format: Live Webinar, 8 one hour, sessions

Overview: Forward error correction is a vital process in communication systems. The last channel codes discovered in the research world are the "polar codes" which are adapted to be used in 5G standard. The construction and decoding of polar codes are quite different from the construction and decoding of classical channel nodes. Polar codes are the only codes constructed in a non-trivial manner. The discovery of polar codes can be considered as a breakthrough in coding society. It is clear that future channel codes will follow the logic of polar codes. For this reason, it is critical to learn the encoding and decoding philosophy of the polar codes which is the state of art of the coding world.

### Outline of the topics to be covered:

- Entropy and Mutual Information
- Philosophy of Polar Codes
- Generator Matrices of Polar Codes
- Polar Encoder Structures
- Recursive Structures for Polar Encoders
- Channel Splitting and Concept of Channel Polarization
- Split Channels
- Calculation of Splitted Channel Capacities
- Polar Decoding
- Polar Decoding for Noiseless Transmission
- Polar Decoding Formulas for Kernel Structure for noisy Transmission
- Successive Cancelation Decoding of Polar Codes
- Polar Encoders and Decoders in 5G New Radio (NR) and Future Channel Codes

**Target Audience:** Electronic and Communication Engineers, electronic engineers, computer engineers, engineers working in communication industry

### **Benefits of Attending Course:**

1) The participant will have an idea about the state of art polar codes.

- 2) Polar codes are used in 5G standard; the participant can comprehend the polar code used in 5G standard.
- 3) The participant will learn successive cancelation decoding of polar codes.

**Speaker Bio:** Prof. Orhan Gazi is the author of the book "Polar Codes. A Non-Trivial Approach to Channel Coding" which can be reached from https://www.springer.com/gp/book/9789811307362 The book is selected by IEEE COMSOC as one of the best readings in polar codes, https://www.comsoc.org/publications/best-readings/polar-coding

Prof. Orhan Gazi is the sole author of 10 books written in electrical engineering subjects. Apart from the polar code book, he is the single author of the books "Information Theory for Electrical Engineers"

https://www.springer.com/gp/book/9789811084317 and "Forward Error Correction via Channel Coding"

https://www.springer.com/gp/book/9783030333799. The research area of Prof. Orhan Gazi involves "channel coding", and "digital communication subjects". Recently, he focuses on over capacity data transmission using polar codes. He is also interested in practical applications of communication systems involving FPGA devices. He is delivering courses with titles "VHDL circuit design", "interface design using VHDL for FPGA devices" and "system on chip design".

Materials to be included: Lecture slides will be provided.

Decision (Run/Cancel) Date for this Course is Tuesday, February, 23, 2021

IEEE Members \$250 Non-members \$300

# Software Development for Medical Device Manufacturers

# **Web-based Course with live Instructor!**

(11 hours of instructions!)

Times & Dates: 1:00 - 4:00PM ET, May 3, 4, 5, 6, 2021

Speaker: Steve Rakitin, Software Qualtiy Consulting

Course Format: Live Webinar, four, 3 hour sessions

**COURSE SUMMARY:** Developing software in compliance with the FDA Design Control regulation, changing FDA guidance documents and latest international standards is challenging. This intensive course provides practical solutions and suggestions for developing software in a manner that meets applicable FDA regulations, guidance documents and international standards, such as IEC-62304:2015. The focus is on interpreting Design Controls for software. Each section of the Design Controls regulation (820.30) is discussed from the perspective of software development. Discussions on key topics such as Software Requirements, Traceability, Design Reviews, Software Verification & Validation and Risk Management (including recently updated standards ISO-14971:2019 and EN-14971:2019) are included. Also discussed are FDA requirements for validation of software development tools and software used in Manufacturing and Quality Systems. Also discussed are recent FDA Guidance Documents on Cybersecurity, Mobile Apps, and Usability.

THIS COURSE IS INTENDED FOR: Software engineers, project managers, quality managers, software quality professionals, RA/QA staff, and anyone who needs to develop cost-effective processes and procedures that will enable their organizations to deliver high quality software-based medical devices that comply with FDA regulations and international standards. This course is also appropriate for people who are new to the medical device industry. Course notes, access to an extensive collection of reference documents and a training certificate are provided.

**COURSE OUTLINE:** This course will be presented with a live instructor using web-meeting software. The course content will be covered in 4 sessions as described below.

# SESSION 1 - Regulatory Context

Duration ~3 hours with one 15 min break
This session will cover key regulatory requirements for
medical device software in the US and EU.

### Regulations and Guidance:

- FDA Medical Device Regulation (21 CFR Part 820 specifically, design controls)
- EU Medical Device Regulation
- FDA Guidance Documents:
- Guidance for Content of Pre-market Submissions for Medical Devices Containing Software
- Off-the-Shelf Software Use in Medical Devices
- General Principles of Software Validation
- Content of Premarket Submissions for Management of Cybersecurity in Medical Devices
- Policy for Software Device Functions and Mobile Medical Applications
- Applying Human Factors and Usability Engineering to Medical Devices

### International Standards:

- ISO 13485:2016 Medical Devices Quality Management Systems
- IEC 62304: 2015 Medical Device Software Software Lifecycle Processes
- ISO 14971: 2019 Application of Risk Management to Medical Devices

- EN 14971: 2019 Application of Risk Management to Medical Devices
- Off-the-Shelf (OTS) Software and Open Source software (SOUP)
- Discussion: All Software Is Defective...

# SESSION 2 – FDA Design Controls and IEC 62304 – Part 1

Duration ~2.5 hours with one 15 min break
This session will cover FDA Design Controls and IEC
62304 requirements for medical device software.

- Design and Development Planning
  - How does Agile Development fit?
  - Medical Device Software Lifecycle Processes
- Risk Management
  - FDA Levels of Concern
  - IEC 62304 Software Safety Classification
- Software Requirements
- Techniques for Removing Ambiguity from Requirements
- Software Architecture and Design
- Software Design Changes

# SESSION 3 – FDA Design Controls and IEC 62304 – Part 2

Duration ~2.5 hours with one 15 min break This session will cover Software Verification and Validation requirements.

- Software Implementation
- Software Verification
  - Technical Reviews
  - Static Analysis
  - Unit and Integration Testing
- System Testing
- Software Validation Testing

# SESSION 4 – Software Tool Validation and Risk Management

Duration ~2.5 hours with one 15 min break This session will cover Software Tool Validation and Risk Management requirements.

Software Tool Validation

- Deciding which tools need to be validated
- Validation approach for software tools
- Validation of Manufacturing Software and Quality System Software
- Risk Management Using Fault Tree Analysis (FTA)
  - Review of ISO/EN 14971:2019 Requirements
- Example of Fault Tree Analysis and Failure Modes Effect Criticality Analysis (FMECA)

About the instructor: Steven R. Rakitin has over 45 years experience as a software engineer. He has over 30 years of experience in the medical device industry and has been a medical device consultant for over 20 years. He has worked with over 100 medical device manufacturers and biotech companies worldwide, from startups to Fortune 100 corporations. He has published papers on medical device software risk management as well as a book titled: Software Verification & Validation for Practitioners and Managers.

He received a BSEE from Northeastern University and an MSCS from Rensselaer Polytechnic Institute. He earned certifications from the American Society for Quality (ASQ) as a Software Quality Engineer (CSQE) and Quality Auditor (CQA). He is a Senior Life member of IEEE.

Steve works collaboratively with medical device companies to help them comply with FDA regulations, guidance documents, and international standards in an efficient and cost-effective manner.

Decision (Run/Cancel) Date for this Course is Monday, April 26, 2021

IEEE Members \$285 Non-members \$345

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# CALL FOR PAPERS



# 25th Annual HPEC Conference

2021 IEEE High Performance Extreme Computing Conference 21 - 23 September 2021



### www.ieee-hpec.org

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### A Note from the HPEC Committee:

IEEE HPEC will have virtual conference options that will allow safe participation and full publication in IEEE Xplore.

The IEEE High Performance Extreme Computing Conference (HPEC '21) will be held in the Greater Boston Area, Massachusetts, USA on 21 – 23 September 2021. The HPEC charter is to be the premier conference in the world on the confluence of HPC and Embedded Computing.

The technical committee seeks new presentations that clearly describe advances in high performance extreme computing technologies, emphasizing one or more of the following topics:

- Al / Machine Learning
- Graph Analytics & Network Science
- Advanced Multicore Software Technologies
- Advanced Processor Architectures
- Automated Design Tools
- Big Data & Distributed Computing
- Big Data Meets Big Compute
- Case Studies & Benchmarking of Applications
- Cloud HPEC
- Computing Technologies for Challenging Form Factors
- ASIC & FPGA Advances

- Quantum and Non-Deterministic Computing
- Data Intensive Computing
- Digital Front Ends
- Fault-Tolerant Computing
- Embedded Cloud Computing
- General Purpose GPU Computing
- High Performance Data Analysis
- Interactive and Real-Time Supercomputing
  Mapping & Scheduling of Parallel & Real-
- Time Applications
- New Application Frontiers
- Open System Architectures
- Cyber Analysis and Secure Computing

### HPEC accepts two types of submissions:

- 1. Full papers (up to 6 pages, references not included; additional pages can be purchased for \$200/page).
- 2. Extended abstracts (up to 2 pages, references included).

### IMPORTANT DATES:

Submission Deadline: JUL 9, 2021 Notification of Acceptance: AUG 13, 2021 Camera Ready Deadline: AUG 31, 2021

Preference will be given to papers with strong, quantitative results, demonstrating novel approaches or describing high quality prototypes. Authors of full papers can mark their preference for a poster display or an oral presentation. Presenters who wish to have hardware demonstrations are encouraged to mark their preference for a poster display. Accepted extended abstracts will be displayed as posters. Papers can be declared "student paper" if the first author was a student when doing the presented work, and will be eligible for the "IEEE HPEC Best Student Paper Award." Papers should not be anonymized. All paper and extended abstract submissions need to use the approved IEEE templates. Full paper submissions with the highest peer review ratings will be published by IEEE in the official HPEC proceedings available on IEEE eXplore. All other accepted submissions and extended abstracts are published on ieee-hpec.org.

Vendors are encouraged to sign up for vendor booths. This will allow vendors to present their HPEC technologies in an interactive atmosphere suitable for product demonstration and promotion. We welcome input (hpec@ieee-hpec.org) on tutorials, invited talks, special sessions, peer reviewed presentations, and vendor demos. Instructions for submitting will be posted on the conference web site shortly.

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